Innovations in Memory System Architecture: PIM and CXL-Memory

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Agenda

- PIM (Processing In Memory)
- AXDIMM (Processing Near Memory)
- CXL Memory
- SMDK (Scalable Memory Development Kit)
- Concluding Remarks
PIM (Processing-in Memory) Rationale

- System-level performance is constrained by bandwidth scaling
  - Limited by # of PCB wires, # of CPU ball, and thermal constraints
- Proposing to use PIM to improve performance of bandwidth-intensive workloads and improve energy efficiency by reducing computing-memory data movement.
Aquabolt-XL, 1st In-system Demonstrated PIM

- The first demonstrator vehicle of PIM is based on HBM2 Aquabolt, used in leading edge AI and HPC systems.
- HBM-PIM targeted to complement xPUs for optimal system balance and performance per watt for memory-bound AI workloads
  - Accelerate FP32/FP16/INT16 data processing capability in memory
- Programmable Computing Unit (PCU) integrated with memory core within HBM to enable parallel processing and minimize data movement.
- Improves the performance and energy efficiency of the system with in-DRAM processing
  - Performance: Utilize up to 4x higher in-DRAM bandwidth by multi-bank parallel operation
  - Energy Efficiency: Reduce data movement energy by utilizing in-DRAM data processing unit
Xilinx Alveo U280: HBM-PIM Evaluation

- **Performance**:
  - GEMV: 2.82x
  - ADD: 2.85x
  - LSTM: 2.54x

- **RNN-T Performance and Energy results**:
  - **RNN-T Latency (ms)**: Faster by 2.14x
  - **System Energy Consumption (J)**: Less Energy by 2.38x

- **2-HBM-PIM stacks**

- **Baseline vs PIM-enabled**
  - Baseline
  - PIM-enabled
AXDIMM – Near Memory Compute

- CPU-memory data movement bottlenecks system performance → Use rank-level parallelism
  - Instead of processing in-memory, AXDIMM places compute on buffer with commodity DRAM on memory module
  - Near-Memory Compute instead of In-Memory Compute. Same idea – alleviate von Neumann memory bus bottleneck
  - Samsung to provide AXDIMM SW stack to offload the acceleration functions in AXB(AXDIMM Buffer)

- Improve the performance and energy efficiency of the system with in-DIMM processing
  - Utilize up to higher in-DIMM bandwidth by multi-Rank parallel operation, 1.8x by 2-rank
  - Reduce data movement energy by utilizing in-DIMM data processing unit, -42.6% by 2-rank
AXDIMM Evaluation System and Results

- x86 based platform with Xilinx Zynq Ultrascale+ FPGA Chip configured as AXDIMM
- Enabled RecNMP* logic
  - Achieved 1.8x SLS execution speed-up from HW
- Modified DLRM** application utilizing AXDIMM
  - Achieved 1.8x/3.5x/6.9x QPS

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In/Near Memory Compute Future

- Wider target applications
  - PIM unit supporting multiple functions
- Various DRAM types
  - LPDDR5, DIMM-DDR5, GDDR6, HBM3
- New standards for PIM
  - Command truth table/timing for PIM

- Addendum or addition to current product specs, not new generations
  - Enhanced performance
  - Reduced energy
- Collaborate with industry
  - Supporting custom functions
  - Investigating CXL enablement
CXL Device Types

Caching Devices / Accelerators

- **TYPE 1**
  - Processor
  - DDR
  - CXL
  - CXL.io
  - CXL.cache
  - Accelerator NIC
  - Cache
  - USAGES:
    - PGAS NIC
    - NIC atomics

Accelerators with Memory

- **TYPE 2**
  - Processor
  - DDR
  - CXL
  - CXL.io
  - CXL.cache
  - CXL.memory
  - Accelerator
  - Cache
  - USAGES:
    - GP GPU
    - Dense computation

Memory Buffers

- **TYPE 3**
  - Processor
  - DDR
  - CXL
  - CXL.io
  - CXL.memory
  - Memory Buffer
  - Memory
  - Memory
  - Memory
  - USAGES:
    - Memory BW expansion
    - Memory capacity expansion
    - Storage class memory

Samsung CXL Type 3 Memory

- Form Factor

- CXL Specification
  - 2.0

- Media
  - DDR5

- Capacity
  - 128 GB to TBD

- Other Features (under consideration)
  - Dual Port

Memory Pooling with CXL Type 3 Memory

Multiple hosts using pooled memory, attaining memory capacity for exclusive use for certain duration, as needed – through CXL switch

Two hosts using pooled memory, attaining memory capacity for exclusive use, as needed
New learnings in
• Component placement
• Routing
• Signal Integrity
• Power Integrity
• Thermal
• Firmware Development

Form Factors
• HDD: 5.25” → 3.5” → U.2
• SSD: U.2 → EDSFF
• CXL: EDSFF → ??
CXL Memory Development

- Bandwidth
- Latency
- Cost
- Power
- Capacity
- QoS

- Media controller ownership
  - RAS Features
  - Security Features
  - Thermal Management
  - Persistence Management
  - Media Management
    - DRAM
    - DDRx
    - LPDDRx
    - Future Memory
SMDK: Scalable Memory Development Kit

Compatible API
: Supports Memory Expander application without application SW modification

Optimization API
: Supports high-level optimization by modifying the SW application

Intelligent Tiering Engine
: Supports different use cases by tiering priorities / capacities / bandwidth among memories

Memory Pool Management
: Separate management of normal memory and CXL.Mem
: Supports scalability according to CPU memory capacity change

Memory Zone
: Optimized management preventing mixed usage of different memories

SMDK Architecture & Full-stack SW/HW System
* Full-stack : DC to Edge application + SMDK + CXL Memory Expander + CPU System

Datacenter to Edge Applications (IMDB, DLRM, ML/AI, etc)
SMDK Summary

• Open-source software tool to
  • Facilitate CXL memory deployment without the need to modify existing applications
  • Or, allow application programmers to optimize use of memory with different BW/latency characteristics

• Development framework to lays the foundation to managing memory tiering, Intelligent data flow, advanced RAS features

• Now available on a limited basis for initial testing and optimization and will be open-sourced within the first half of next year

• CXL Memory Demo w/SMDK @ OCP

CXL Memory OCP Demo

1. Memory Allocation Demo
   - CXL memory zone allocation with SMDK (CXL zone vs Main memory zone)

2. IMDB(Redis) Functional Test Demo
   - Running Redis and Memcached on CXL memory, CXL+DRAM with SMDK (w/o performance test)
   - SMDK is Samsung’s s/w development kit which contains CXL memory allocator

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**IMDB(Redis/Memcached) function test demo**

- **Memcached Client**
  - Set
  - Get
- **Redis Client**
  - Set
  - Get

**SMDK(Scalable Memory Dev. Kit)**

**CXL Kernel**

**CXL Memory Allocator**

**SW**
- Memcached Container
- Redis Container
- Memcached Server
- Redis Server
- CXL Memory Allocator

**HW**
- CXL Expander Mem
- DDR5
- CPU/Mainboard (iboF V2 / CRB)

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**SMDK Architecture**

- **Scalable memory development kit allows for easy and optimized deployment of heterogeneous memory**
  
  ① Compatible & Optimization API
  ② Intelligent Memory Tiering (priority/capacity/bandwidth)
  ③ Separate MGMT. of Normal/CXL Memory

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**OCP Demo Scenario**

- **Scalable memory development kit**
- **CXL Memory Allocator**
- **CXL Memory Zone**
- **CXL Kernel**
- **Memory Expander**
- **Normal ZONE**
- **CXL Mem ZONE**
- **Datacenter to Edge Applications (IMDB, DLRM, ML/AI, etc)**

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**SMDK Architecture**

- **CXL Allocator**
  - Compatible API
  - Optimization API
- **Intelligent Tiering Engine**
- **Memory Pool Mgmt**
Concluding Remarks

- Must understand application requirements in context of (ever evolving) Memory Hierarchy
- Move data where it is needed, when needed
- Don’t move data if it can be avoided
  - Local, heterogeneous computing
- Software (as always) key to manage (or reduce/eliminate) data movement for performance and energy efficiency improvement
- CXL will be key interface for enabling development of new media and SDM system architecture, as well as heterogeneous computing system architecture

* In package memory
** Storage Class Memory