



HETEROGENEOUS
INTEGRATION ROADMAP

Heterogeneous Integration Roadmap

<http://eps.ieee.org/technology/heterogeneous-integration-roadmap.html>

Presentation at ODSA Workshop

September 12th, 2019

William Chen (ASE)

WR Bottoms (3MTS)

Marc Hutner (Teradyne) Jeffrey Demmin (Darpa, Booz Allen)

Presentation Outline

- Introduction and brief history of Semiconductor technology
- Heterogeneous Integration is the path forward
- Heterogeneous Integration in the smartphone
- Heterogeneous integration in high performance applications
- Heterogeneous Integration Roadmap
- Summary

Introduction and brief history of the Semiconductor technology

54 Years After Moore's Law The World Has Changed...

**CMOS Scaling Is no longer Driving The Pace Of Progress
The ITRS Is Over**

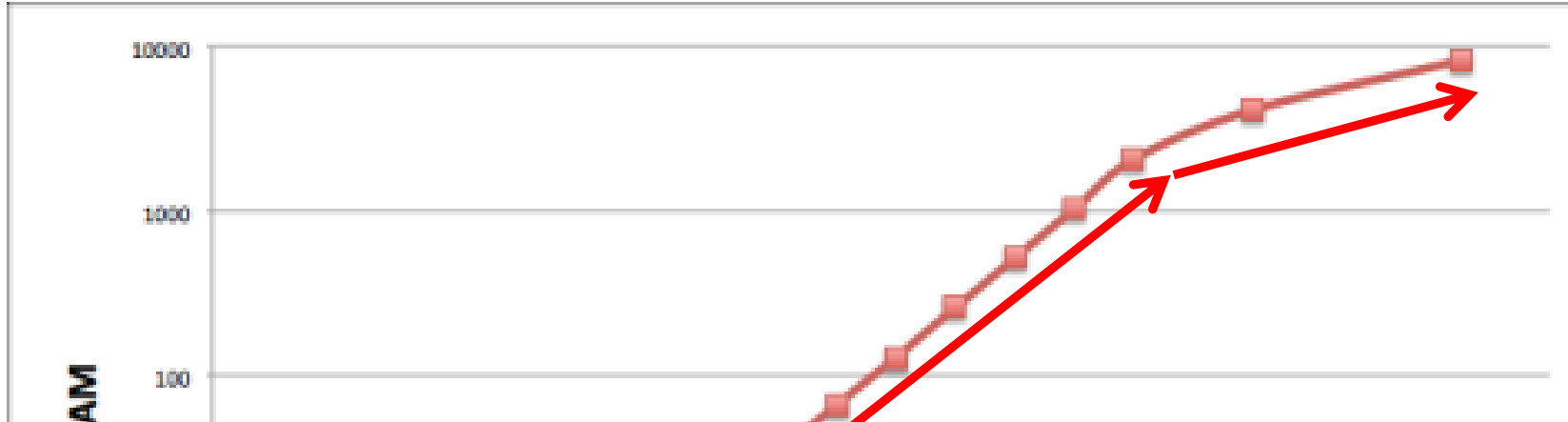


....the world has evolved and is changing in ways never imagined.

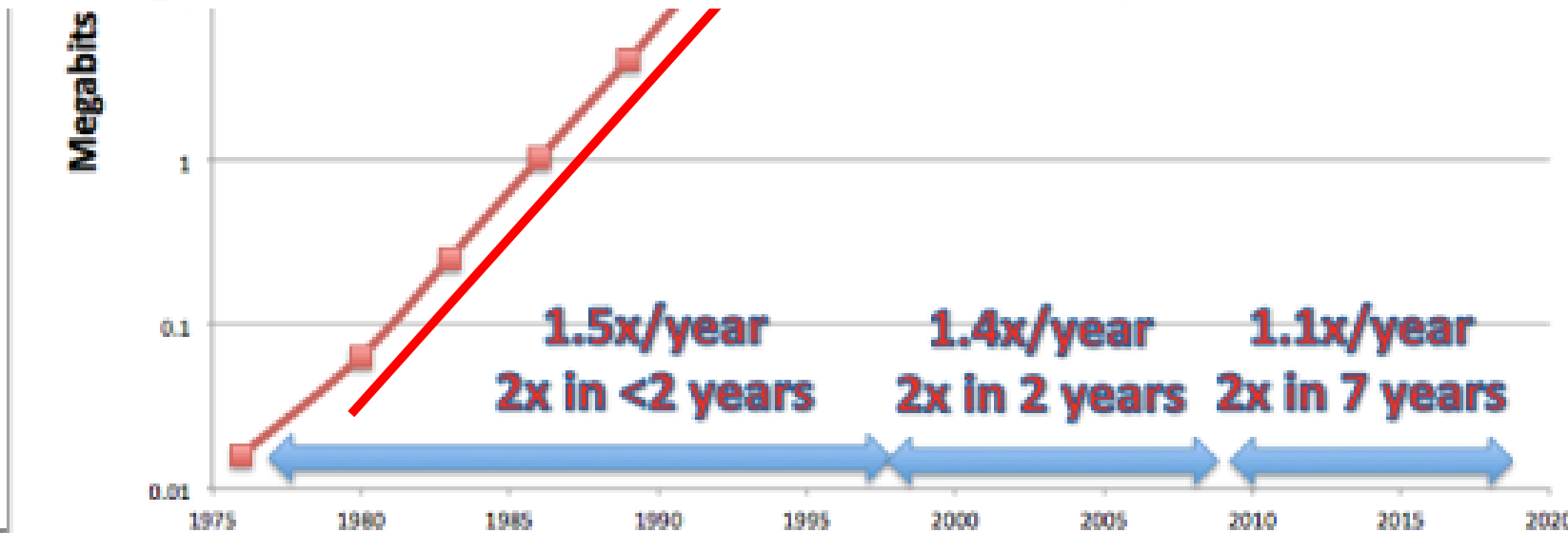
We are entering a period of technology chaos driving new ideas that increase the pace of innovation

40 Year DRAM Memory Capacity Increase

John Hennessy at DARPA ERI Conference July 2018

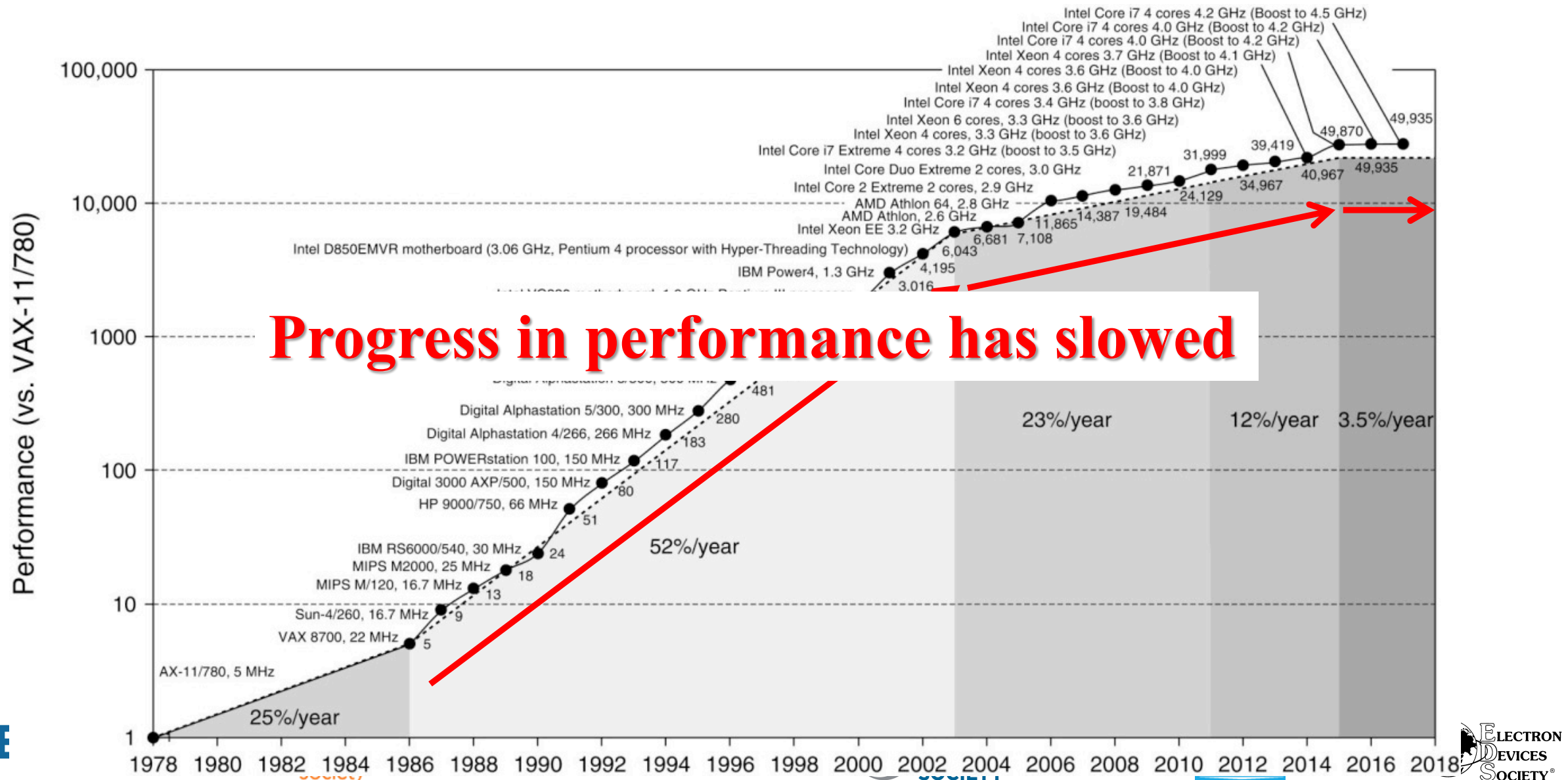


Progress in functional density has slowed



40 Years Of Progress In Computing

John Hennessy at DARPA ERI Conference July 2018



Technology Roadmapping History

1991

World's first Open Source Technology Roadmap, the National Technology Roadmap for Semiconductors (NTIS) sponsored by the US Semiconductor Industry Association

1998

NTIS expanded forming the first Global Technology Roadmap. Europe, Japan, Taiwan, and Korea joined. It was renamed International Roadmap for Semiconductors (ITRS).

2014

The benefits of Moore's Law scaling diminishing and decision was made to end ITRS.

2016

The last edition of the ITRS was published July 8, 2016

Technology Roadmapping History

In March of 2015 the ITRS Heterogeneous Integration Focus Team signed a Memorandum of Understanding with the IEEE CPMT Society initiating the formation of the Heterogeneous Integration Roadmap



Heterogeneous Integration Roadmap (HIR)



HIR was founded with initiative from three IEEE Societies (Electronics Packaging Society, Electron Devices Society, Photonics Society), SEMI and ASME EPPD. It is dedicated to embrace innovation wherever it arises and promote collaboration wherever possible to accelerate progress in the microelectronics market landscape.



Heterogeneous Integration is the path forward

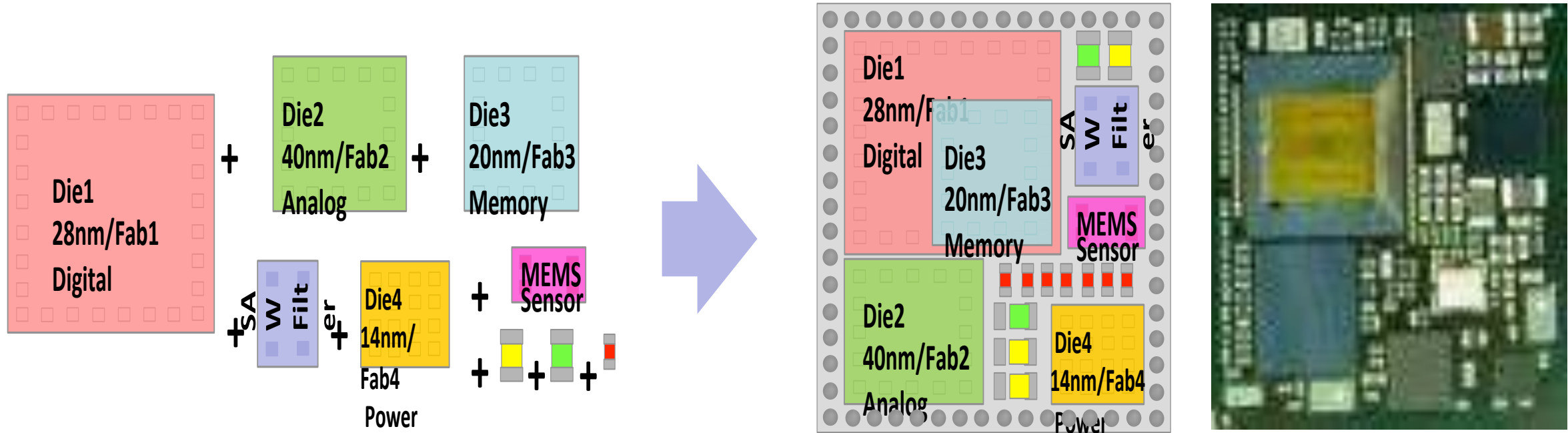
Semiconductor Research Opportunities

“An Industry Vision & Guide”

SIA & SRC March 2017

“The path forward is not as clear as it was during the Moore’s Law era. However, the enormous potential for economic and societal benefits—some that are envisioned and others yet to be imagine.”

The Definition of Heterogeneous Integration



Die/Package, Heterogeneous Components

System-in-Package (SiP)

Heterogeneous by material, component type, circuit type, node and bonding/interconnect method

Purpose and Theme of Heterogeneous Integration

Maintain the pace of progress needed for electronic systems today and tomorrow by integration of separately manufactured components into a higher level assembly that provides enhanced functionality and improved operating characteristics.

A pre-competitive technology roadmaps addressing future vision, difficult challenges, & potential solutions.

Volunteer driven for benefit of electronics ecosystem

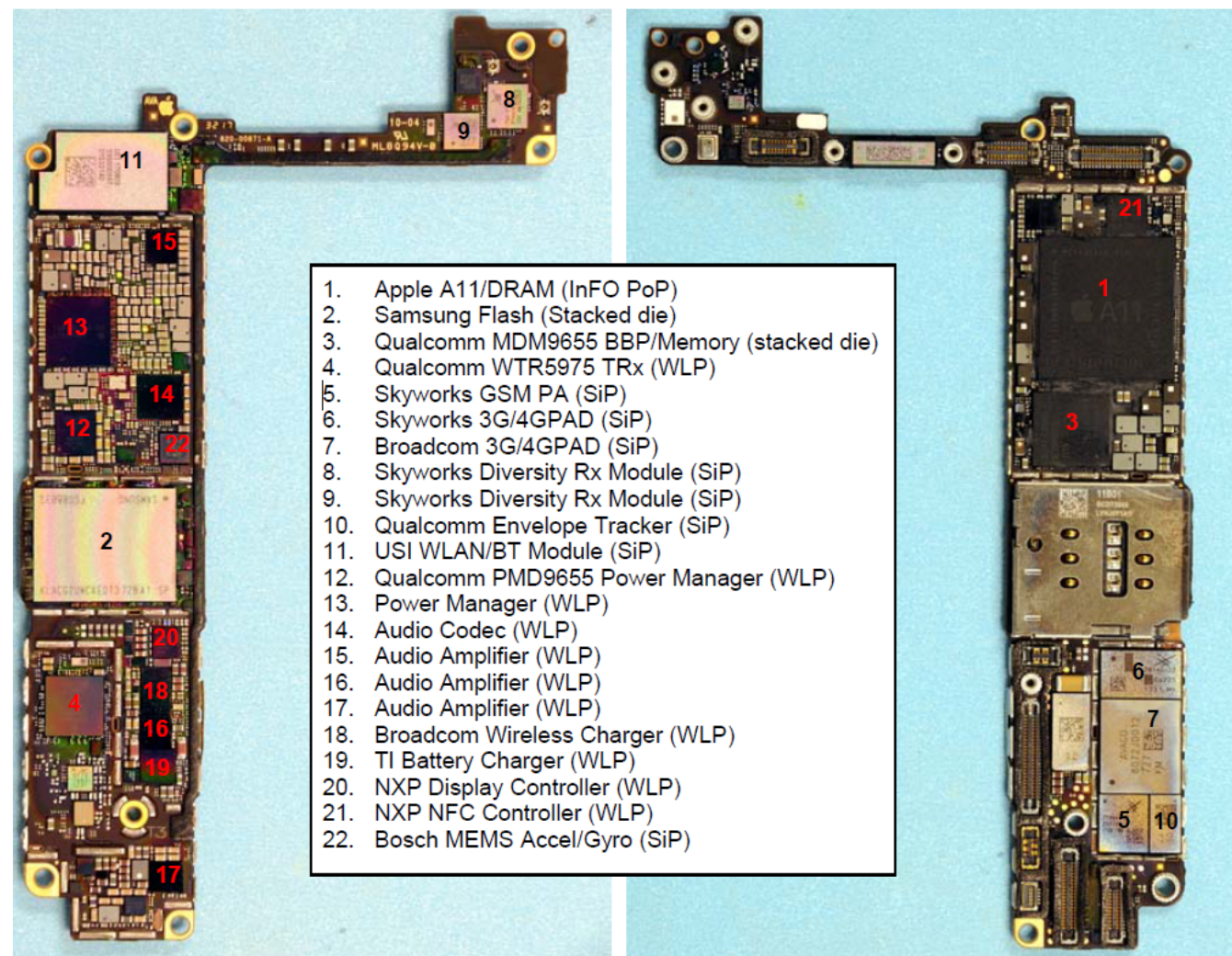
Heterogeneous Integration in the Smartphone

Apple iPhone X Main Board

Source Prismark Partners

- Main processor A11 in Package on Package (PoP)
- 8 other System in Package (SiPs)
- 11 WLCSPs

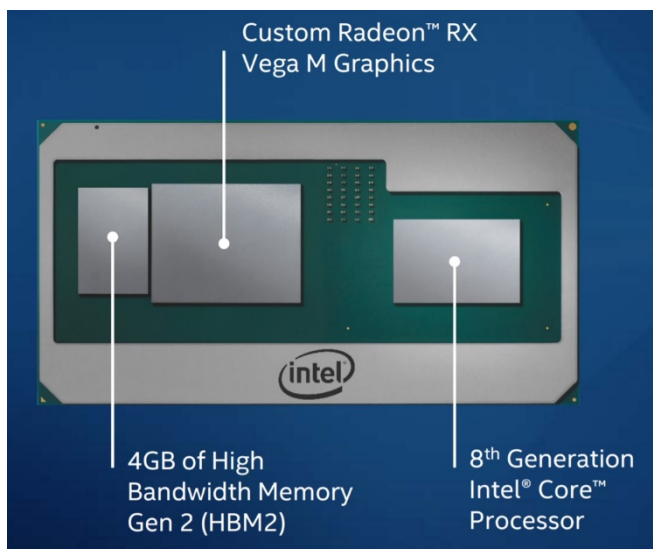
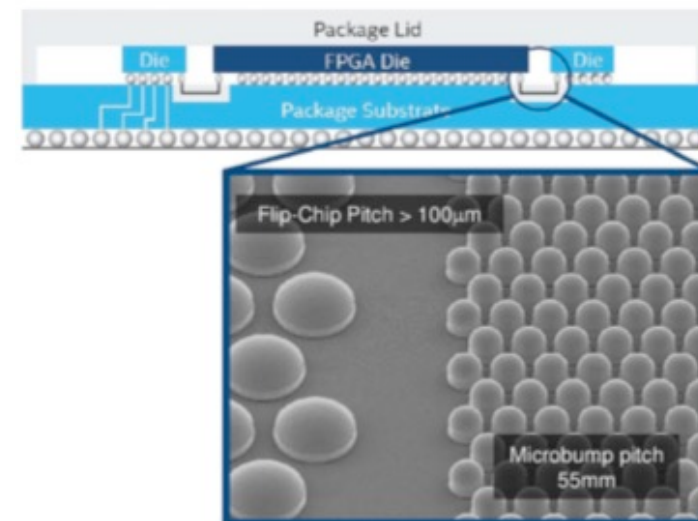
Teardowns of APPLE XSMaX, Samsung Galaxy S9+ and Huawei 20 Pro all show similar adoption of leading edge Heterogeneous Integration



Heterogeneous Integration in High Performance Applications

Intel's Embedded Multi-die Interconnect Bridge

EMIB is high bandwidth link between multiple die of different nodes and circuit types on organic substrate



EMIB example: Intel Kaby Lake G card with Intel CPU, AMD GPU and 4GB HBM2.

Heterogeneous Integration Roadmap

Heterogeneous Integration Roadmap (HIR)



HIR was founded with initiative from three IEEE Societies (Electronics Packaging Society, Electron Devices Society, Photonics Society), SEMI and ASME EPPD. It is dedicated to embrace innovation wherever it arises and promote collaboration wherever possible to accelerate progress in the microelectronics market landscape.



HIR's 22 Technical Working Groups



HI for Market Applications

- Mobile
- IoT
- Medical, Health & Wearables
- Automotive
- High Performance Computing & Data Center
- Aerospace & Defense

Heterogeneous Integration Components

- Single Chip and Multi Chip Packaging (including Substrates)
- Integrated Photonics
- Integrated Power Electronics
- MEMS & Sensor integration
- RF and Analog Mixed Signal

Cross Cutting topics

- Materials & Emerging Research Materials
- Emerging Research Devices
- Interconnect
- Test
- Supply Chain
- Security
- Thermal Management

Integration Processes

- SiP
- 3D +2.5D
- WLP (fan in and fan out)

Design

- Co-Design & Simulation – Tools & Practice

HIR 2019 Event Schedule



HETEROGENEOUS
INTEGRATION ROADMAP

1. [Heterogeneous Integration Roadmap Symposium](#) Milpitas, CA 2/21/2019
2. [SEMICON China](#), Shanghai, China CSTIC 3/18-19/2019
3. [EuroSimE](#) Hannover, Germany 3/24-27/2019
4. [ICEP](#) Niigata 4/17-20/2019
5. [ECIO](#) Ghent, Belgium 4/24-26/2019
6. [Advanced Semiconductor Manufacturing Conference](#) 5/6-9/195.
8. [ECTC](#) & [ITherm](#) Las Vegas, NV 5/28-31/2019
9. [NordPac](#) Denmark 6/11-13/2019
10. Palo Alto Workshop, Palo Alto, CA, July 8, 2019
11. [SEMICON West](#) San Francisco, CA 7/9-11/2019
12. [ICEPT](#) Hong Kong 8/11-15/2019
13. [Electronics Packaging Symposium](#) Niskayuna, NY 9/2019
14. HIR Workshop with EPS Japan, JIEP & SEMI Japan Tokyo, Japan TBD
15. [IMAPS](#) Boston, MA 10/1-3/2019
16. [International Test Conference](#) Washington D.C., 11/12-14/2019
17. [INTERPACK 2019](#) Anaheim, CA 10/7-9/2019
18. [IMPACT](#) Taiwan 10/24-26/2019
19. [SEMICON Europa](#) Germany 11/12-15/2019
20. [ICSJ](#) Kyoto, Japan 11/18-20/2019

HIR Global Advisory Council



- **Ajit Manocha** - President and CEO of SEMI. Former CEO of GlobalFoundries and served as chair of SIA. Also served in executive roles at Philips/NXP & Spansion.
- **Nicky Lu** - Founder and Chairman of Etron Technology in Taiwan. Served as chair of TSIA and WSC and is a member of the US National Academy of Engineering.
- **Babak Sabi** - Intel Corporation Corporate Vice President, General Manager, Assembly Test Technology Development.
- **Hubert Lakner** - Board of Directors Chairman, Fraunhofer Microelectronics Group and Founding Director of Fraunhofer Institute of Photonic Microsystems (IPMS) in Dresden.



HIR International Roadmap Committee

- William (Bill) Chen , ASE Fellow & Senior Technical Advisor, (Chair)
- W. R Bottoms, Chairman 3MTS (Co-Chair representing EPS)
- Subramanian Iyer, Distinguished Professor UCLA (representing EDS)
- Amr Helmy, Chair Professor , U Toronto (Representing Photonics)
- Tom Salmon, VP SEMI Collaboration Platform (Representing SEMI)
- Ravi Mahajan, INTEL Fellow (Representing ASME EPPD)
- Gamal Refai-Ahmed, Distinguished Engineer Xilinx (ASME EPPD alternate)

Summary

1. Progress paced by Moore's Law with focus on CMOS is reaching its economic end.
2. There is immense need for pre-competitive technology roadmaps addressing future vision, difficult challenges, & potential solutions
3. HIR is focused on system level integration at the package level addressing emerging markets and enabling continued progress at the rate of Moore's Law for decades to come.

We are very excited at the ODSA goals &
significant Chiplet progress

**We would like to find ways
to Collaboration and Cooperate
For benefit of All**