PIPE Adapters
ODSA Project Workshop
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Multiple chiplets need to function as though they are on one die.
All USR SerDes need PIPE adapters

None of the USR SerDes on the market support the PIPE interface directly
PIPE arose from Intel and the PCIe world
Each of USR SerDes arose out of the LAN/WAN world and not the PCIe/CCIX world

All of the USR SerDes run faster than PCIe individual SerDes and need to bundle PCIe lanes
An XSR SerDes runs at 112 Gb/s and can carry 3 ½ PCIe Gen 5 (32 GT/s) lanes
The Kandou Glasswing runs at 500 Gb/s and can carry 16 PCIe Gen 5 (32 GT/s) lanes
The Aquantia AQLink SerDes also functions along these lines (ask Ramin)

Fortunately, the adapters needed are routine
Kandou PIPE Adapter

An application note exists that describes the PIPE adapter in detail. A summary is:

Divide the 640-bit system side interface into sixteen 40-bit slots
Feed the data from each of 16 PIPE interfaces into the sixteen slots
Arrange the clocks to match up
Create a matching configuration interface to pretend to be sixteen PIPE interfaces to PCIe or CCIX controllers and their associated software and power modes

PIPE adapters for XSR and AQLink would presumably be similar

Probably need lightweight framing layer
XSR uses PAM-4 and must have Forward Error Correction (FEC) with its latency
Product Development

To my knowledge, PIPE adapters do not exist in product form for any of the SerDes options.

While the complexity level is modest as compared to the SerDes themselves, the development of a PIPE interface would need to be attended to.

Test chips would increase the confidence in such a development.