PIPE Adapters

ODSA Project Workshop

March 28, 2019
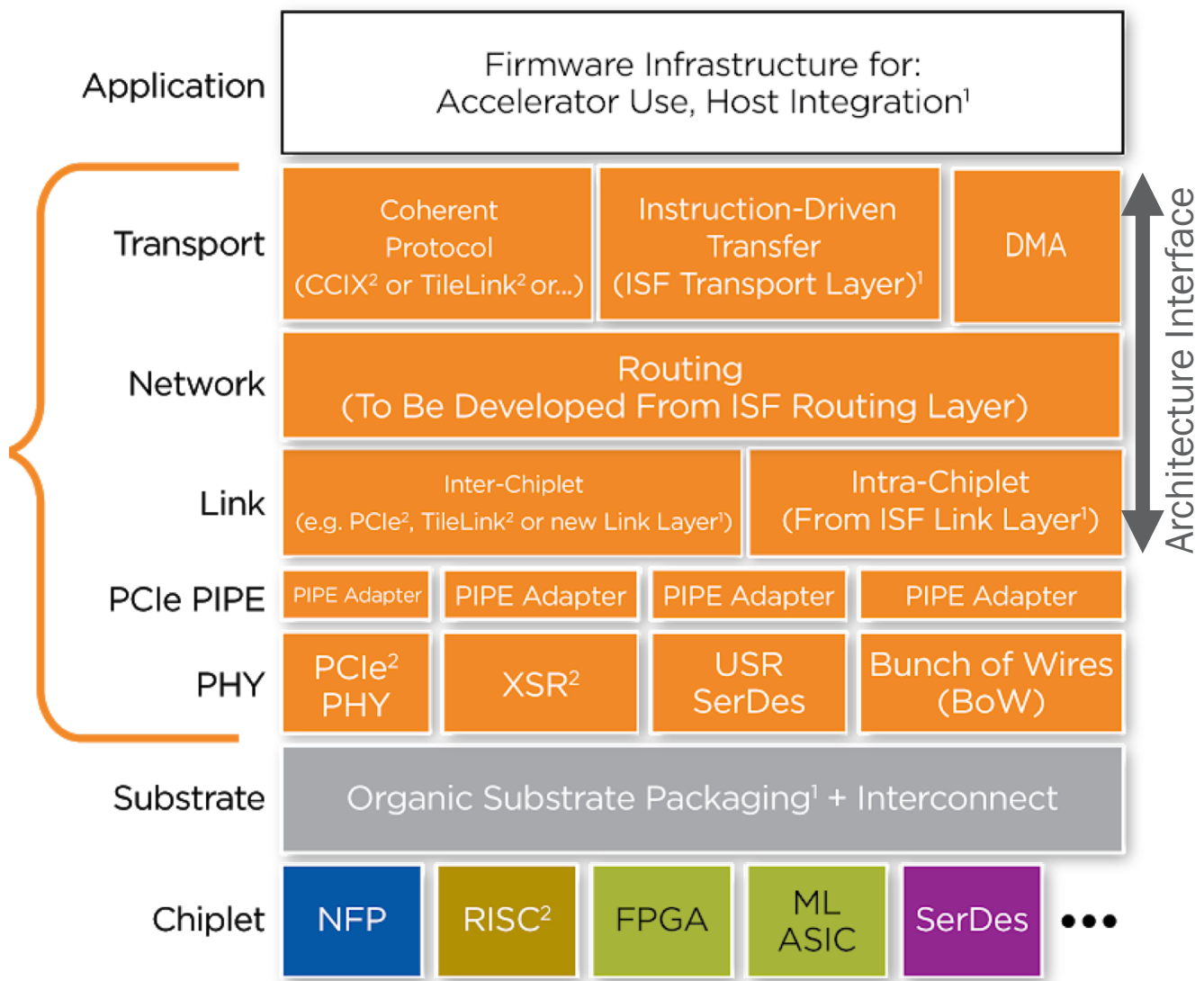
Open Interface for Chiplet-Based Design

Switch Fabric Interconnect the Logic Blocks Inside the NFP Device

CPU Cores

Memory Engines

Hardware Accelerators

Flow Processing Cores

MAC/SerDes Network Ports

PCIe Host Interfaces

Long Reach SerDes — XSR — XSR — NFP — CCIX — CCIX — RISC CPU

USR

USR

ASIC or FPGA or ManyCore

ORGANIC SUBSTRATE

Open Chiplets Connectivity Specification
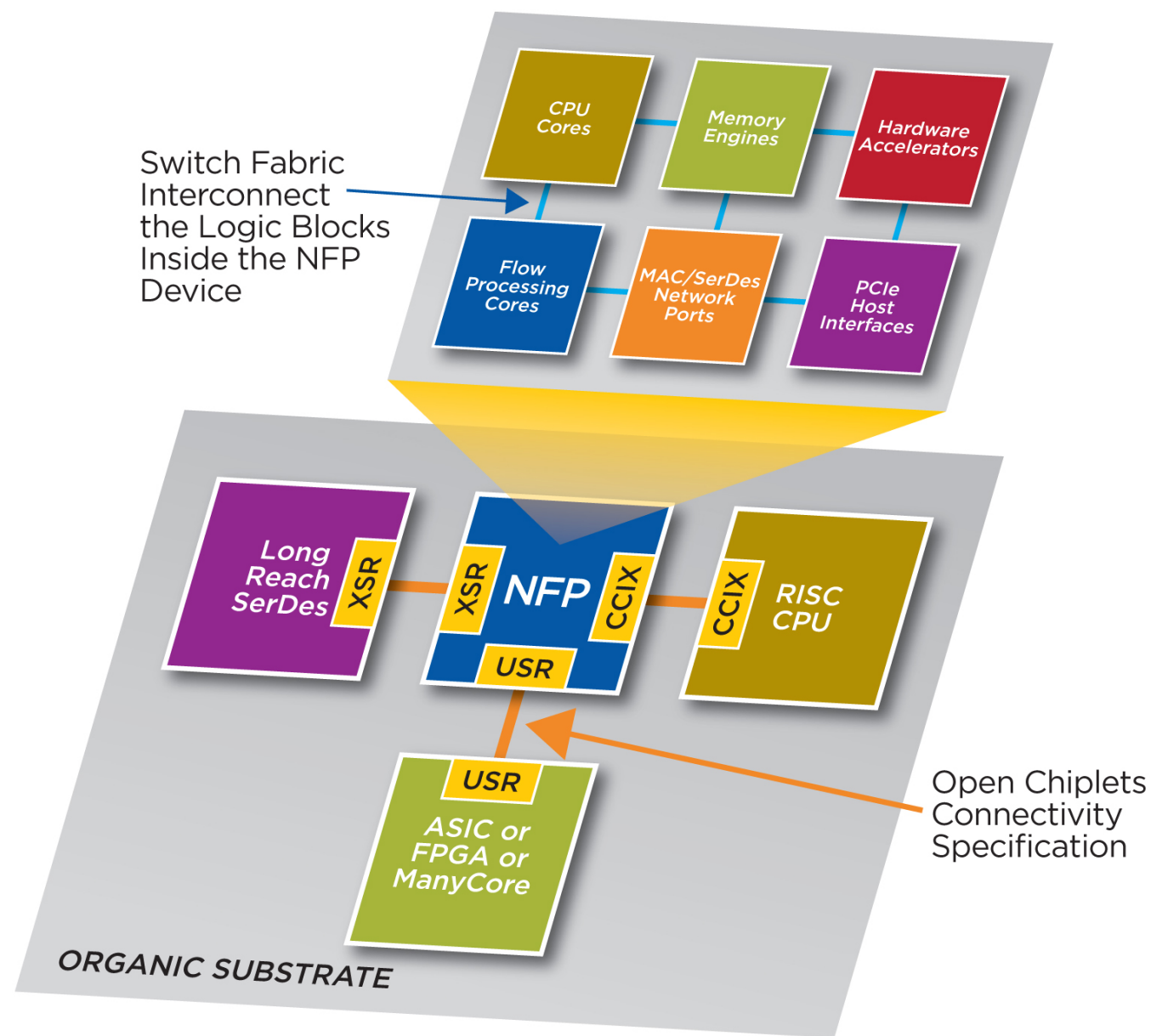
Multiple chiplets need to function as though they are on one die

Consume. Collaborate. Contribute.

Application	Firmware Infrastructure for: Accelerator Use, Host Integration[1]		
Transport	Coherent Protocol (CCIX[2] or TileLink[2] or…)	Instruction-Driven Transfer (ISF Transport Layer)[1]	DMA
Network	Routing (To Be Developed From ISF Routing Layer)		
Link	Inter-Chiplet (e.g. PCIe[2], TileLink[2] or new Link Layer[1])	Intra-Chiplet (From ISF Link Layer[1])	
PCIe PIPE	PIPE Adapter / PIPE Adapter / PIPE Adapter	PIPE Adapter	
PHY	PCIe[2] PHY / XSR[2] / USR SerDes	Bunch of Wires (BoW)	
Substrate	Organic Substrate Packaging[1] + Interconnect		
Chiplet	NFP / RISC[2] / FPGA / ML ASIC / SerDes •••		

Architecture Interface

[1] New Open IP/Specification
[2] Existing Open Standard

Source: ODSA
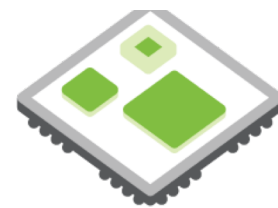
All USR SerDes need PIPE adapters

None of the USR SerDes on the market support the PIPE interface directly

   PIPE arose from Intel and the PCIe world

   Each of USR SerDes arose out of the LAN/WAN world and not the PCIe/CCIX world

All of the USR SerDes run faster than PCIe individual SerDes and need to bundle PCIe lanes

   An XSR SerDes runs at 112 Gb/and can carry 3 ½ PCIe Gen 5 (32 GT/s) lanes

   The Kandou Glasswing runs at 500 Gb/s and can carry 16 PCIe Gen 5 (32 GT/s) lanes

   The Aquantia AQLink SerDes also functions along these lines (ask Ramin)

Fortunately, the adapters needed are routine
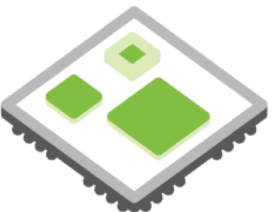
Kandou PIPE Adapter

An application note exists that describes the PIPE adapter in detail. A summary is:

Divide the 640-bit system side interface into sixteen 40-bit slots

Feed the data from each of 16 PIPE interfaces into the sixteen slots

Arrange the clocks to match up

Create a matching configuration interface to pretend to be sixteen PIPE interfaces to PCIe or CCIX controllers and their associated software and power modes

PIPE adapters for XSR and AQLink would presumably be similar

Probably need lightweight framing layer

XSR uses PAM-4 and must have Forward Error Correction (FEC) with its latency
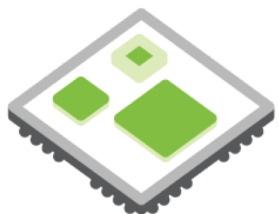
Product Development

 To my knowledge, PIPE adapters do not exist in product form for any of the SerDes options

While the complexity level is modest as compared to the SerDes themselves, the development of a PIPE interface would need to be attended to

Test chips would increase the confidence in such a development