

# Using In-Chip Monitoring and Deep Data Analytics for High Bandwidth Die-to- Die Reliability

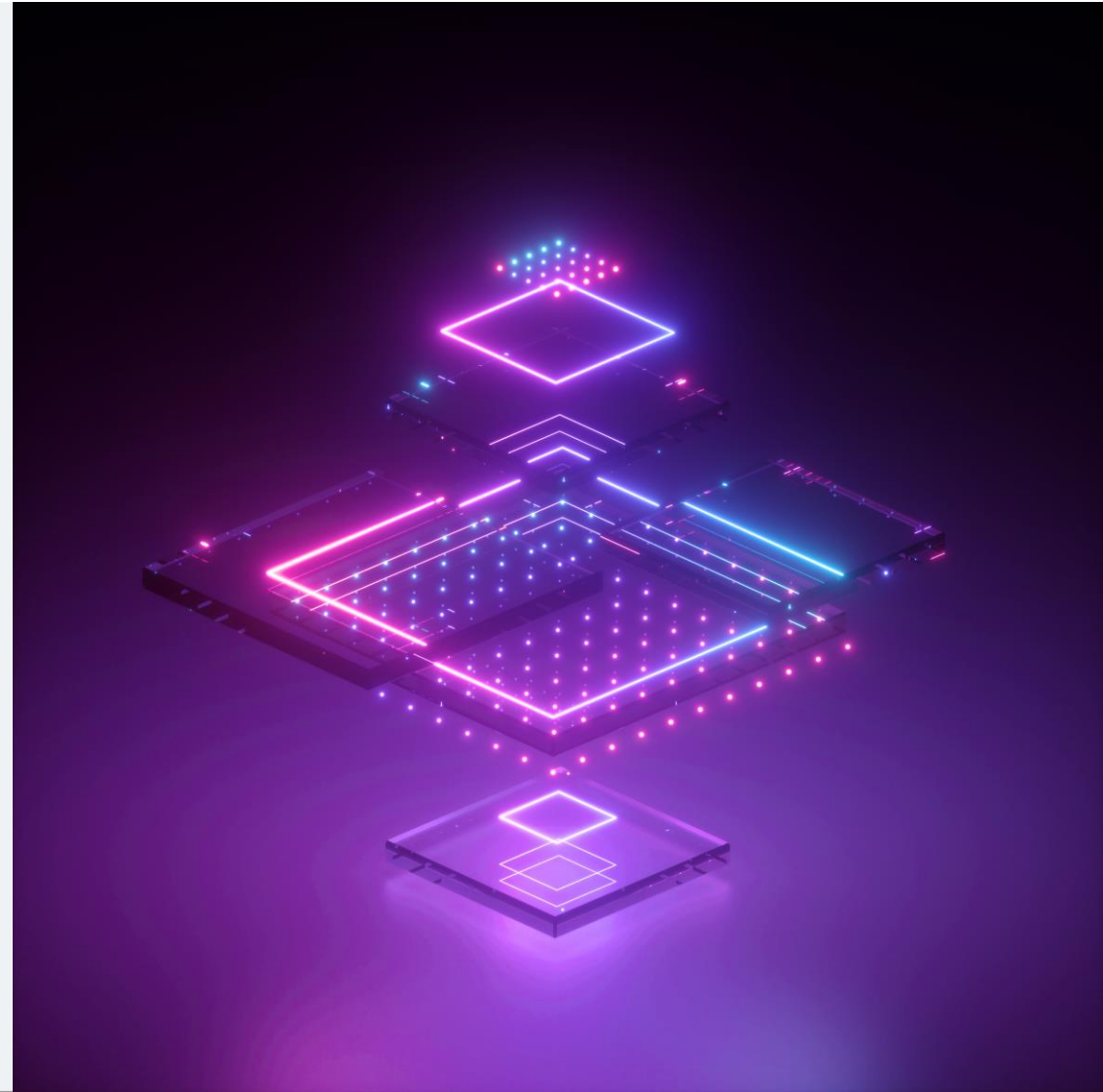
Alex Burlak, VP Test & Analytics

19 June 2022



# More Than Moore

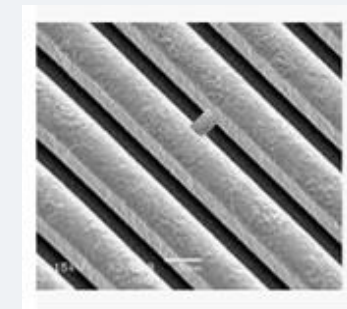
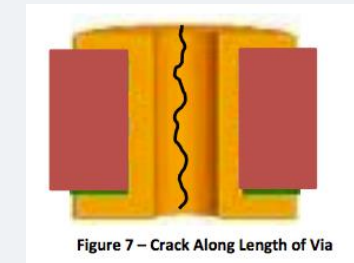
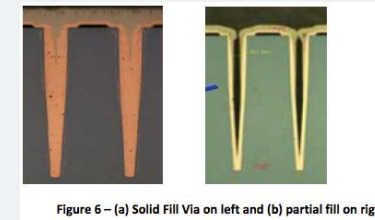
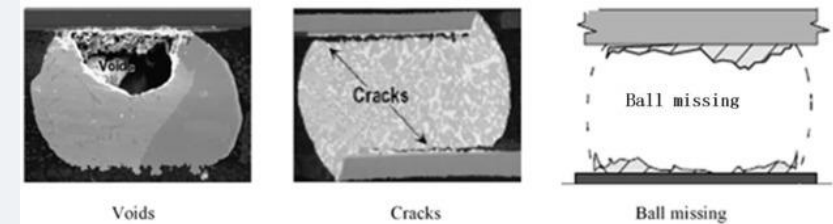
- Allow overcoming reticle size limitations for large devices
- Improve yield: Yield goes down exponentially with size but with tiling, it is linear
- Allow hybrid devices: Each IC in a SiP can be manufactured at a different process:
  - CPU/GPU/NPU/TPU on latest CMOS technology
  - DRAM on DRAM process
  - Wireless/RF on Analog RF process
- Support “economies of scale” with Chiplet
  - Uses the same building block multiplied according to application instead of multiple designs



# Heterogeneous Integration

## Quality and Reliability Challenges

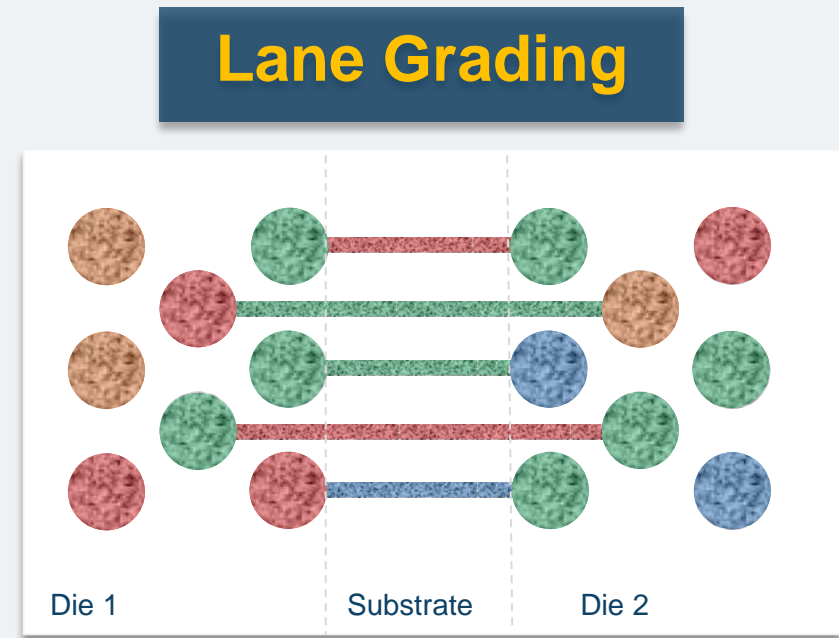
- Bump Reliability
  - Voids and cracks
- TSV Reliability
  - Partial fill
  - Copper plating cracking
- Lane Trace Reliability
  - Bridge shorts
- Driver and Receiver
  - Parametric variation
  - Aging (driver weakening, VREF shift, etc.)



**Thousands to millions of potential failure points, no visibility!**

# Per-Lane **High Resolution Monitoring**

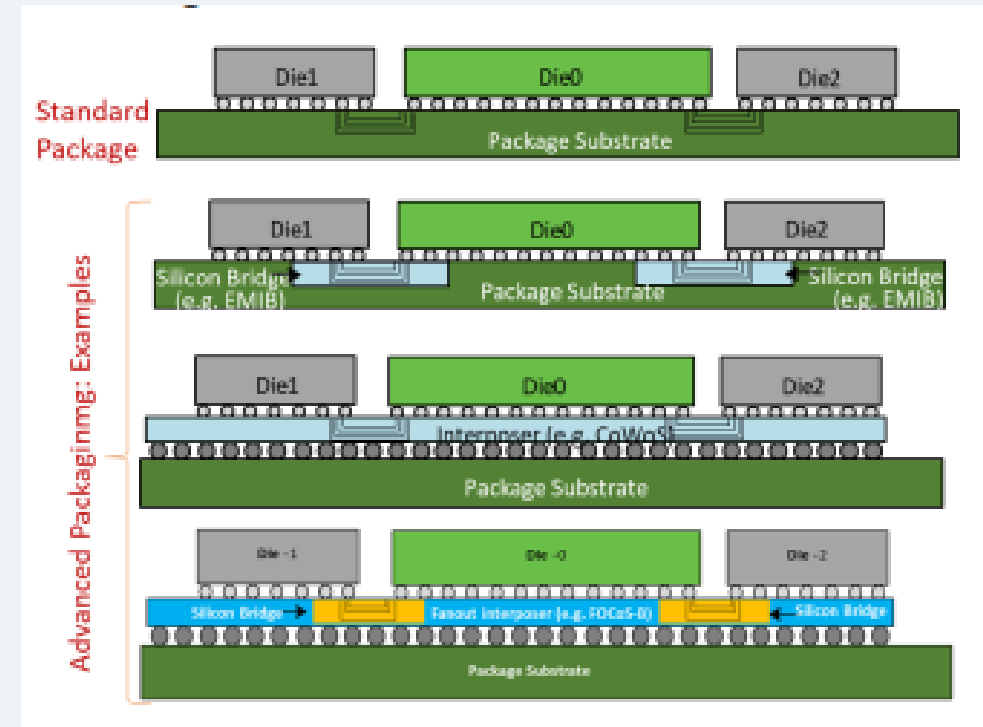
- Comprehensive parametric lane grading
- 100% lane coverage
- During test and in-mission
- Data analytics capabilities
- Patent protected



- **Go beyond just Pass/Fail testing**
- **Part of proteanTecs comprehensive chip performance and health monitoring solutions**

# Visibility at Every Stage, from Production to the Field

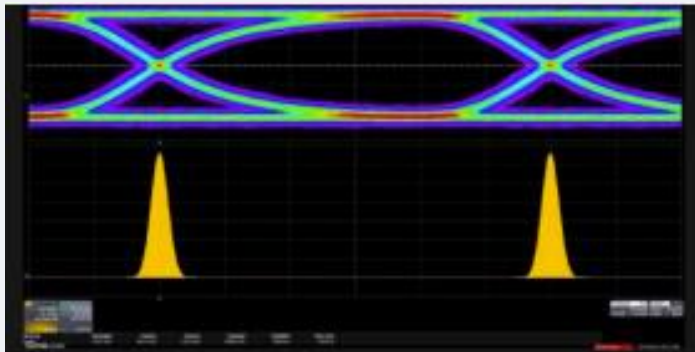
- NPI and Characterization
  - Lane performance (eye width and jitter) under PVT range
  - Test coverage and test time optimization
  - Inter-lane skew and cross-talk characterization
- Mass Production (MP)
  - Outlier detection (assembled unit)
  - Spare lane activation (if available)
  - Yield monitoring and early alerting
- In-field Reliability
  - Lane degradation for Predictive Maintenance (spare lane, module swap)



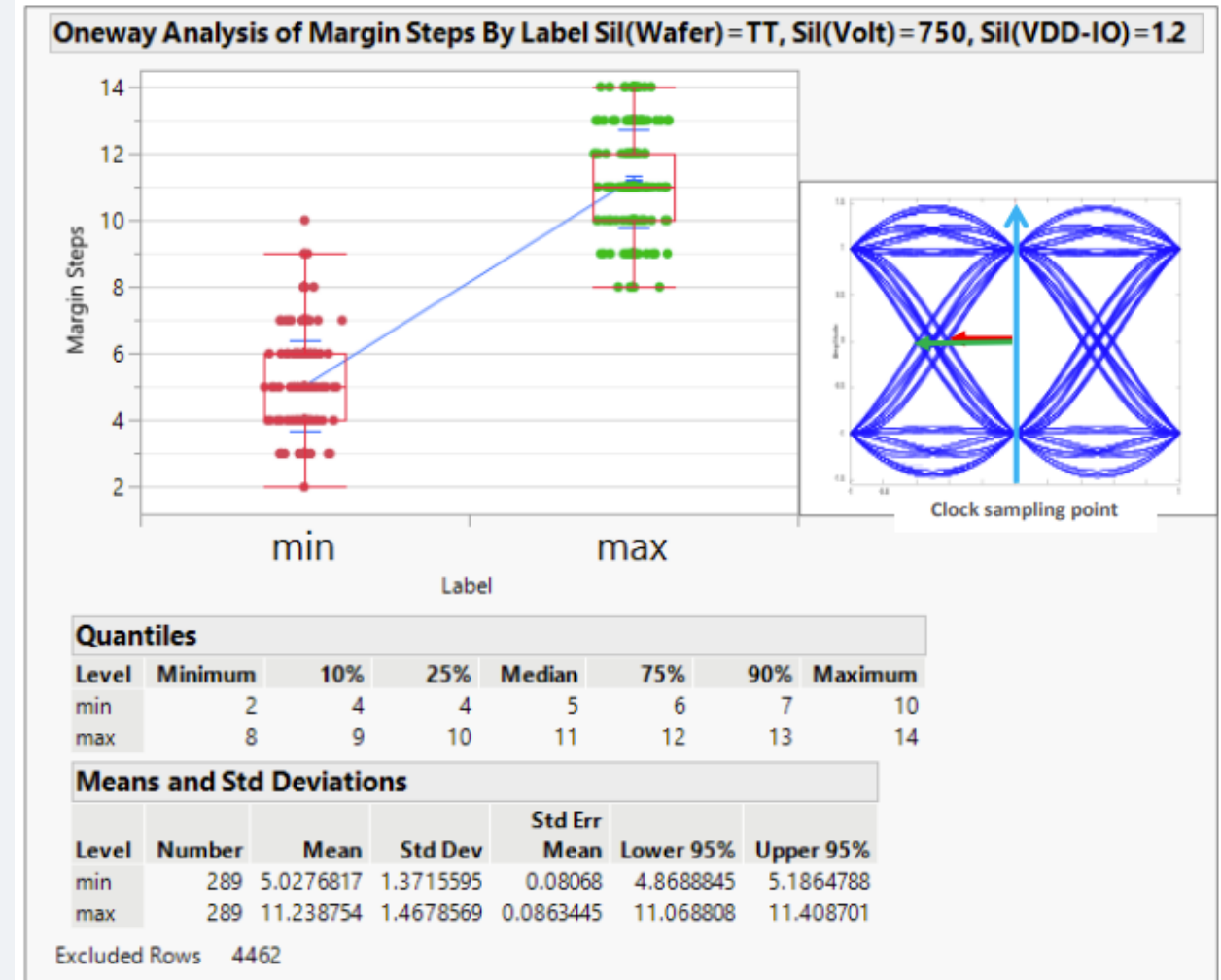
# Enhanced Characterization

At Product Introduction

- Parametric Lane Grading
  - Maximum eye width measurement (green arrow)
  - Minimum eye width measurement (red arrow)
  - Eye width crossing jitter, max-min (orange arrow)
- Per PVT (Process Voltage Temp) data visualization
- 100% pin coverage



- Full eye width and jitter characterization across PVT

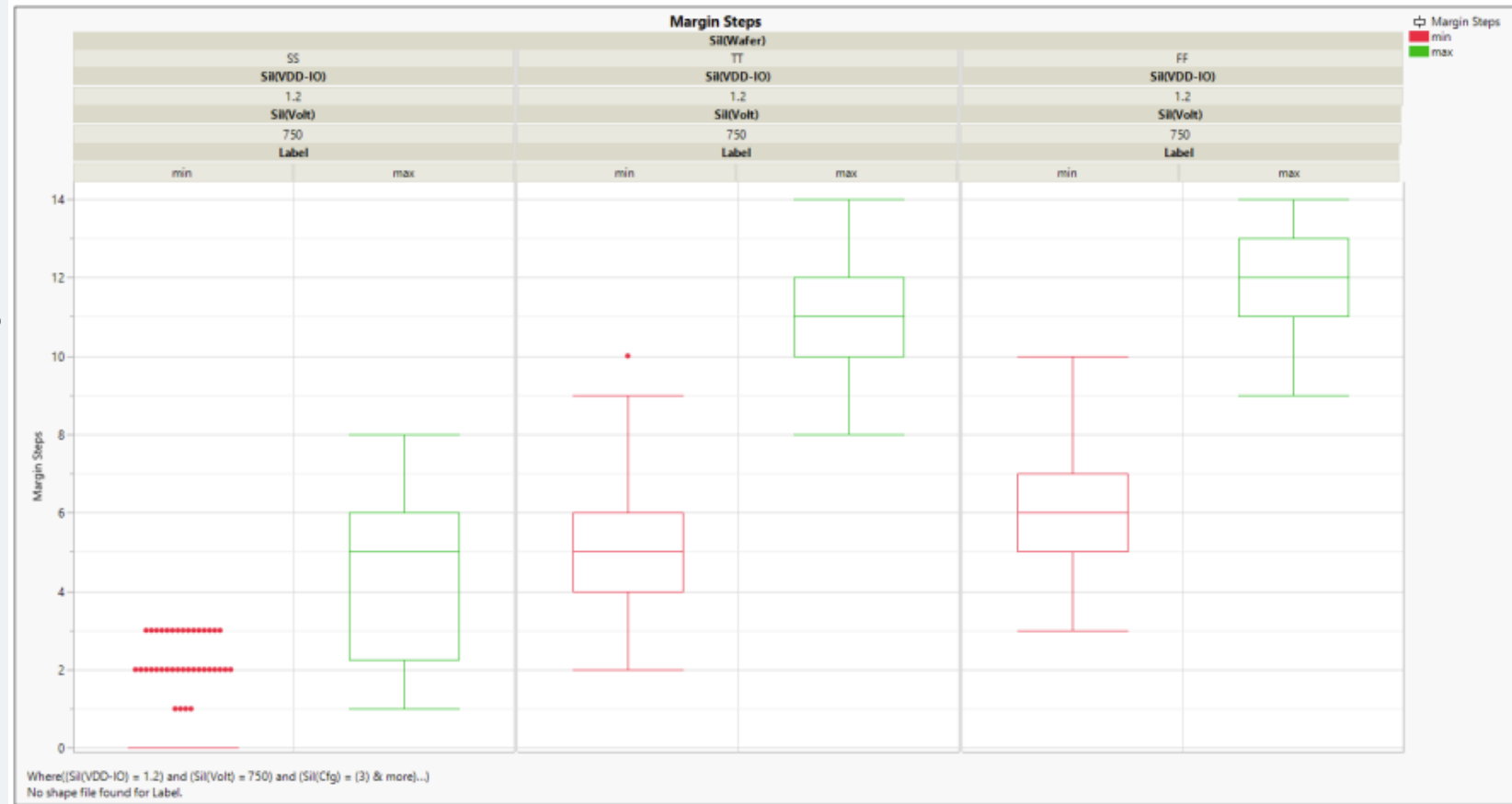


# Improved Characterization

At Product Introduction

- Samples from different process corners are analyzed
- By showing similar measurements for all samples, characterization is improved
- Enhanced with pin-point process related issues

Process corner effects on transceiver performance, per lane



# Test Optimization with Enhanced Coverage

At Product Introduction

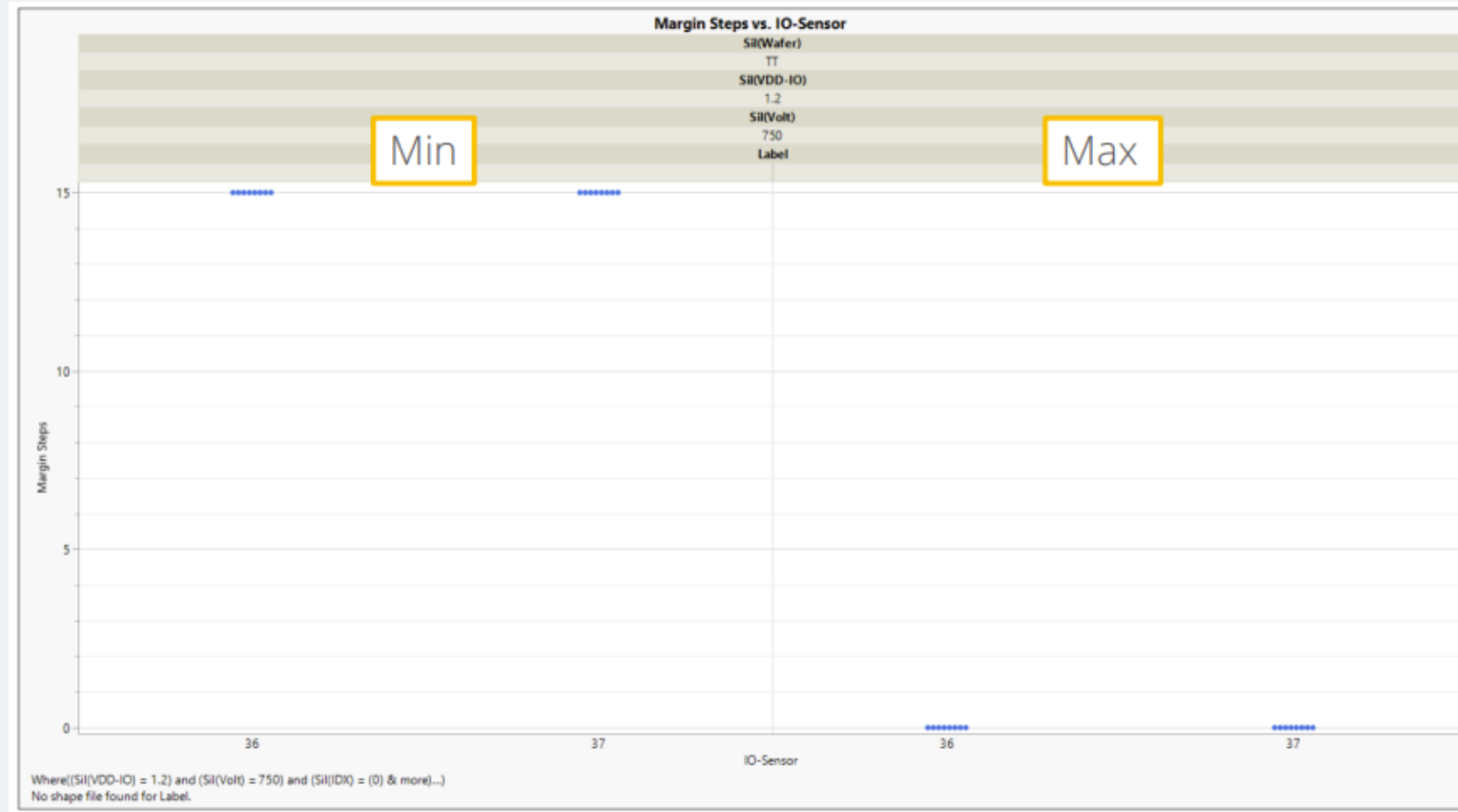
Test coverage is critical to assure all lanes are fully operational and meeting performance requirements

Figure shows:

Observation for specific pins that were not toggling (sufficiently) during test

Results:

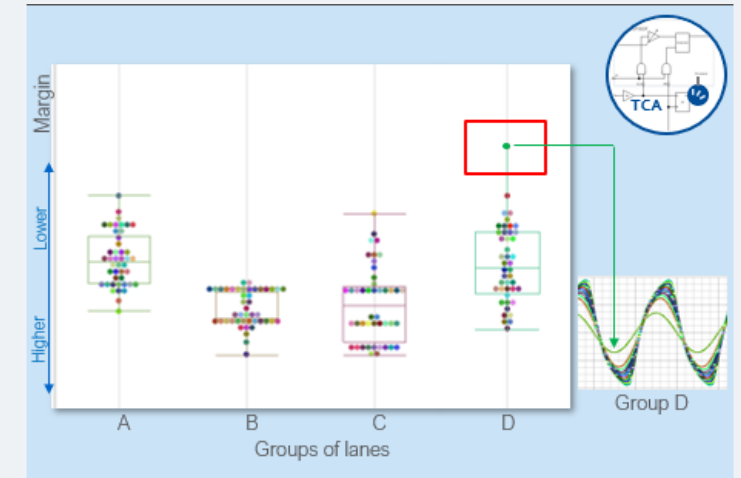
- Test coverage increased
- Test time optimized



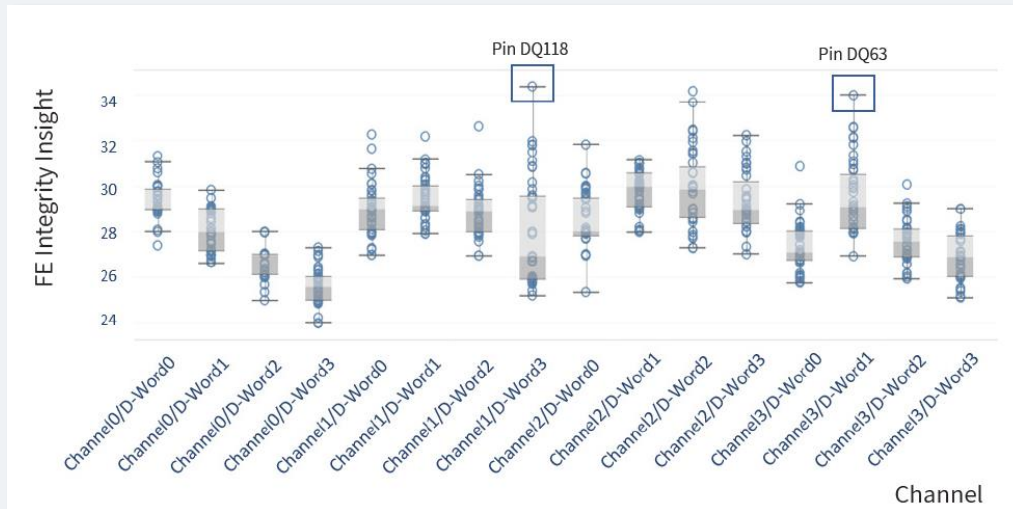
# Personalized Outlier Detection

At Volume Production

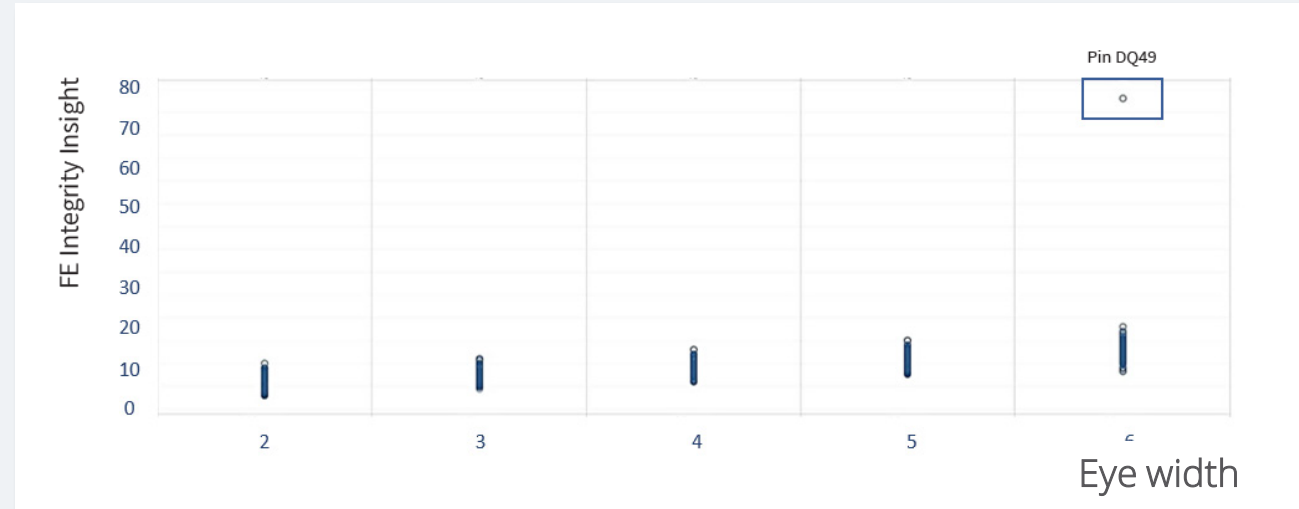
- Full population analysis
- In-line monitoring
- Real-time alert via Edge Client



Far-End Integrity Insight per Channel and Pins in Channel



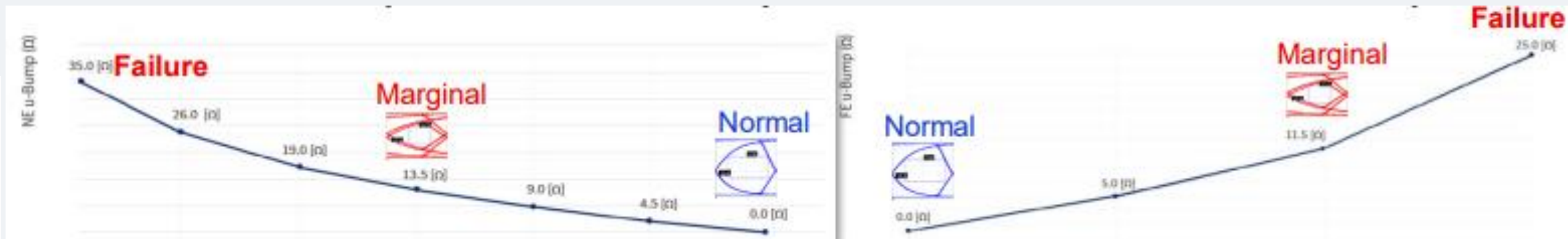
Rx Signal margin at Pin



# Performance Degradation Monitoring

In-Field

- Continuous Monitoring
- In-field and in-mission
- Issue alert to enable Predictive Maintenance



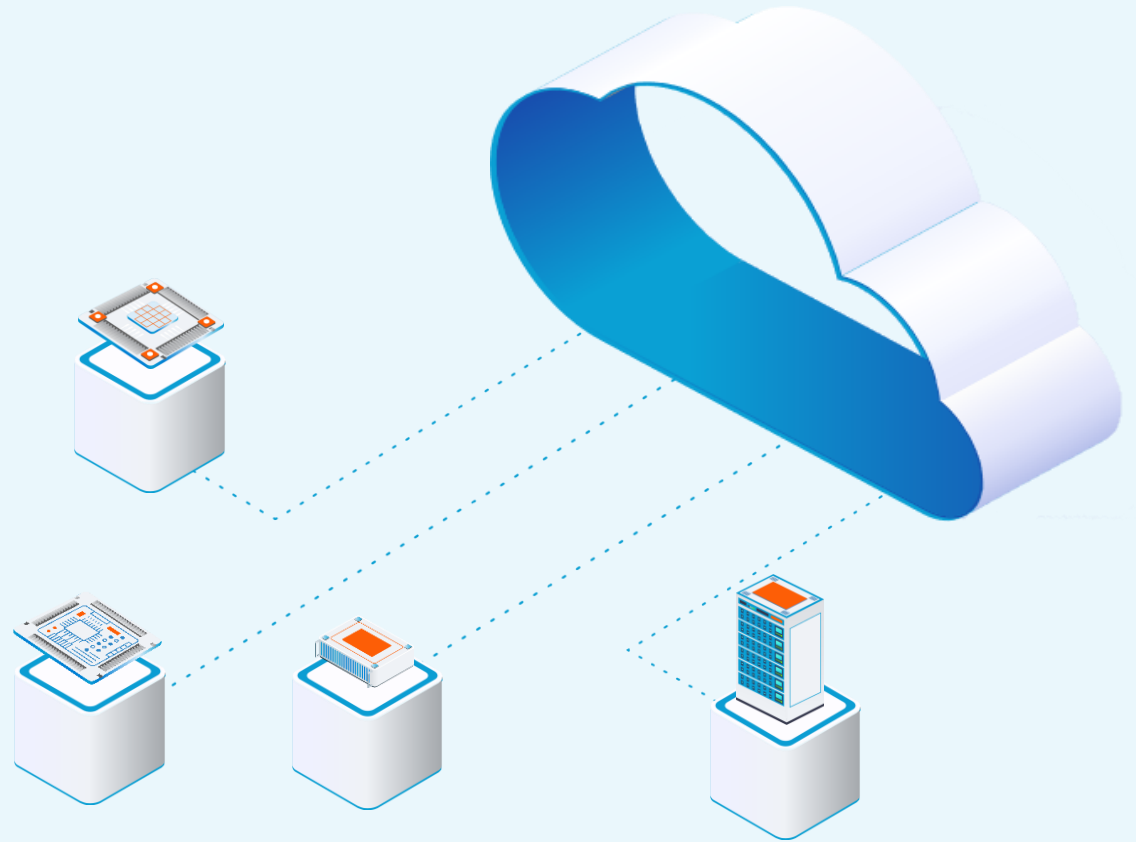
# Thank you.



[www.proteanTecs.com](http://www.proteanTecs.com)



[alex.burlak@proteanTecs.com](mailto:alex.burlak@proteanTecs.com)



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