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HETEROGENEOUS INTEGRATION ROADMAP

Dave Armstrong

Chairman – Test Technology Working Group,
Heterogeneous Integration Roadmap
Director of Business Development, Advantest

- >30 years in semiconductor test industry (HP, Agilent, Advantest)
- 9 years in semiconductor component industry (Design, Product, and Test Engineering)
- Degrees in Electrical, Computer, and Environmental Engineering from the University of Michigan

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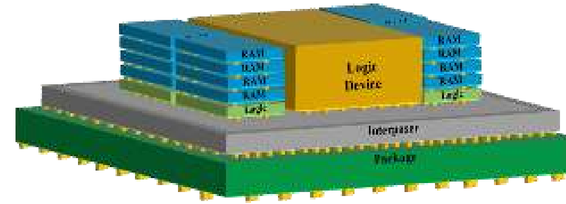
Yesterday (Circa 2018)



- Multichip integration < 10 parts
- Significant use of HBM stacks which were assumed to be "KGS".
- Wafer testing of logic part was limited. (usually not at speed or power)
- Bump size and pitch provided OK yield (but there were problems)
- Logic device was responsible for testing each HBM interface (BIST)
- DUT $$ = $\boldsymbol{f}\,(\text{Yield}_{\text{FinalTest}})$
- $\text{Yield}_{\text{FinalTest}} = \boldsymbol{f}(\text{Yield}_{\text{HighTemp}}) * \boldsymbol{f}(\text{Yield}_{\text{HighFreq}}) * \boldsymbol{f}(\text{Yield}_{\text{Contacts}})^{\#\text{Bumps}}$
- $\text{Yield}_{\text{SLT}} <$ Typically 95%-98%

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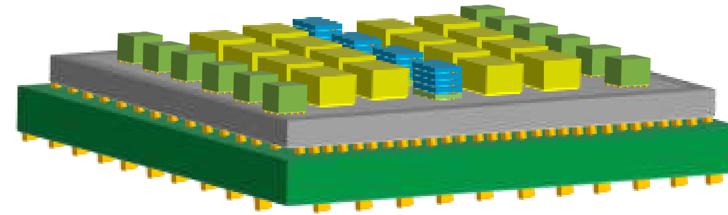
Tomorrow (Circa 2020)



- Multichip integration >> 10 parts
- Some HBM stacks – many logic devices.

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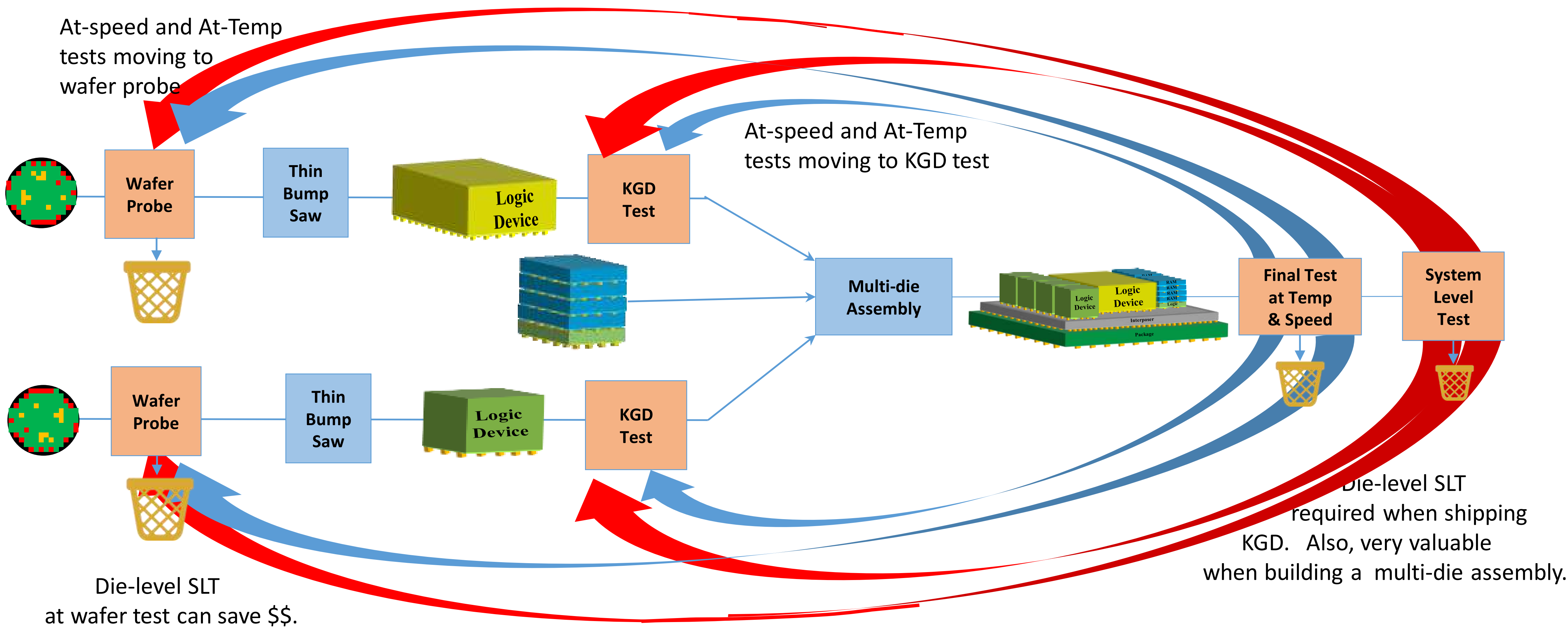
What Must we Do? ➔ Shift Left



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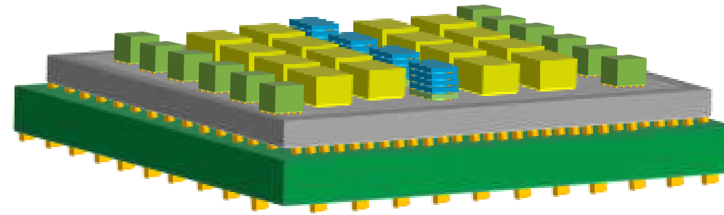
HETEROGENEOUS INTEGRATION ROADMAP

Tomorrow (Circa 2020)



- Multichip integration >> 10 parts
- Some HBM stacks – many logic devices.
- Wafer testing of logic part needs to include speed, power, & harvesting
- Bump size and pitch shrinking. # Bumps/die growing.
- KGD test becomes critical to manufacturing cost-effective assemblies.
- Die to die testing of buried interface is responsibility of logic parts (BIST)
- DUT $$ = ***f*** (Test Coverage at KGD)
- $Yield_{FinalTest} = f(1\text{-Test Coverage at KGD})^{\#Logic} * f(Yield_{Contacts})^{\#Bumps}$
- $Yield_{SLT}$ ➔ SLT will likely become final-test.

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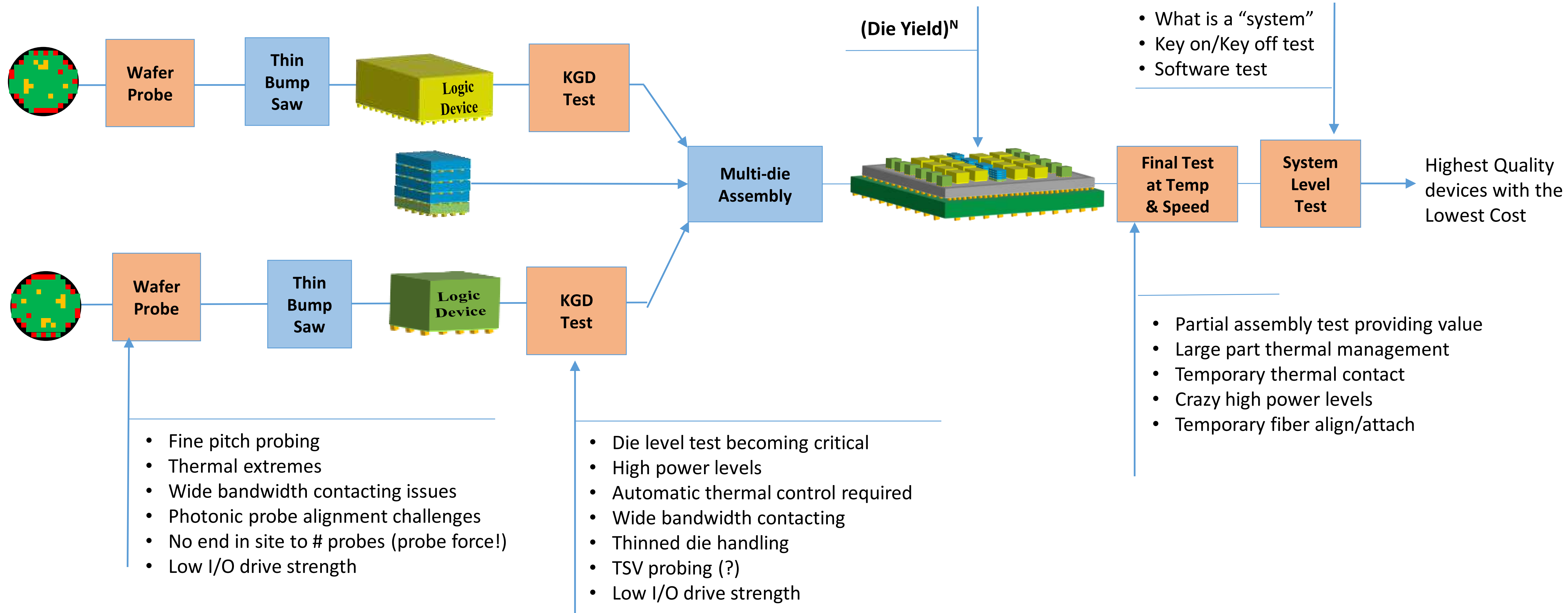
Tomorrow (circa 2020)



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