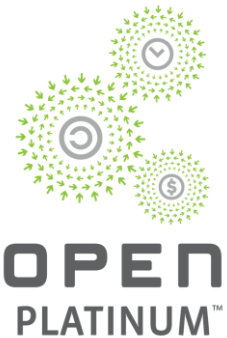
OPEN POSSIBILITIES.

DC-SCM 2.0 LVDS Tunneling Protocol & Interface (LTPI) Introduction [On Demand Virtual Session]

NOVEMBER 9-10, 2021

DC-SCM 2.0 LVDS Tunneling Protocol & Interface (LTPI) Introduction

Kasper Wszolek, Principal Engineer, Intel
Yi (Roy) Zeng, Principal Engineer, Intel



Agenda

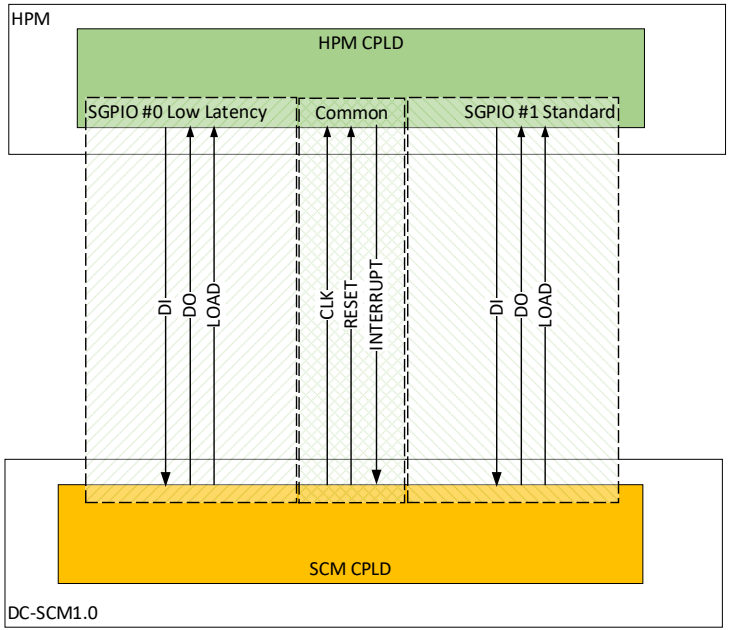
- Background
- LTPI Introduction
- Channels Concept
- Working Principle
- Frames definition
- Electrical I/O Specification
- Link training and interface bring-up
- Implementation example
- Call to Action

SERVER

Background

- DC-SCM modular designs moves substantial part of server platform on a module (BMC, Root Of Trust, Front Panel, SPI Flashes & TPM)
- DC-SCM 1.0/2.0 SFF-TA1002 4C+ connector is limited to 168 pins and cannot accommodate all low speed and high pin count interfaces
- 2 x Serial GPIO (9 pins) interfaces are defined in DC-SCM 1.0 to tunnel GPIO signals between HPM platform and DC-SCM Module

DC-SCM 1.0 Serial GPIO

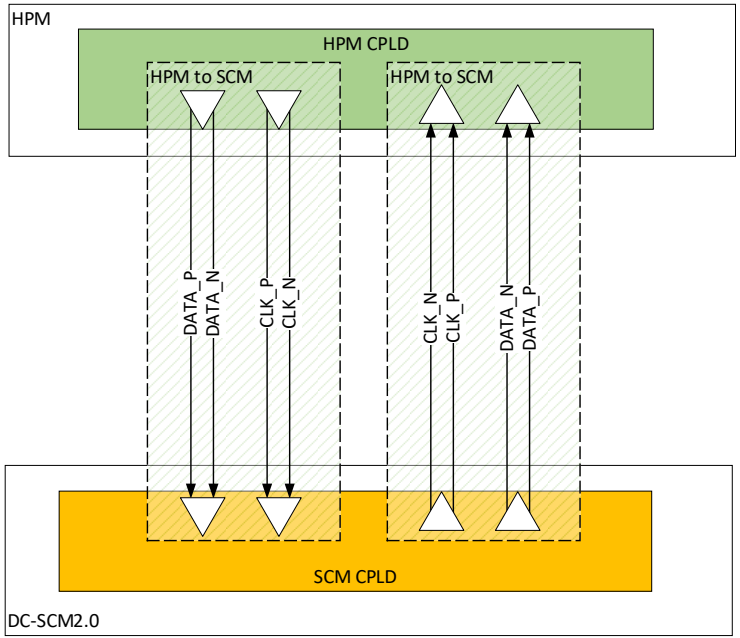


LTPI Introduction

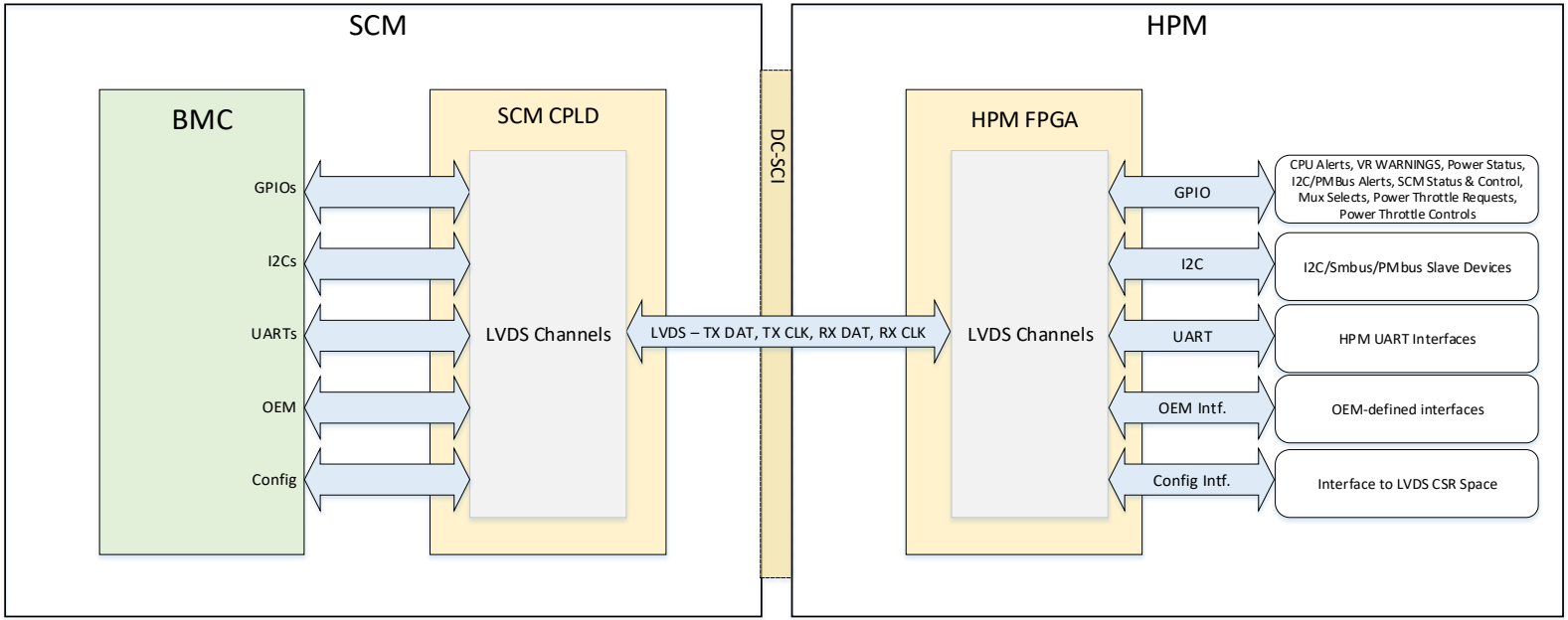
DC-SCM 2.0 LTPI:

- DC-SCM 2.0 introduces high-speed and scalable Low-voltage differential signaling Tunneling Protocol & Interface (LTPI)
- LTPI uses 4 differential links (8 pins) in place of 2 Serial GPIO interfaces from DC-SCM 1.0 and can be used to tunnel more than just GPIOs making room for DC-SCM evolution

DC-SCI 2.0 LTPI

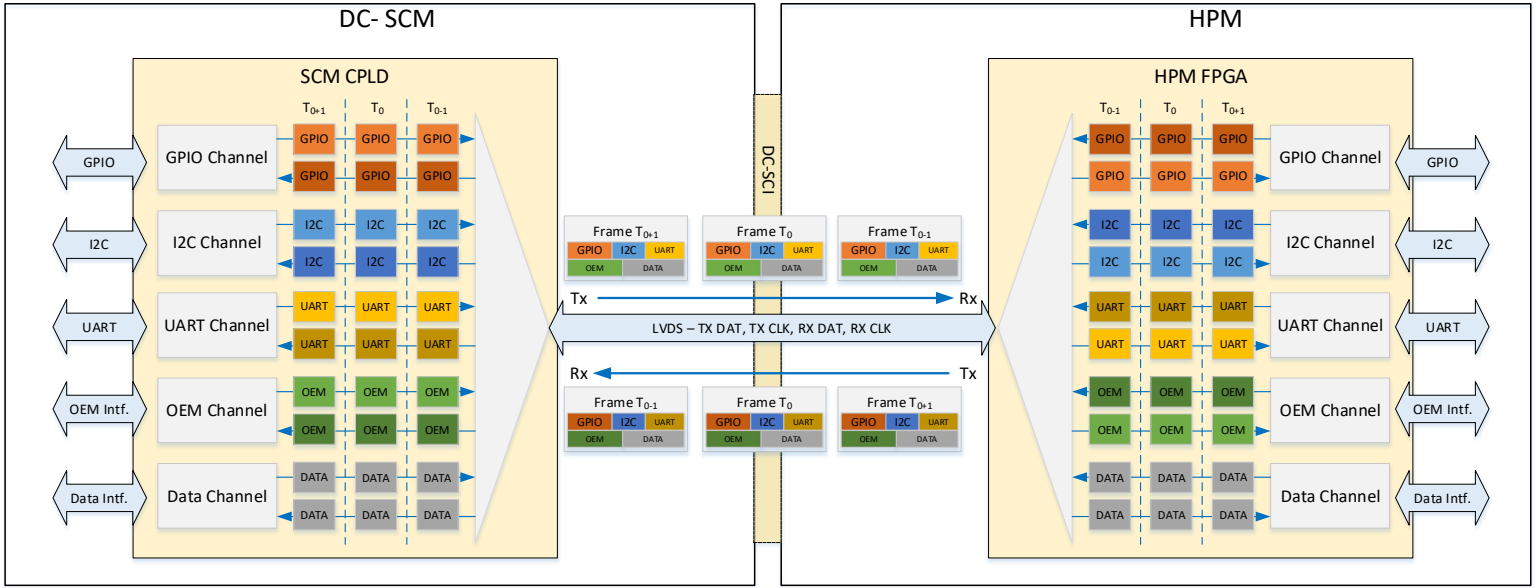


LTPI Overview



LTPI Channels

- Each channel is mapped to a physical interface that is serialized through LTPI i.e., GPIO, I2C/SMBus, UART, OEM Interfaces and Data Interfaces
- Time-Division Multiplexing (TDM) method is used to tunnel each channel through LVDS

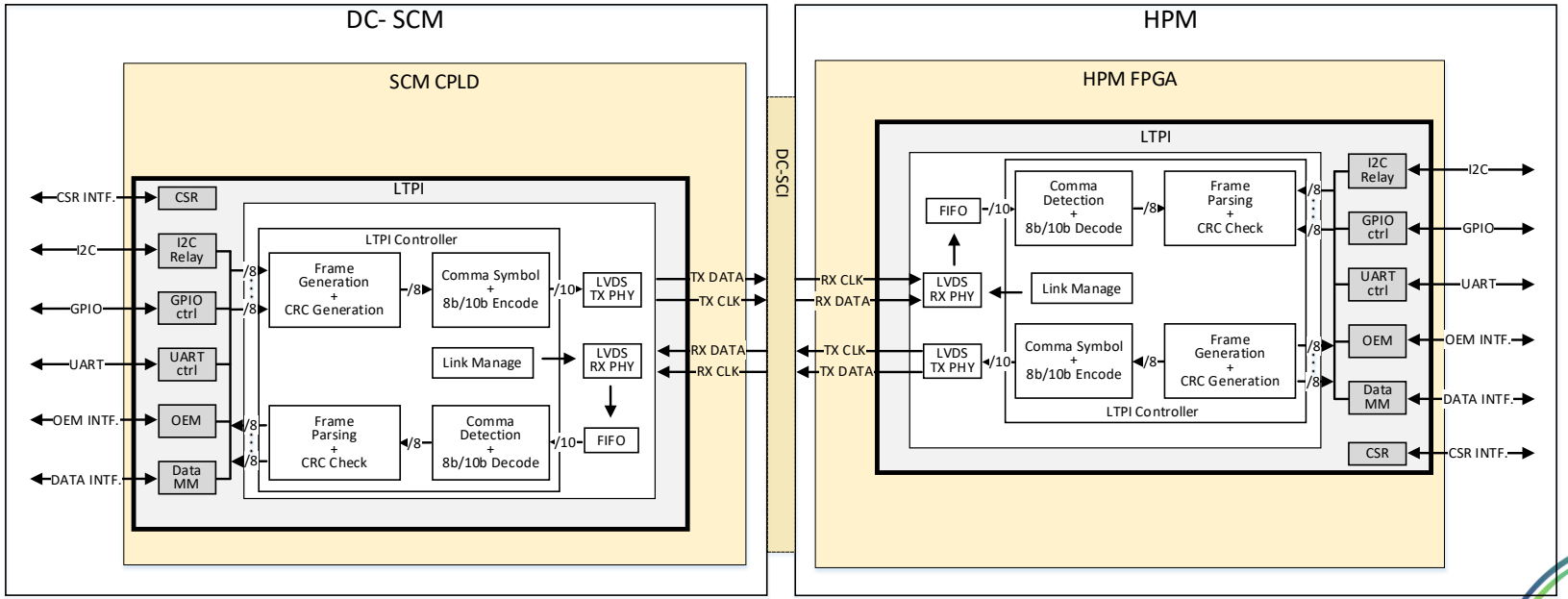


Channel	Mandatory
GPIO	Yes
I2C/SMBus	No
UART	No
Data Channel	No
OEM	No

OPEN POSSIBILITIES.

OCP GLOBAL SUMMIT
NOVEMBER 9-10, 2021

Working Principle

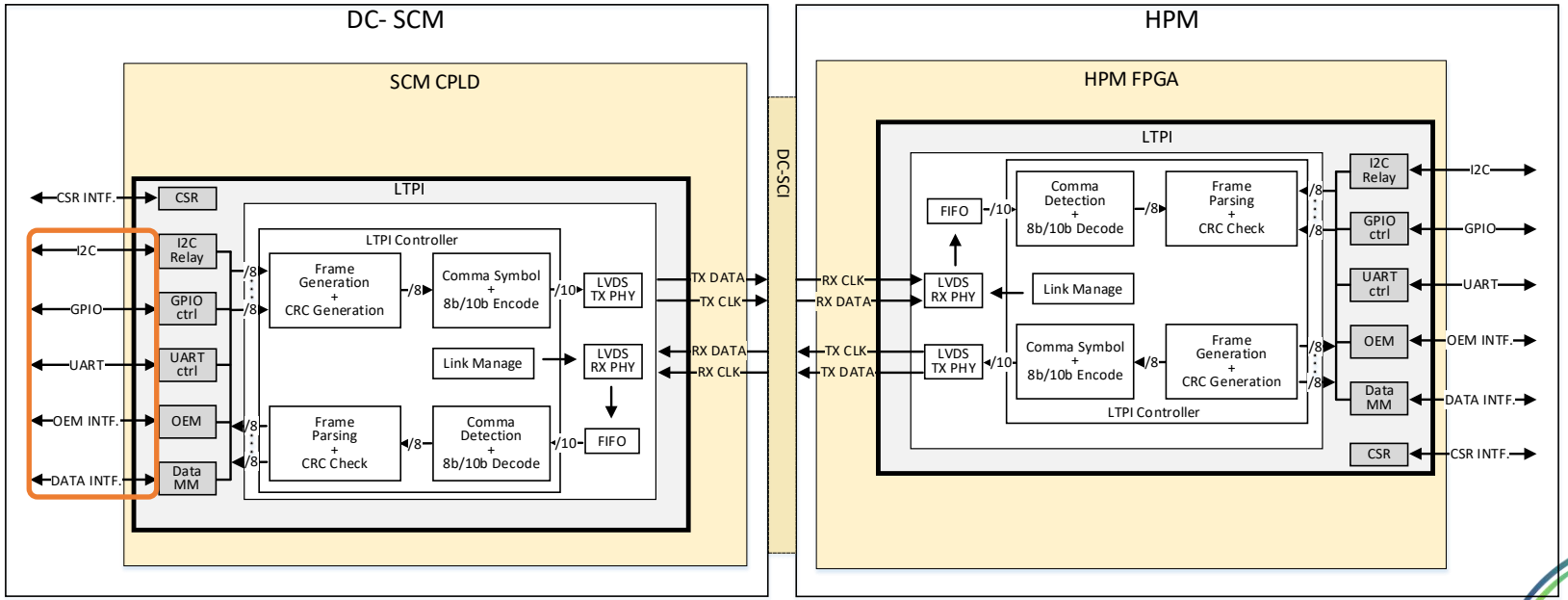


OPEN POSSIBILITIES.

OCP GLOBAL SUMMIT
NOVEMBER 9-10, 2021

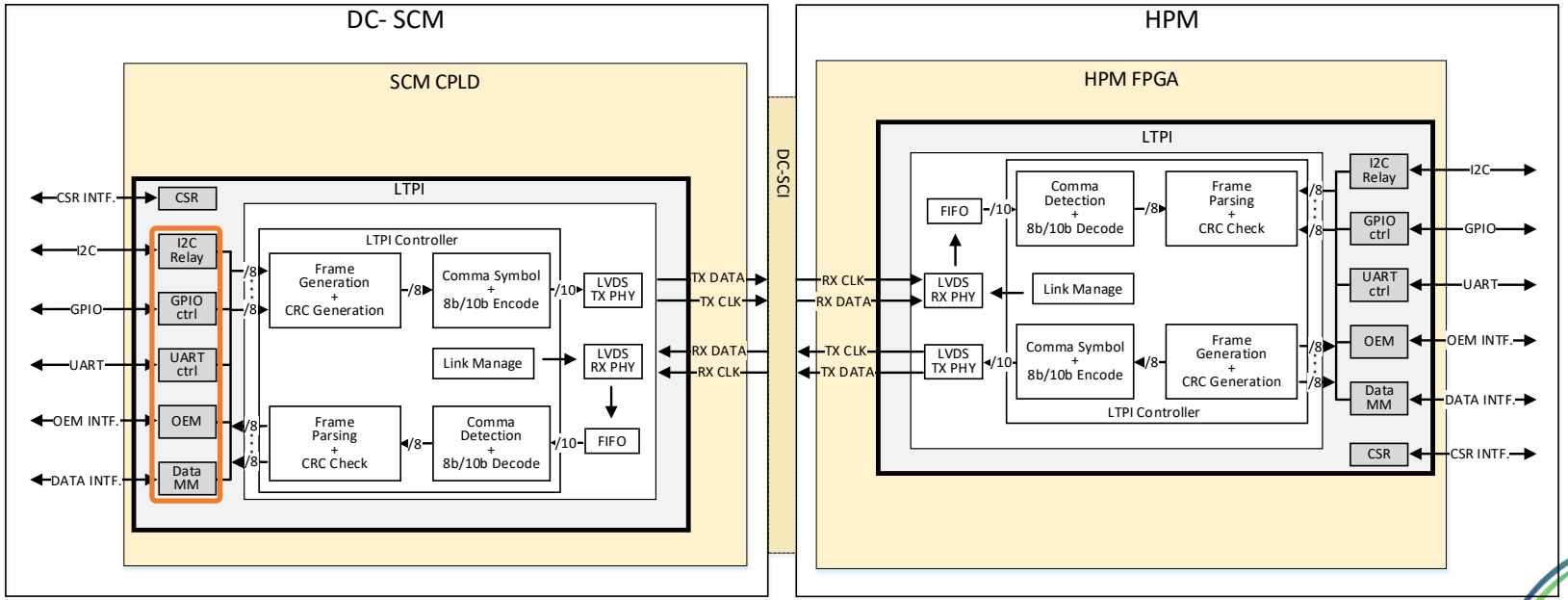
Working Principle

- Traffic on supported interfaces is generated/consumed by devices connected on DC-SCM (e.g., BMC) and HPM (e.g., CPU)



Working Principle

- LTPI captures/generates the traffic from supported interfaces through dedicated interface controllers

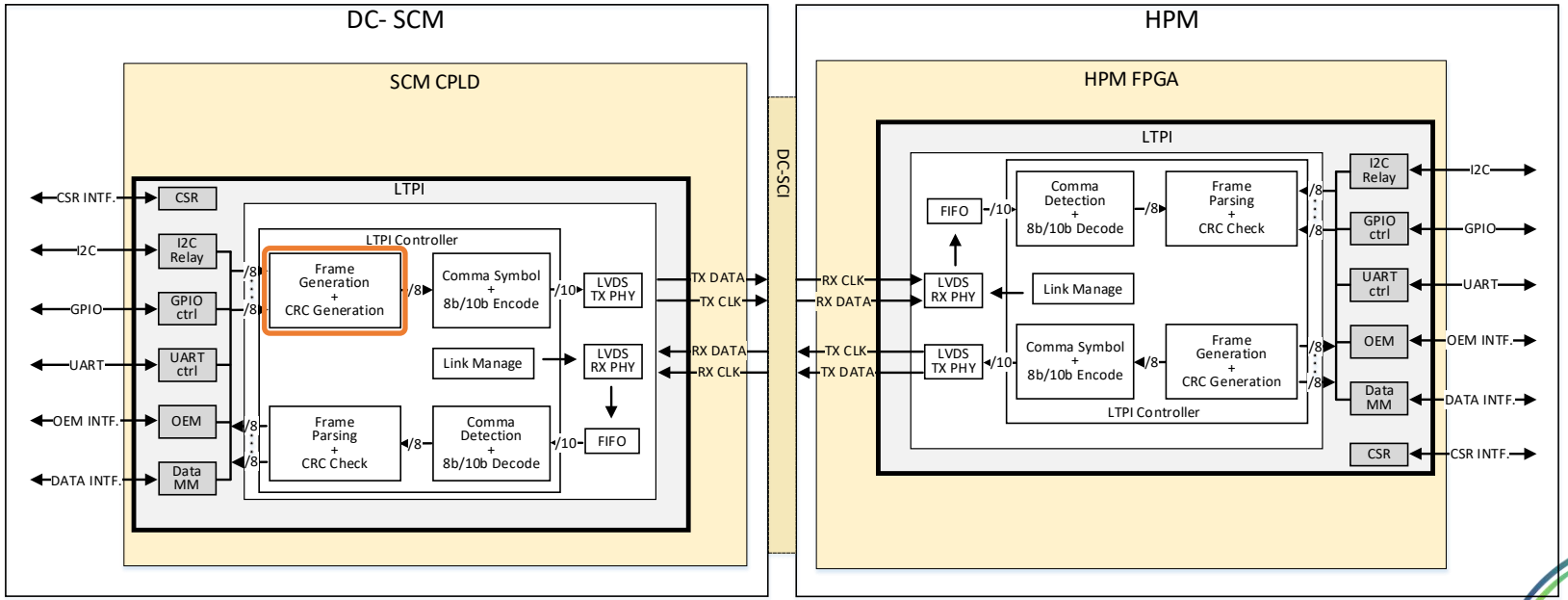


OPEN POSSIBILITIES.

OCP GLOBAL SUMMIT
NOVEMBER 9-10, 2021

Working Principle

- LTPI Controller generates a frame with each interface state encoded on bits dedicated for given channel

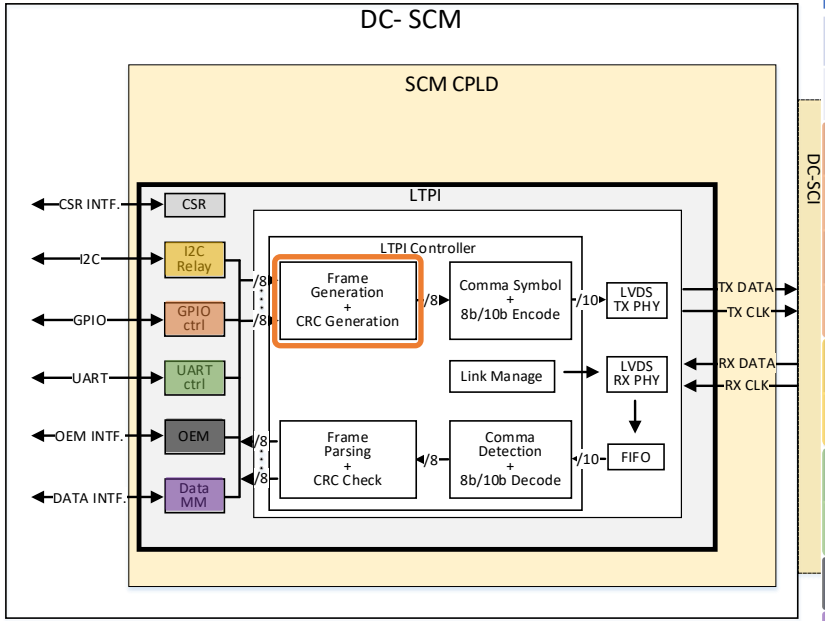


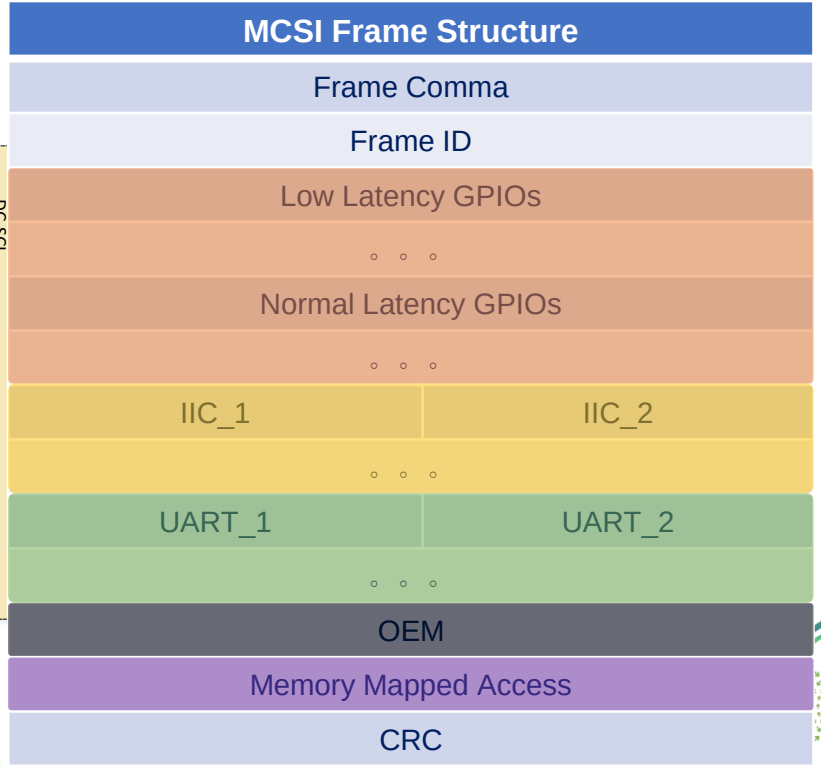
OPEN POSSIBILITIES.

OCP GLOBAL SUMMIT
NOVEMBER 9-10, 2021

Working Principle

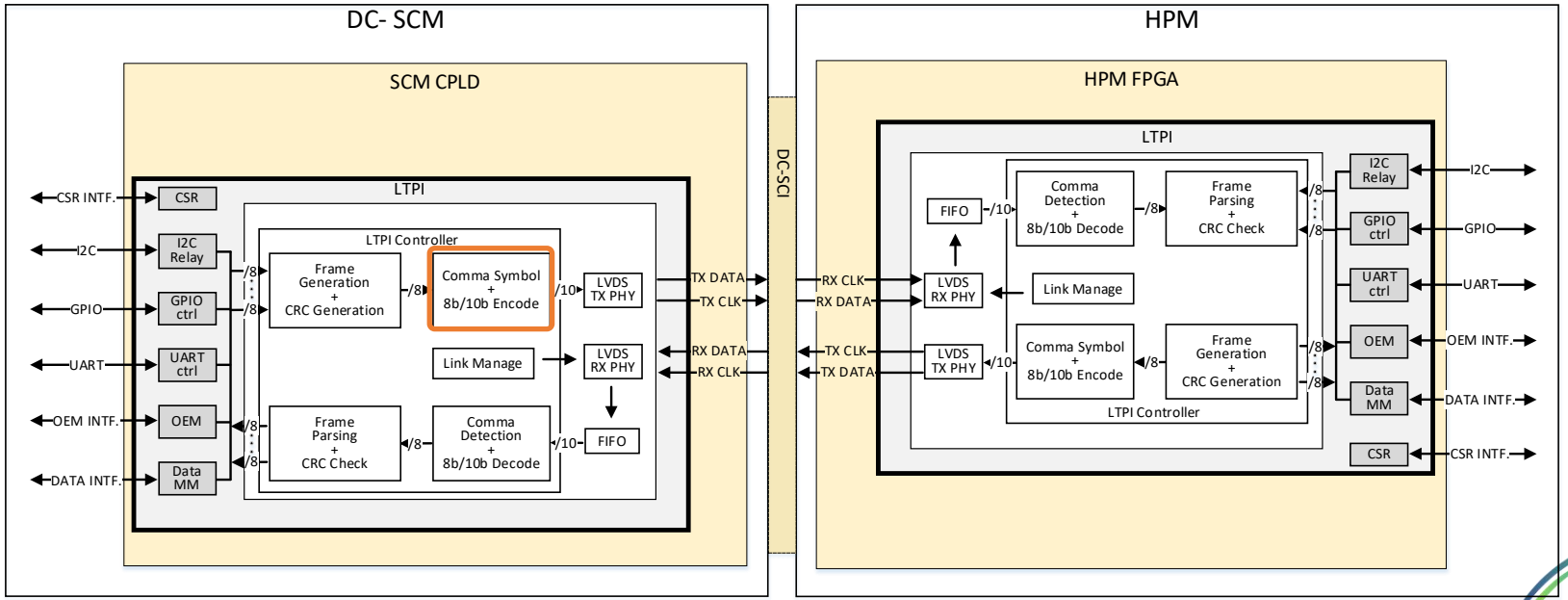
- Each channel is encoded on predefined bits within LTPI Frame





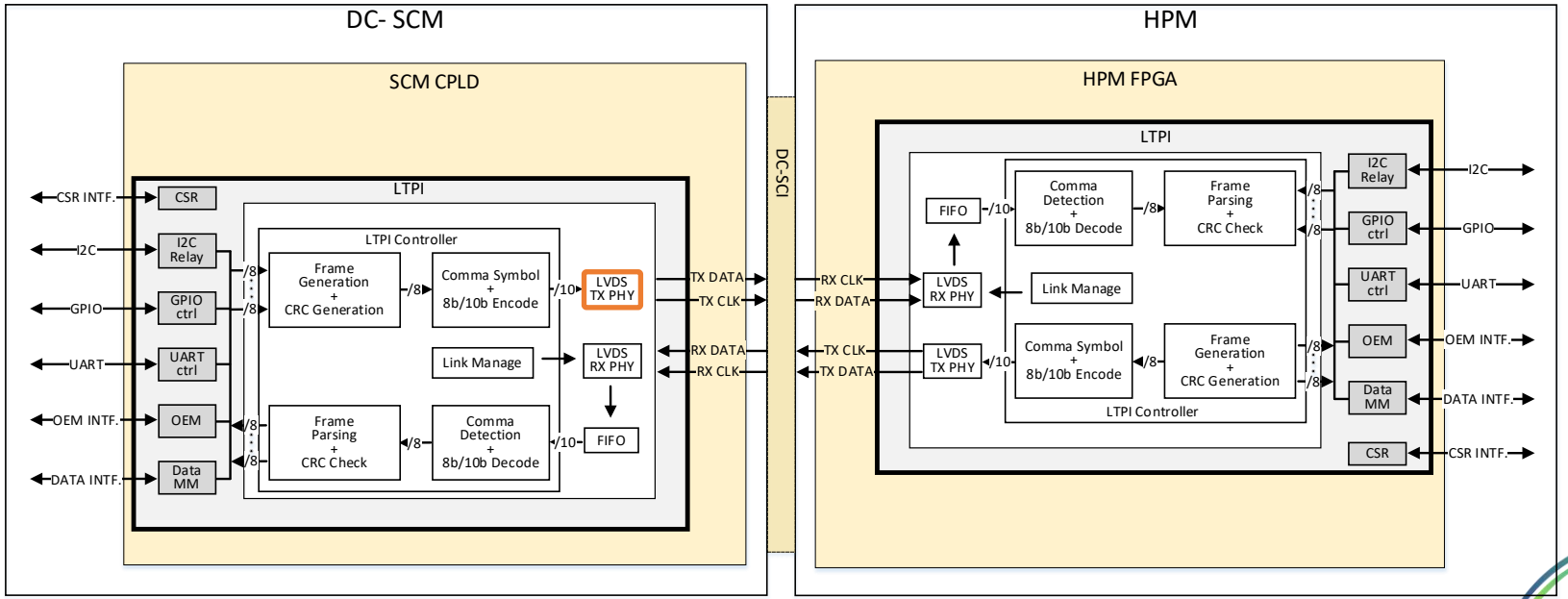
Working Principle

- The LTPI Frame is encoded using 10b encoding and Comma Symbol is added to the frame



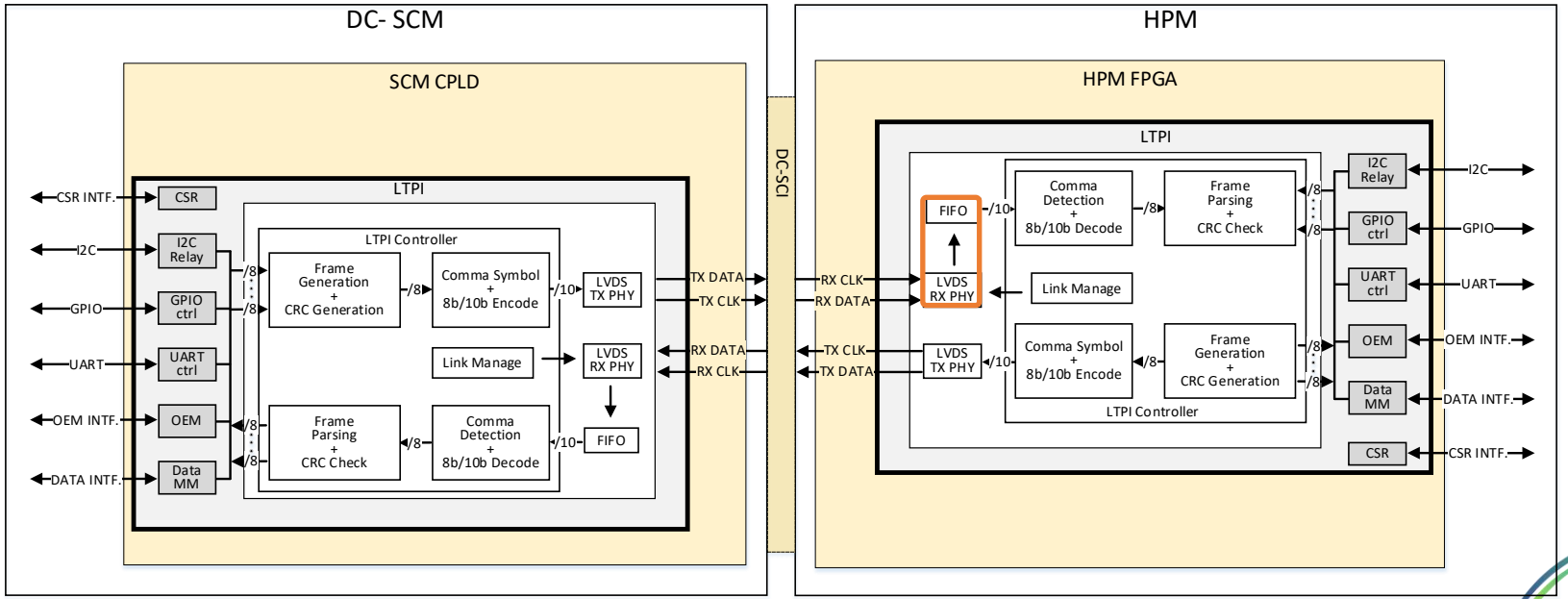
Working Principle

- The frame is serialized through LVDS link with dedicated synchronized clock



Working Principle

- On RX side the LVDS PHY is used to capture the frame from LVDS serial link

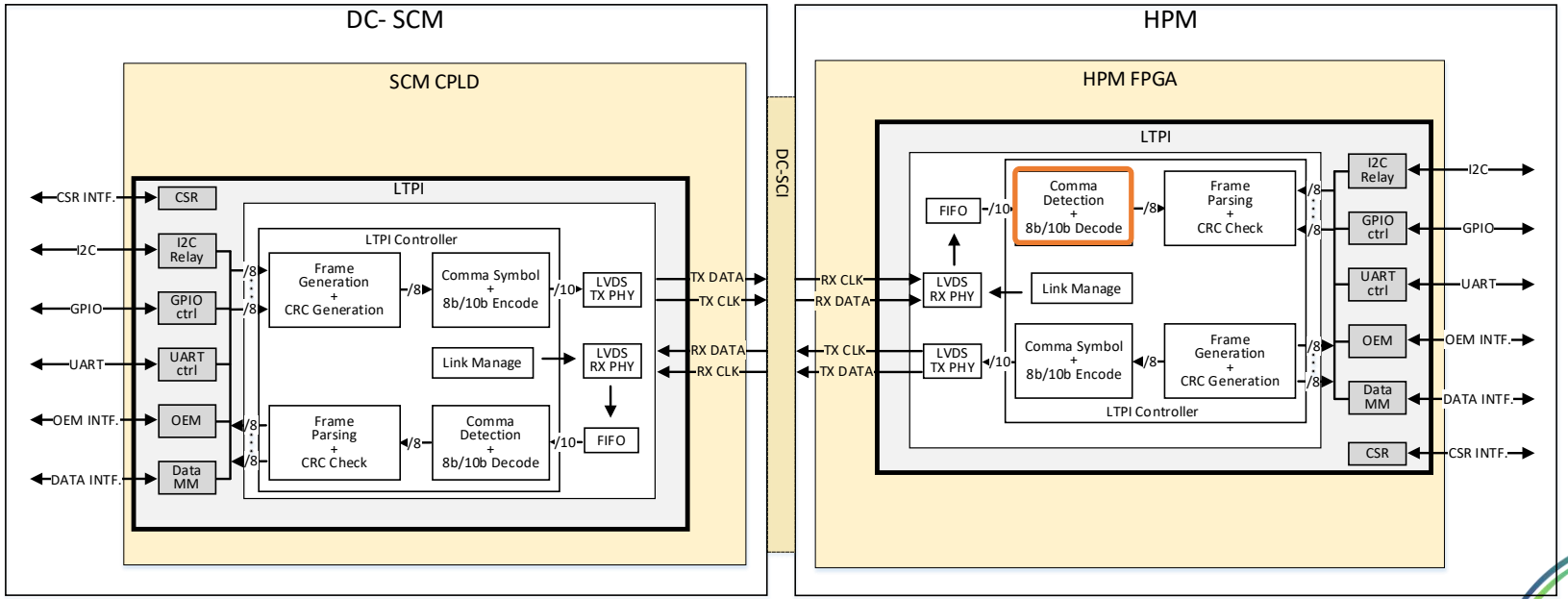


OPEN POSSIBILITIES.

OCP GLOBAL SUMMIT
NOVEMBER 9-10, 2021

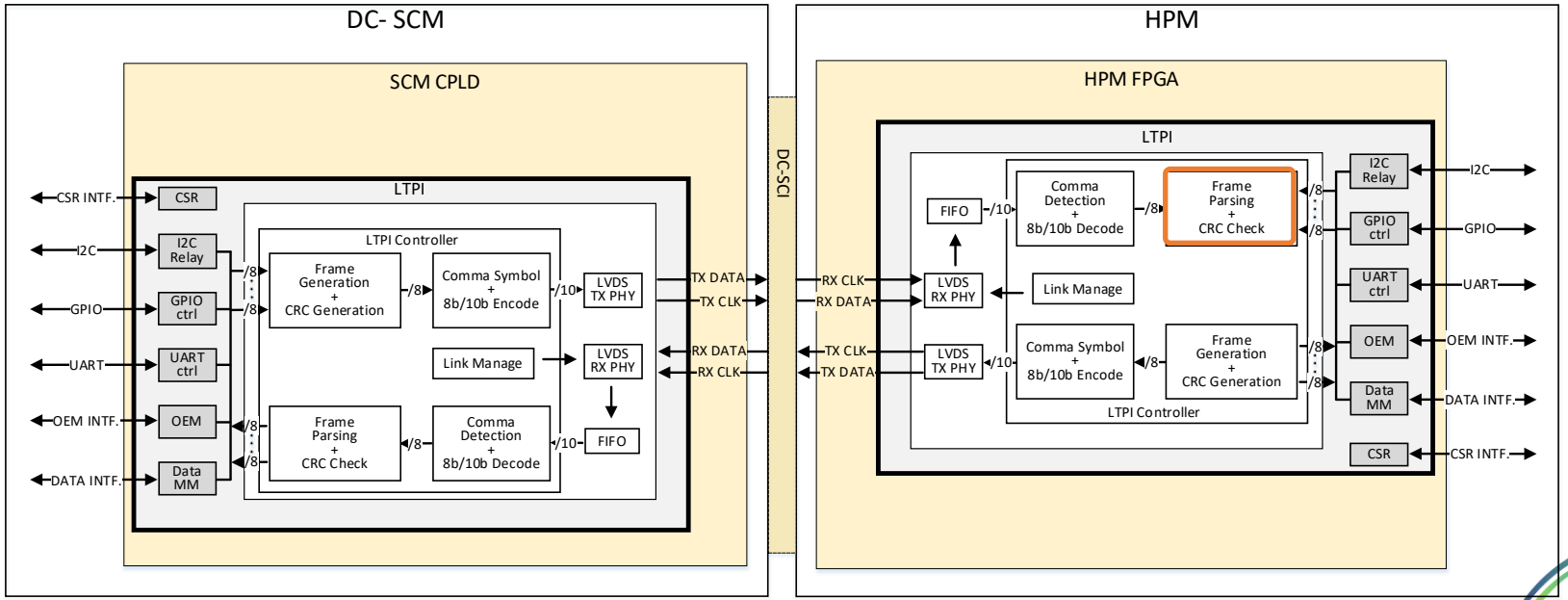
Working Principle

- Frame is detected based on Comm Symbol and deserialized



Working Principle

- Frame is validated against CRC and decomposed into channels

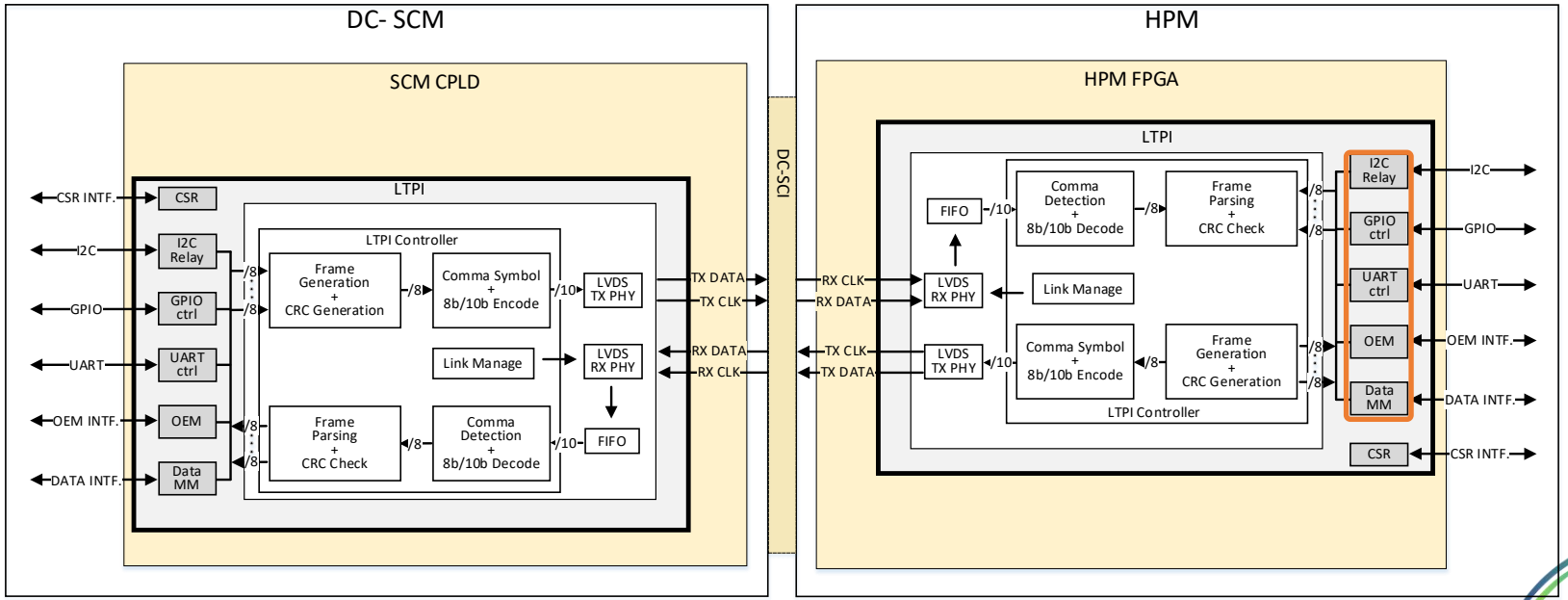


OPEN POSSIBILITIES.

OCP GLOBAL SUMMIT
NOVEMBER 9-10, 2021

Working Principle

- Respective channel states are passed to interface controllers

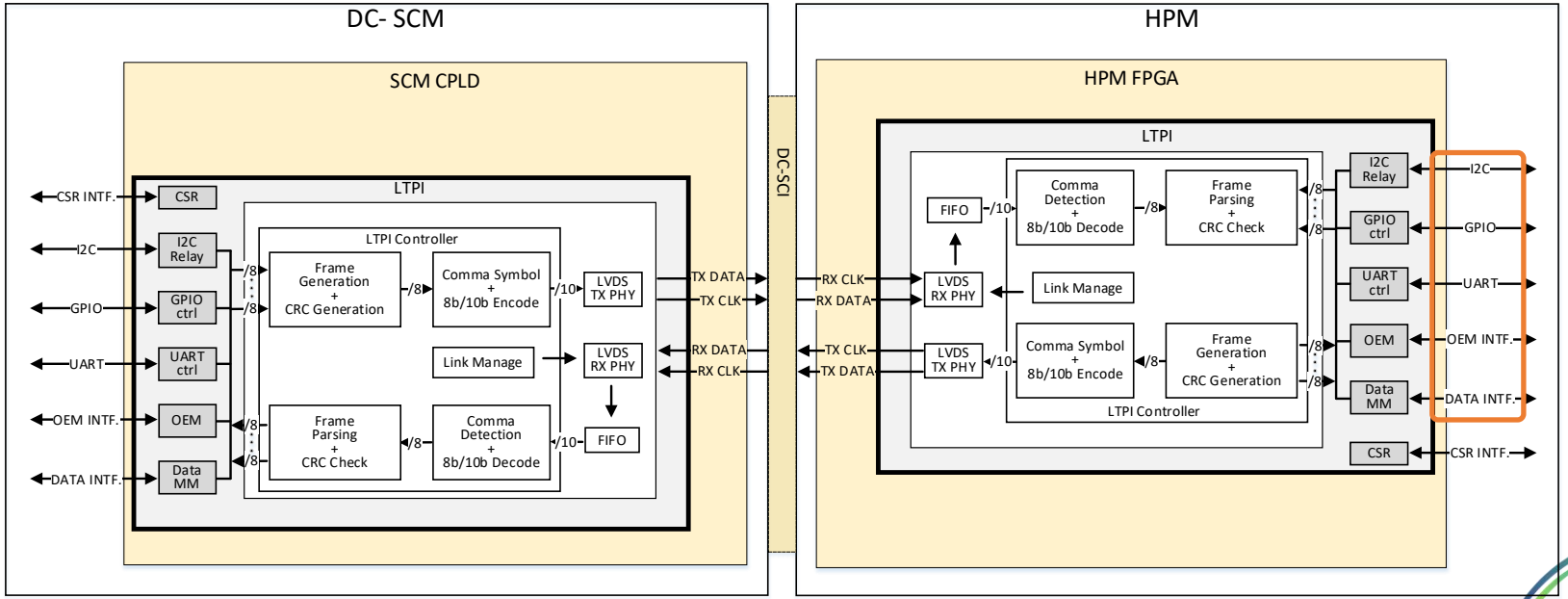


OPEN POSSIBILITIES.

OCP GLOBAL SUMMIT
NOVEMBER 9-10, 2021

Working Principle

- Traffic is re-generated on supported interfaces connected to physical devices e.g. CPU or BMC

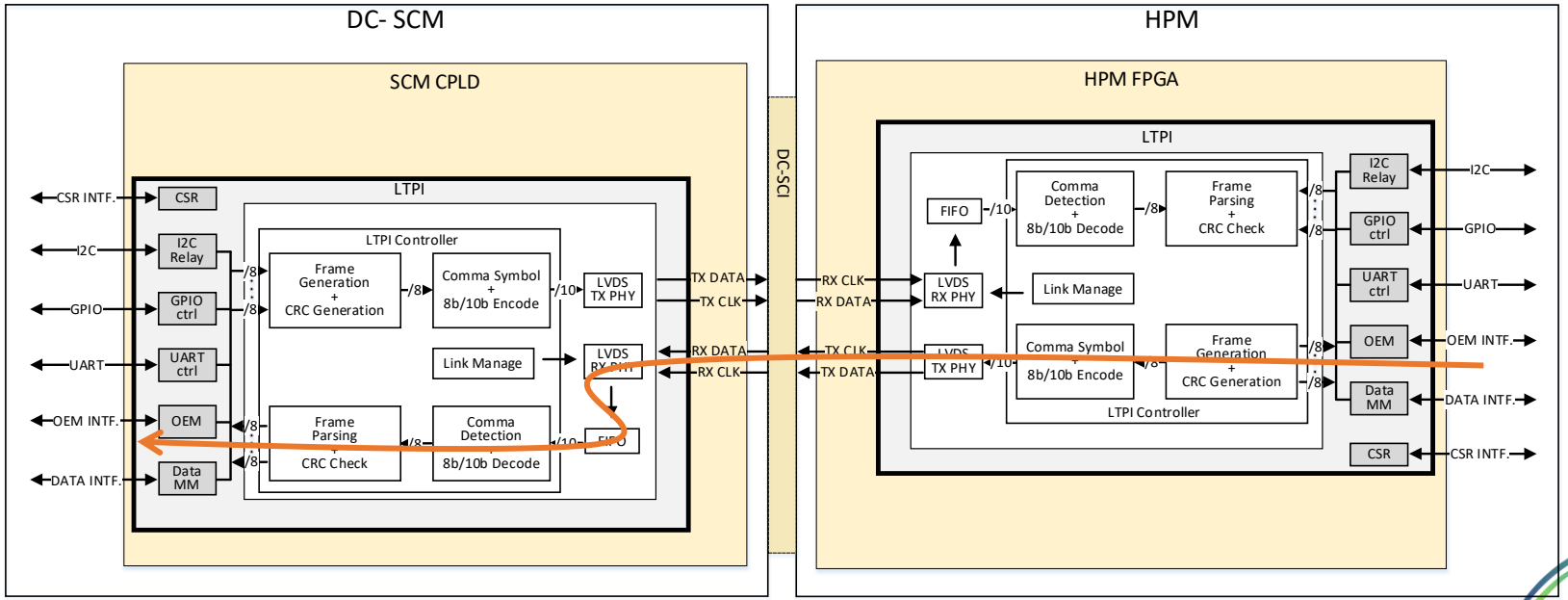


OPEN POSSIBILITIES.

OCP GLOBAL SUMMIT
NOVEMBER 9-10, 2021

Working Principle

- The other direction from HPM to DC-SCM follows exactly same principle



LTPI frames definition

LTPI Frames are fixed size frames

- Default size is 160 bits : 16 symbols x 10bits

Sequence	Symbol
0	Comma Symbol
1	Frame Payload
2	Frame Payload
⋮	⋮
14	Frame Payload
15	CRC

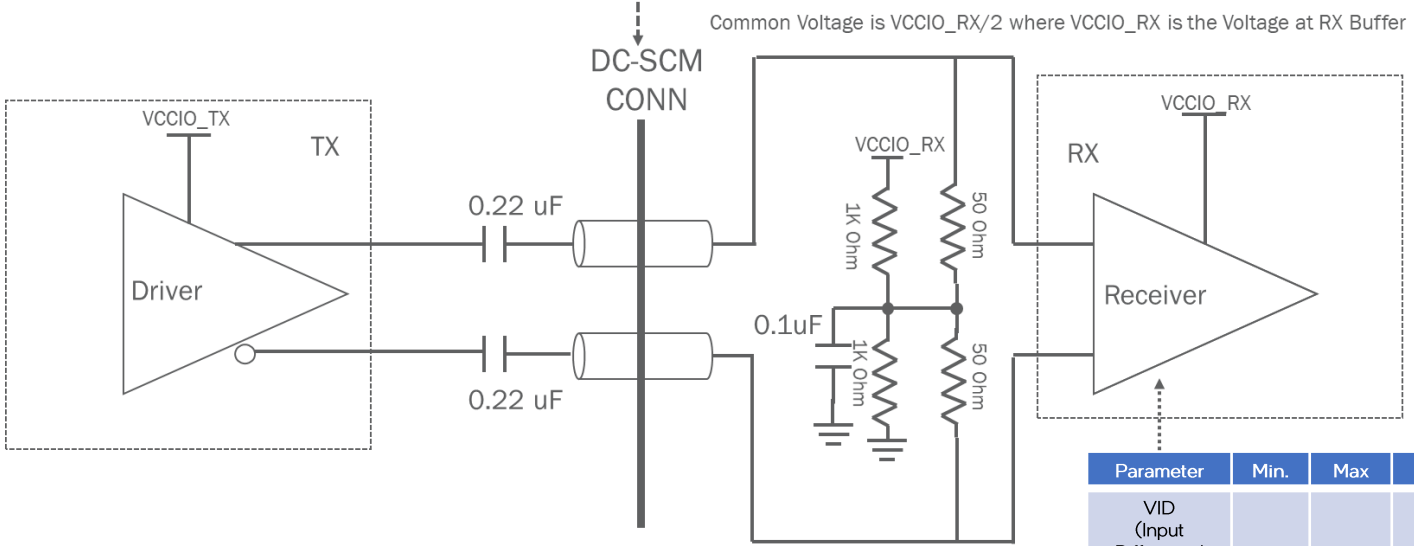
LTPI Frames Types are identified by different Comma Symbols:

Comma Symbol	Frame Type	Description
Comma Symbol 1	Link Detect and Speed Selection	Initial frame transmitted during LTPI bring-up flow to provide information about supported LTPI speed capabilities. Frame is also used to achieve DC balance on the link and select target link speed.
Comma Symbol 2	Capabilities Advertise and Configure/Accept	Frame is used to advertise supported capabilities (Channels and features supported by LTPI) and configure enabled capabilities supported by DC-SCM and HPM LTPI endpoints.
Comma Symbol 3	LTPI Operational Frame	Frame use during normal LTPI operation after interface initialization and configuration is completed. Frame carries all the channels supported by given LTPI implementation.

Electrical I/O Specification

Measured at DC-SCM CONN Side

Parameter	Minimum	Max	Unit
Vod (Differential Voltage Swing)	100	800	mV

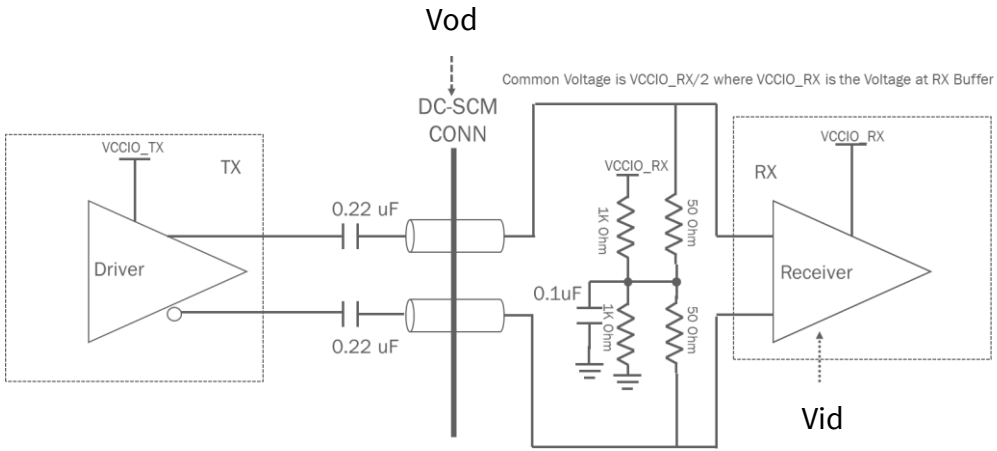


Parameter	Min.	Max	Unit
VID (Input Differential Voltage Swing)	100	800	mV

Electrical I/O – LVDS Standards

Typical Common Voltage and Vod/Vid for various LVDS Standards

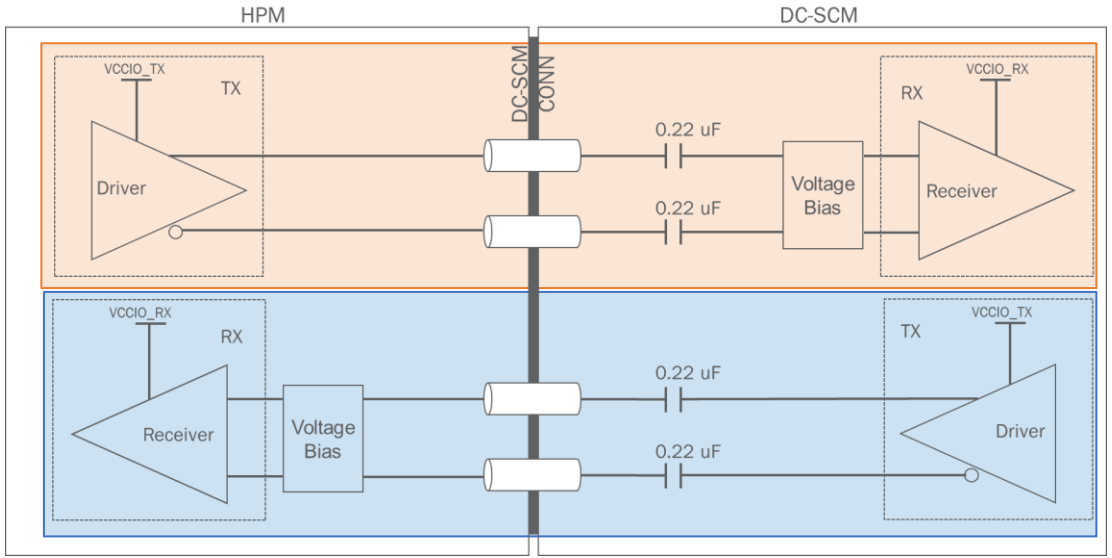
VCCIO TX \ VCCIO RX	3.3V		2.5V (LVDS)		1.8V (Sub-LVDS)	
3.3V	Common Voltage 1.65V	Vod 350mV Vid 350mV	Common Voltage 1.25V	Vod 350mV Vid 350mV	Common Voltage 0.9V	Vod 350mV Vid 150mV
2.5V (True LVDS)		Vod 350mV Vid 350mV		Vod 350mV Vid 350mV		Vod 350mV Vid 150mV
2.5V (Emulated LVDS)		Vod 500mV Vid 350mV		Vod 500mV Vid 350mV		Vod 500mV Vid 150mV
1.8V (True Sub-LVDS)		Vod 150mV Vid 350mV		Vod 150mV Vid 350mV		Vod 150mV Vid 150mV
1.8V (Emulated Sub-LVDS)		Vod 150mV Vid 350mV		Vod 150mV Vid 350mV		Vod 150mV Vid 150mV



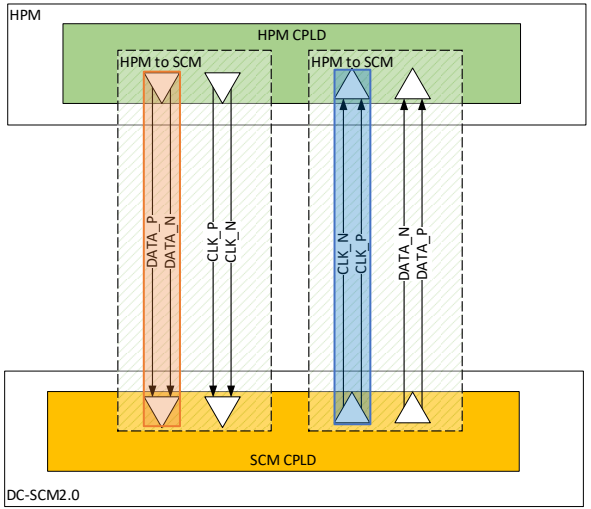
LVDS I/O Voltage Swing Requirements

Parameter	Minimum	Max	Unit
Vod/Vid (Differential Voltage Swing)	100	800	mV

Electrical I/O Interoperability

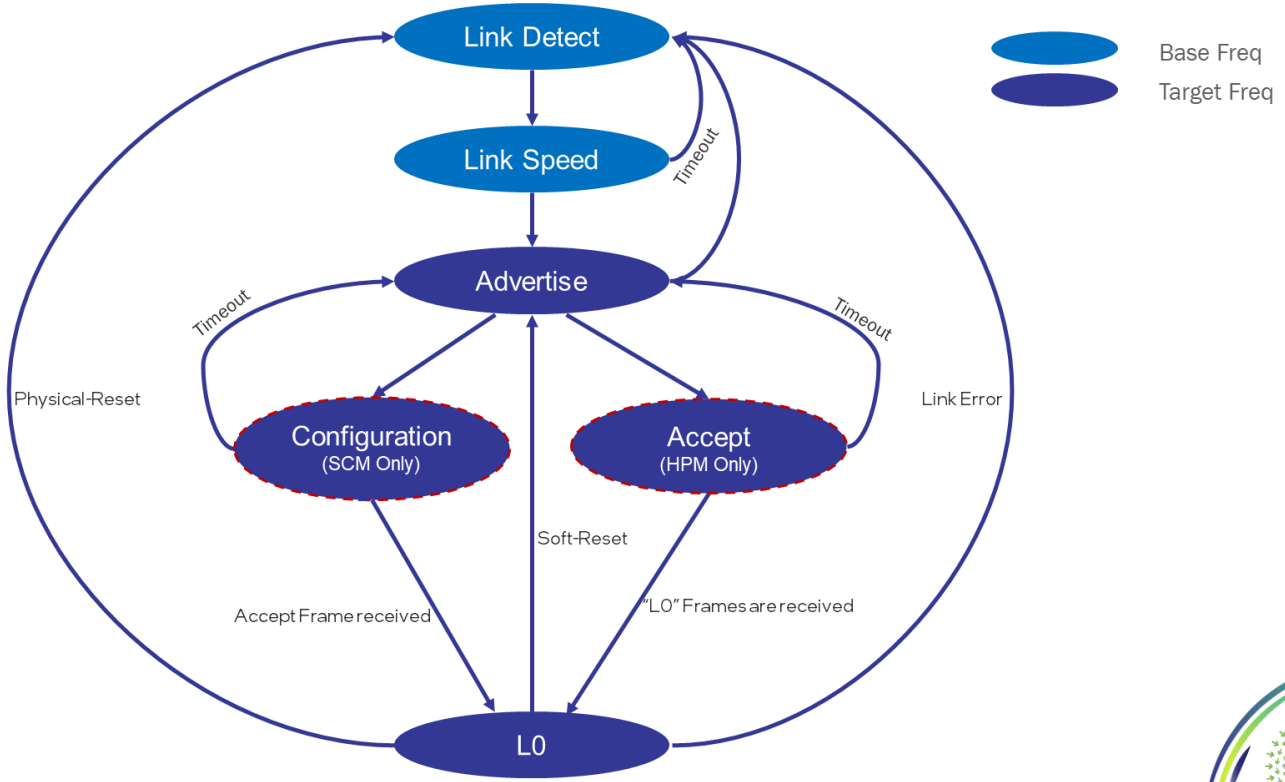


DC-SCI 2.0 LTPI



Parameter	Value
DC Blocking Capacity	0.22 uF
LVDS PCB Impedance	85 Ohm
LVDS Termination Resistor	100 Ohm
DC Blocking Caps Placement	DC-SCM Module

Link training and interface bring-up



Implementation example

Summary

Device	LVDS Link Speed	Normal Latency GPIOs	Low Latency GPIOs	I2C Links 400kHz	UART Links 115200	Data Channels
Intel MAX10 10M25 CPLD	200 MHz	112	4	4	2	0

Latency/Bandwidth

Normal Latency GPIOs	Low Latency GPIOs	I2C Links	UART Links	Data Channels
~9.4us	~1.3us	185 kHz	115200	N/A

Resource utilization

Parameter	Utilization	Percentage
Total Logic Elements	~2,200	~8.8%
PLL	2	50%

GPIOs/UARTs	~1,000
I2C	~1,200 (300 LE per link)

Key features Re-cap

Key Features	Benefits and Value Add
LVDS I/O (Low-Voltage Differential Signaling)	- Improved Signal Integrity and Bandwidth comparing to Single-ended - Supported by most of CPLD & FPGA
AC-coupling	- Allows for multiple LVDS voltage standard use - Improved CPLD/FPGA interoperability
Multiple interfaces tunneling	- Supports tunneling of more interfaces than just GPIO: SMBus/I2C, UART, Data Channel
High bandwidth capabilities	- Reference designs running at 200Mbps - Latest FPGAs support LVDS at 1600 Mbps
Scalability & Flexibility	- Specific designs can choose which interfaces are tunneled with LTPI - OEM Extensions can be added to LTPI as OEM channels - Data Channel allows for random access and data exchange between DC-SCM CPLD and HPM CPLD
Interoperability	- Link training and capabilities exchange protocol defined - BMC controls the process of LTPI bring-up and configuration

Call to Action

- Join us in Experience Center to see the Live Demo of LTPI interface:
  - Intel Demo of LTPI Implementation on Intel Max10 CPLDs
  - Lattice Demo of LTPI Implementation on Lattice MachXO3 FPGAs
- Provide feedback to OCP HW Management Module Subproject

Project Wiki with latest specification :
https://www.opencompute.org/wiki/Hardware_Management/Hardware_Management_Module

Mailing list: OCP-HWMgt-Module@OCP-All.groups.io

Thank you!