DC-SCM 2.0 Specification Update

Qian Wang, Software Architect, Intel

Tim Lambert, Distinguished Engineer, Dell EMC
DC-SCM2.0 Overview

A collaboration to expand upon the DC-SCM 1.0 specification to allow for future scalability and longevity across multiple generations of enterprise platforms. To support evolving manageability interfaces, range of entities being securely managed and forthcoming use cases such as multi-node server designs.
DC-SCM 2.0 changes from 1.0

• "Plug & Code" model to achieve universality among Host Processor Modules (HPM) and DC-SCMs
• Evolved interfaces for broader and future looking use cases with more typical examples toward maximizing interoperability
• Refined power states, limits and discovery rules for improved electrical compatibilities
• Overlayed dual-node alternate pin definition
• Evolved high-speed serial interface & protocol (LTPI) for pin reduction, remote BMC peripheral expansion & low latency transfers
• Mechanical foolproof break in compatibility between 1.0 & 2.0 (connector skew)
DC-SCM2.0 example use diagram
DC-SCM2.0 LTPI – LVDS Tunneling Protocol & Interface

Kasper Wszolek and Yi Zeng (Intel) own this section

DC-SCM 1.0

DC-SCM CPLD/ FPGA

Many GPIOs

SGPIO

DC-SCM 2.0

DC-SCM CPLD/ FPGA

Fewer GPIOs

LTPI

HPM

HPM FPGA

Slow, Single ended, Fixed length GPIO bit shifter

High Speed, differential, Lower latency, Multi-channel, GPIOs + remote peripherals

See LTPI workshop on-demand video and spec for more details
DC-SCM2.0 Mechanical Changes

Glen Hanna (Intel) owns this section of the spec

Many great ideas from Andrew Junkins (Lenovo)

- All refinements targeted at horizontal form factor only
- Same X-Y board dimensions
- Removed vertical formfactor in the 2.0 spec
- Same 168 pin standard 4C+ connector, shifted to prevent cross version mis-plugs
- Improved keep-outs to maximize usable 3D and board space
- Added eject and install/hold down options
- More generic models for I/O face plate/port flexibility
- Removal of specific daughter card sizes/locations such as TPM and platform root of trust

OPEN POSSIBILITIES.
DC-SCM2.0 Power Sequencing & Discovery

• "Plug-n-Code" is enabled via "Plug-N-Detect-Else-Halt" Guidance with optional step bypasses in closed / non-cross compatibility necessary environments
• Power state common nomenclatures (Pre-STBY, STBY, S5, S0)
• DC-SCM 2.0 sourced trickle power rail for HPM FRU/ Authentication IC, aiding discovery before engaging system specific rails/interfaces
• Narrowed voltage tolerance to improve DC-SCM peripheral options (from 10-14V to 12.0V +-10% with a new max target wattage)
• Increased battery drain max by 200nA
• Refined physical handshakes and example virtual handshakes
DC-SCM2.0 Interface Definition

- Common bus/signal/partition name & instance nomenclatures
- Best fit pin assignments / bus counts / voltages / mutually-exclusive alternate pin functions for multi-generational expected use cases.
- Accommodates all asks within pin count constraints
- Targeted min BOM cost where possible e.g., 2 clocks vs always a fanout buffer
- Alternate pin functions in typical-to-exotic order
- Defined minimum system power state where bias is allowed for every signal, driving clear rules for cross-power domain logic (avoiding contention + leakage)
- Multi-voltage pin allowances based on DC-SCM 2.0 + HPM combination
- Refined typical example interface drawings to aid adopters
### High-Level Interface Deltas between 1.0 and 2.0

<table>
<thead>
<tr>
<th>Features</th>
<th>DC-SCM1.0</th>
<th>DC-SCM2.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SGPIO</td>
<td>yes</td>
<td>removed</td>
</tr>
<tr>
<td>LTPI (serialization over LVDS)</td>
<td>no</td>
<td>new</td>
</tr>
<tr>
<td>I2C 3.3V</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>I2C/I3C 1.8V</td>
<td></td>
<td>new</td>
</tr>
<tr>
<td>I3C 1.0V</td>
<td>1.0V</td>
<td>1.8V</td>
</tr>
<tr>
<td>I3C/FSI 1.0/1.2</td>
<td></td>
<td>new</td>
</tr>
<tr>
<td>PCIE topology</td>
<td>yes</td>
<td>Enhanced options</td>
</tr>
<tr>
<td>USB topology</td>
<td></td>
<td>Host &amp; managed USB enhanced options</td>
</tr>
<tr>
<td>Dual node support</td>
<td></td>
<td>new</td>
</tr>
<tr>
<td>SPI</td>
<td>yes</td>
<td>more alt-functions</td>
</tr>
<tr>
<td>NCSI</td>
<td>yes</td>
<td>2x with alt-functions</td>
</tr>
<tr>
<td>VCC_SCM_HPM_FRU</td>
<td></td>
<td>new</td>
</tr>
<tr>
<td>VIRTUAL_RESEAT</td>
<td>yes</td>
<td>removed</td>
</tr>
<tr>
<td>HPM_FW_RECOVERY</td>
<td>yes</td>
<td>removed</td>
</tr>
</tbody>
</table>
DC-SCM Future Exploration Topics

- New or optional expansion connector for more pins where needed
- Compliance test vehicle
- Continually evaluate evolving interfaces/voltages/HPM use cases
Call to Action

Project Wiki: [https://www.opencompute.org/wiki/Hardware_Management/Hardware_Management_Module](https://www.opencompute.org/wiki/Hardware_Management/Hardware_Management_Module)

Mailing list: [https://ocp-all.groups.io/g/OCP-HWMgt-Module](https://ocp-all.groups.io/g/OCP-HWMgt-Module)

Call to community to add what is missing/wish-list to public wiki

Specification contribution targeted for 2022

Please visit the Experience Center for LTPI demos
Thank you!