

# Multiphysics Simulation for Chiplets

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## **Physical Integrity Challenges**





Thermal Integrity Power Integrity Signal Integrity EMI/EMC ESD

Need for Chip Aware System Simulations

## Wafer Scale Engine (WSE)

- CS-1 being used at Argonne national Laboratory
- 15-20 kW
- 1.2 trillion transistors

Purpose-built for Deep Learning: enormous compute, fast memory and communication bandwidth

**46,225 mm<sup>2</sup> chip** 56x larger than the biggest GPU ever made

**400,000 core** 78x more cores

18 GB on-chip SRAM 3000x more on-chip memory

100 Pb/s interconnect 33,000x more bandwidth



Image from cerebras.net

## **Advanced Multi-Die Packaging**

## ANSYS Solutions certified for latest packaging technologies

## ADVANCED PACKAGING



#### 3D-IC/2.5D-IC and FOWLP

- Multi-die Co-analysis
- Power, Signal & Thermal Integrity

ANSYS multiphysics solutions are now certified for TSMC's latest SoIC, CoWoS and InFO\_MS advanced packaging technologies. It can simulate 3D-IC, 2.5D-IC, fan-out wafer-level packaging (FOWLP) and more.

#### ANSYS Achieves Certification for TSMC's Innovative System-On-Integrated-Chips (TSMC-SoIC™) Aadvanced 3D Chip Stacking Technology

TSMC and ANSYS enable 3D-IC reference flows for mutual customers to address multiphysics challenges

PITTSBURGH, Apr. 24, 2019 – TSMC certified ANSYS (NASDAQ: ANSS) solutions for its innovative System-on-Integrated-Chips (TSMC-SoIC<sup>\*\*</sup>) advanced 3D chip stacking technology. SoIC is an advanced interconnect technology for multi-die stacking on system-level integration using Through Silicon Via (TSV) and chip-on-wafer bonding process — enabling customers with greater power efficiency and performance for highly complex and demanding cloud and data center applications.

ANSYS multiphysics solutions for SoIC enable multi-die co-simulation and co-analysis for extraction, power and signal integrity analysis, power and signal electromigration analysis, and thermal and thermal-induced stress analysis.

In addition to SolC certification, TSMC validated the reference flow for the latest Chip-on-Wafer-on-Substrate (CoWoS®) packaging technology using ANSYS® RedHawk™, ANSYS® RedHawk-CTA™, ANSYS® CMA™ and ANSYS® CSM<sup>™</sup> and their corresponding chip models for system level analysis.

"We're pleased with the result of our collaboration with ANSYS in delivery of TSMC-SolC" technology reference flow, which empowers customers to address growing performance, reliability and power demands for cloud and data center applications," said Suk Lee, senior director, design infrastructure management division at TSMC. "The collaborative efforts combining ANSYS' comprehensive chippackage co-analysis solutions with TSMC SolC advanced chip stacking technology address complex multiphysics challenges in 3D-IC packaging technologies."

"Our 3D-IC solutions address complex multiphysics challenges to meet the stringent power, performance, thermal and reliability requirements," said John Lee, general manager at ANSYS. "ANSYS' comprehensive chip aware system and system aware chip signoff solutions empower mutual customers to accelerate design convergence with greater confidence."

#### About ANSYS, Inc.

If you've ever seen a rocket launch, flown on an airplane, driven a car, used a computer, touched a mobile device, crossed a bridge or put on wearable technology, chances are you've used a product where ANSYS software played a critical role in its creation. ANSYS is the global leader in engineering simulation. Through our strategy of Pervasive Engineering Simulation, we help the world's most innovative companies deliver radically better products to their customers. By offering the best and broadest portfolio of engineering simulation software, we help them solve the most complex design challenges and create products limited only by imagination. Founded in 1970, ANSYS is headquartered south of Pittsburgh, Pennsylvania, U.S.A., Visit www.ansys.com for more information.

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ANSS-C

## **ANSYS and SAMSUNG partners for 3DIC design**



### Samsung Foundry Certifies ANSYS Multiphysics Simulation Solutions for Multi-Die Integration Advanced Packaging Technology

ANSYS and Samsung enable new 3D-IC reference flows for AI, 5G, automotive, high-performance computing and networking applications

PITTSBURGH, October 17, 2019 – Samsung Foundry certified ANSYS (NASDAQ: ANSS) multiphysics simulation solutions for its latest multi-die integration<sup>™</sup> (MDI) advanced two and a half dimensional/three-dimensional integrated circuit (2.5D/3D-IC) packaging technology. The certification empowers mutual customers to achieve higher performance and lower power within a smaller form factor when designing 2.5/3D-ICs for artificial intelligence (AI), 5G, automotive, networking and high-performance computing (HPC) applications.

System-in-Package designs — enabled by Samsung MDI — are highly complex with multiple dies integrated on an interposer in a 2.5D/3D packaging configuration. MDI flow combines analysis, implementation and physical verification in a single canvas and uniquely features early-stage system-level pathfinding and complex multiphysics signoff capabilities. These designs are widely used in AI, 5G, automotive, high-speed networking and HPC applications to achieve extreme system bandwidth, low latency and high performance. ANSYS multiphysics simulation solutions for MDI signoff offer a complete 2.5D/3D-IC methodology for power, signal and thermal integrity and reliability analysis across the broad frequency spectrum of chip, package and board and system design to improve engineering efficiency, achieve simulation accuracy and accelerate time-to-results.

Samsung Foundry certifies ANSYS® Icepak® and ANSYS® RedHawk<sup>™</sup> family of solutions for power, signal and thermal integrity and reliability analyses. The certification allows for detailed modeling of silicon interposer, through silicon vias, microbumps, high-bandwidth memory, high-speed interfaces and different dies, which is critical for accurately simulating power, signal and thermal integrity effects.

"Samsung Foundry and ANSYS' advanced packaging reference flows for MDI empower our mutual customers to achieve improved power, performance and area requirements, as well as cost and turn-around time reduction through accurate analysis of complex interconnections across the chip, package and board," said Jung Yun Choi, vice president, foundry design technology team at Samsung Electronics. "ANSYS provides comprehensive chip-package-system co-analysis workflows for addressing complex multiphysics challenges of extraction, power and signal electromigration, thermal-induced stress, signal integrity and reliability in 2.5D/3D-IC packaging technologies."

## eSilicon Uses ANSYS Multiphysics Simulations

Achieve Silicon to System Success



#### Example of a hyperscale data center ASIC

eSilicon's highly configurable FinFET-class IP platform includes applicationoptimized processor core and a number of high-bandwidth memory(HBM) stacks integrated on a silicon interposer, built into a complex 2.5D package



"With design costs in the tens of millions of dollars and re-spins resulting in schedule delays and missed market opportunities, eSilicon relies on ANSYS' chippackage-system(CPS) modeling and simulation software."

Teddy Lee, Architect SI/PI, eSilicon Corporation, San Jose, USA 2019 ANSYS ADVANTAGE Find interview on "ANSYS, inc." youtube page.

## Eco System for 2.5D/3D IC Power, Signal and Thermal Integrity

## Need for accurate and easy set up for chip, package and board co-simulation

- 1. Modeling connectivity of complicated 3DIC structure
- 2. Parasitic modeling of packages (Interposer, FOWLP), board PCB
- 3. Power, signal and thermal modeling of interconnects of stacked dies



Wendem Beyene, "Power Delivery Network Design and Optimization for High-Speed Systems with Si Interposer", DesignCon 2017

## **Parasitic Extraction**



## Multi Die System PDN Coverage Current Model Generation in ANSYS CMA



## **CPS – Thermal Integrity**

Power-Thermal Analysis

Chip-Package-System information feed small to large



Chip-Package-System information feed large to small

## **CDX work**

- Provide chiplet and p-chiplet integrators with relevant information required for power and thermal modeling.
- Information will allow for analysis at early and late stages of design
- Precision of results will be controlled by data utilized. Early analysis being less precise that final.
- Enable means for dealing with missing or un-available data for given (p)chiplet

## **Input Data for Power and Thermal Analysis**

## • Zeff format used to store chiplet information

- Thermal resistance
- Power information
- Large number of entries will be used to make estimates for parts with missing data
- Precision of results affected by variation in input data
- Interposer/pcb layout and placement information
  - Material properties both electric and thermal
  - Block information can be used for thermal
  - Layout information required for power integrity
- Thermal boundary conditions
  - Fan placement
  - HTC (Heat Transfer Coefficient) boundaries

## Validation

 The proposed specifications for performing thermal and power analysis will be validated on the PoC and results with basic input data vs a full signoff analysis with detailed chip thermal models will be compared along with precision of results

# Thank You