

OCP ODSA's Bunch of Wires (BoW) Interface for Die-to-Die Applications

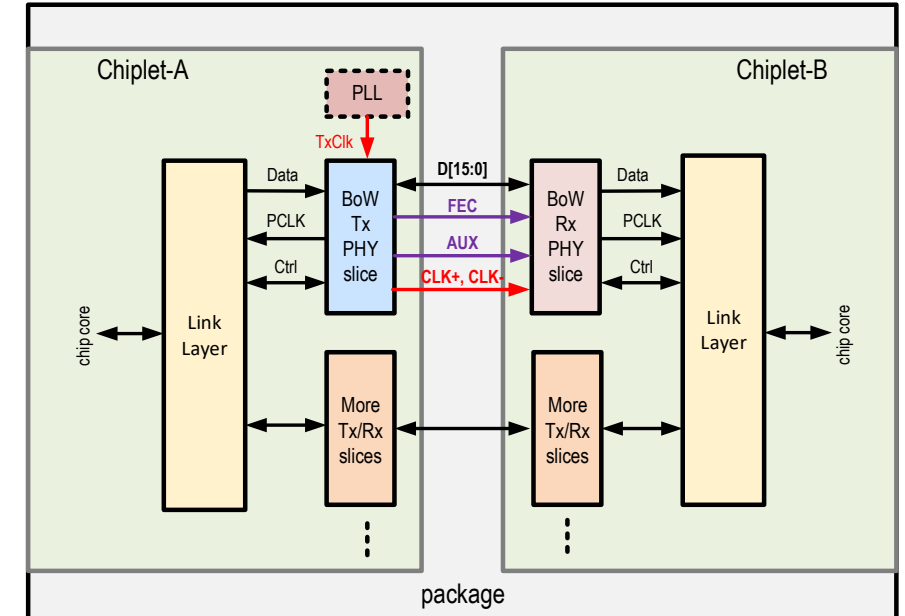
Elad Alon – Blue Cheetah Analog Design

Bapi Vinnakota – Broadcom

Jayaprakash Balachandran - Cisco

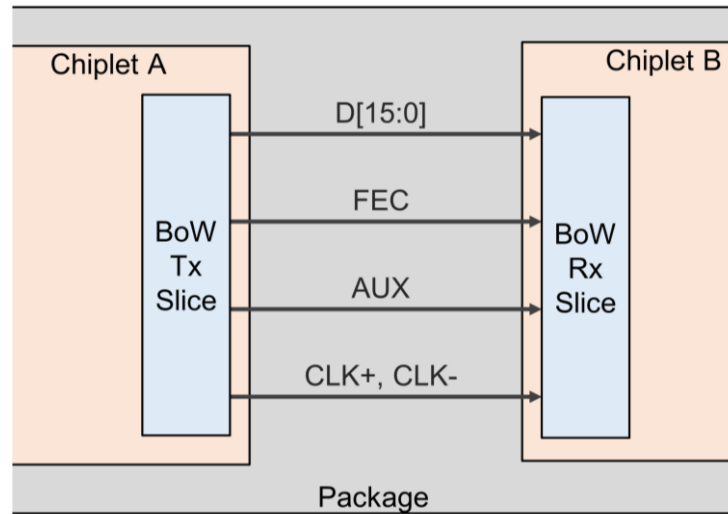
Bunch of Wires (BoW): Key Features

- BoW is an open PHY specification for die-to-die parallel interfaces
 - Optimized for both commodity (organic laminate) and advanced packaging technologies
 - Compatible with a wide range of packages and IC processes
 - Architected to allow many use cases driving significant economies of scale
 - State-of-the-art performance metrics

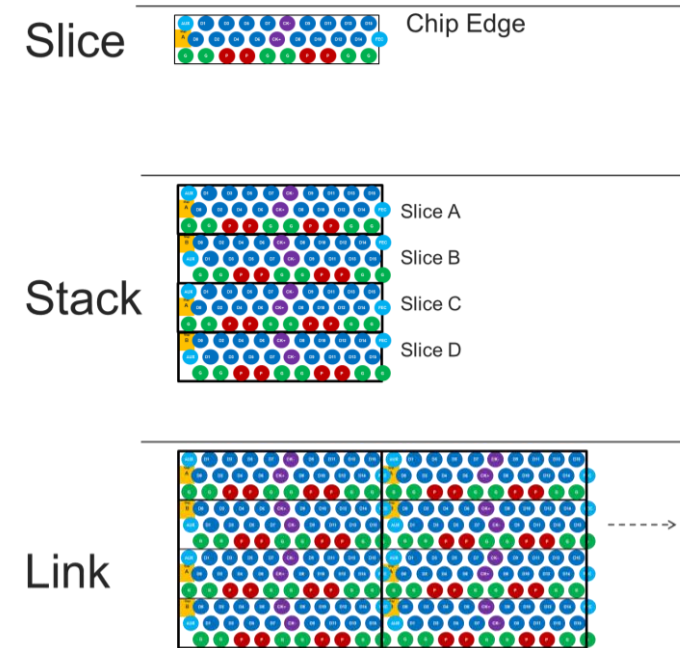


Packaging	Organic	Advanced
Max BW density	1.034 Tb/s/mm	5.12 Tb/s/mm
Energy / bit	<0.5 pJ/bit	< 0.25 pJ/bit
BER	<1e-15	<1e-15
Reach	25 mm	5 mm
Latency	<2 ns	<2 ns

BoW Basic Organization

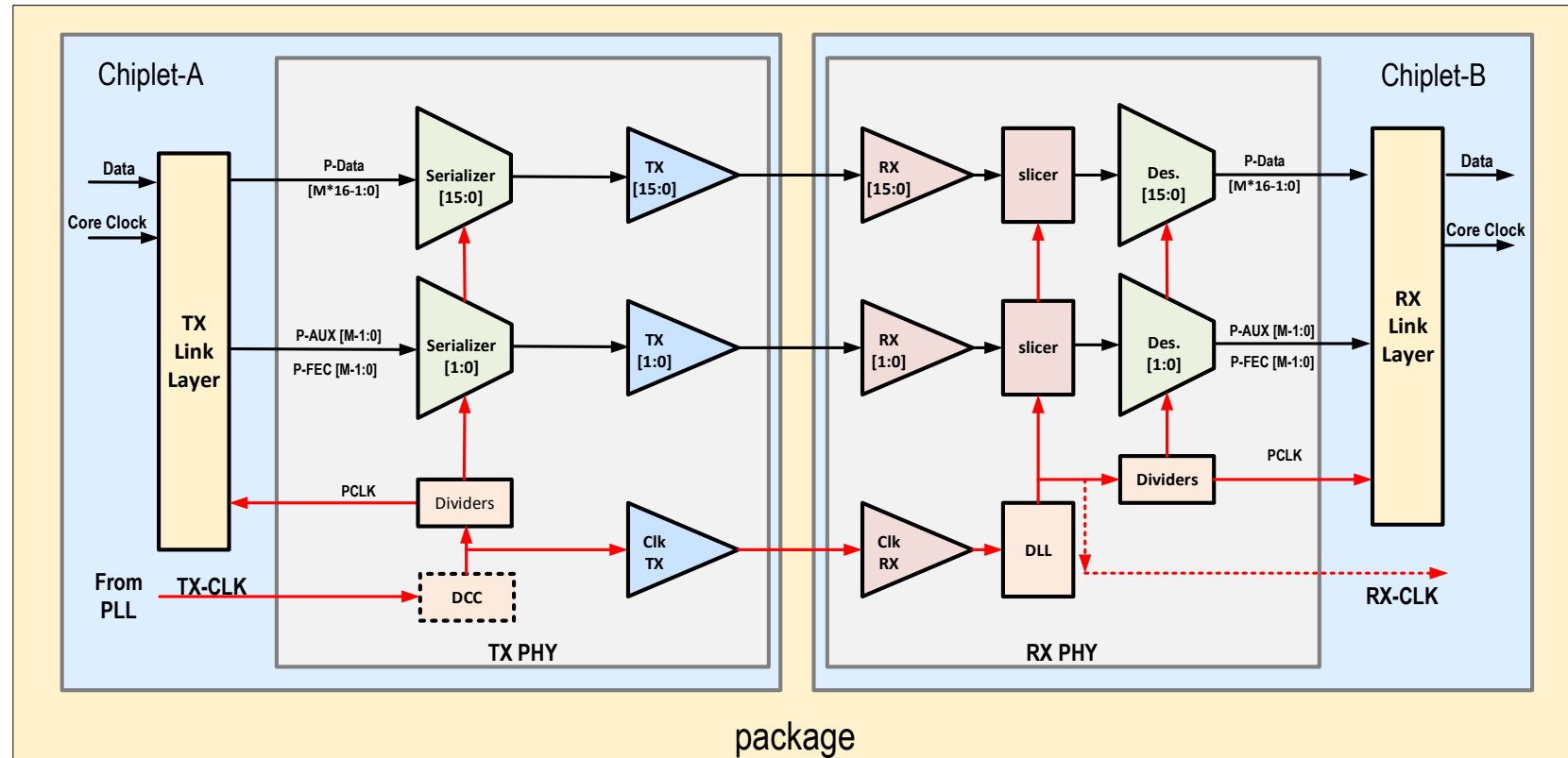


- Slice is the basic unit element
 - 16 data wires
 - Source-synchronous differential clock
 - Optional FEC (error correction) / AUX (DBI / repair / control)



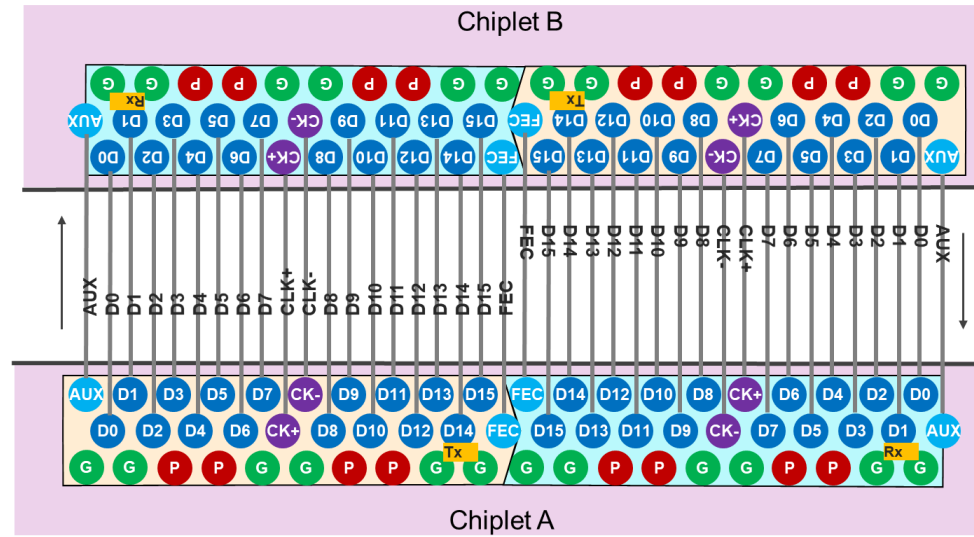
- Stack: group of slices extending towards the inside of the chiplet
- Link: one or more slices forming a logical interface from one chiplet to another
 - May be symmetric, asymmetric, or unidirectional

Slice to Link Layer Interface



- PHY slices include on ser. / deser. – no required clock domain crossing (CDC)
 - Need for CDC is usage dependent, hence decision should be made outside of the PHY
 - Allows for implementations with lowest possible latency

BoW Interoperability and Flexibility

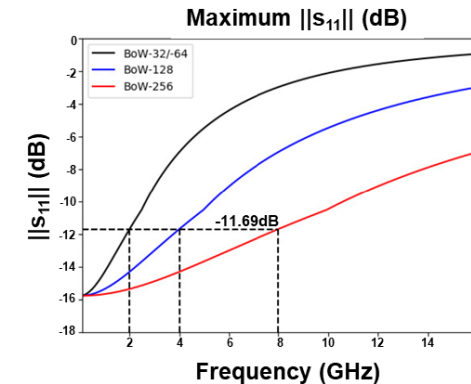


- Specification only requires wire order on the package, not a specific bump map
 - Fosters flexibility while retaining interoperability
- All BoW PHYs must support 0.75V to ensure compatibility across wide range of process technologies

BoW Electrical Specifications

- Detailed set of electrical and timing requirements are included in the specification
 - Specs developed based on studies from community-contributed channels as well as experience from in-flight designs
 - Specs provide clear and detailed guidance to PHY designers while retaining flexibility

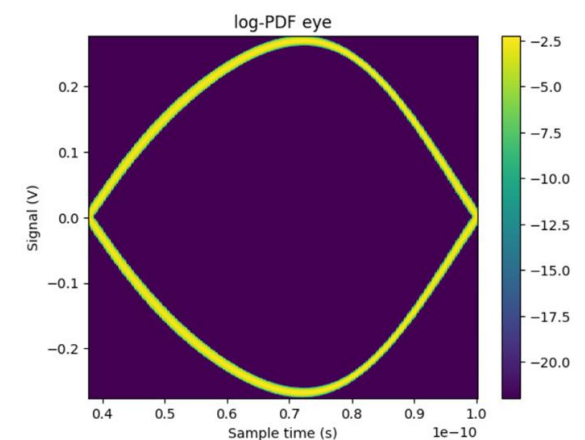
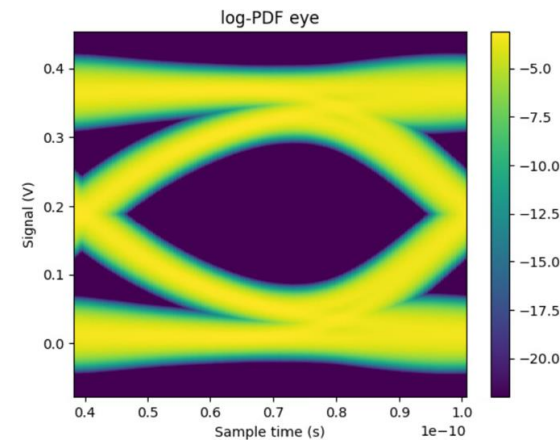
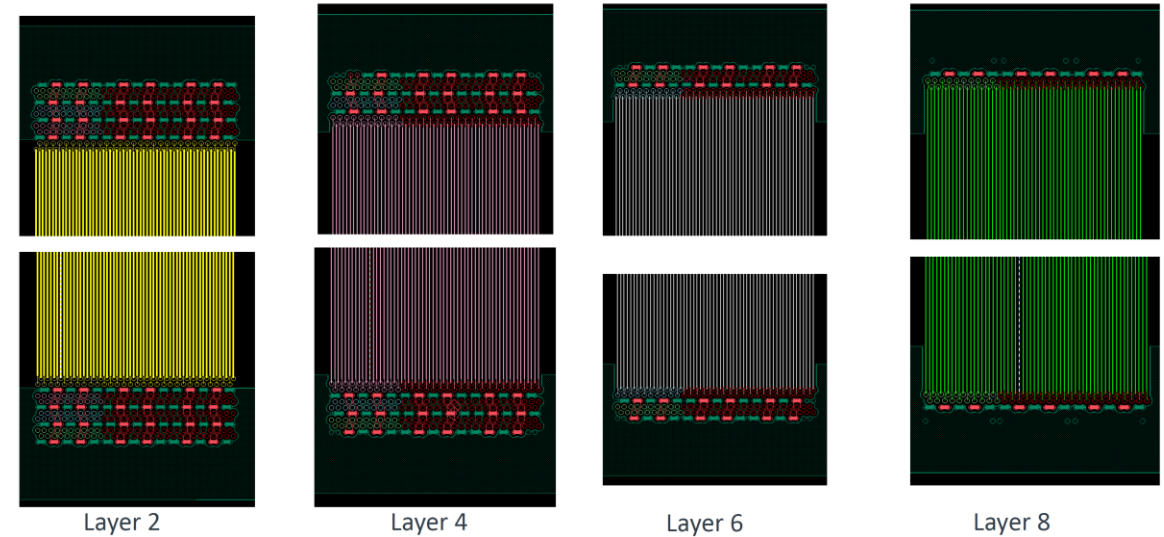
	Underterminated	Source-Terminated	Doubly Terminated
TX DC Term.	As required to meet TX rise-time	36 Ω - 50 Ω (0.72 - 1.0 Z_{chan})	36 Ω - 50 Ω (0.72 - 1.0 Z_{chan})
RX DC Term.	-	-	50 Ω - 69 Ω (1.0 - 1.38 Z_{chan})
Within-Slice DC Term. Matching	-	$\sigma = 1.333\%$ (8% over 6 σ)	$\sigma = 0.667\%$ (4% over 6 σ)



	BoW-256	BoW-128	BoW-128	BoW-64 or BoW-32	BoW-64 or BoW-32
	Any Termination	Doubly Terminated	Source- or Underterminated	Doubly Terminated	Source- or Underterminated
$V_{\text{err,det,RX}}$	40 mV	40 mV	100 mV	65 mV	150 mV
$V_{\text{err,tot,RX}}$	75 mV	75 mV	150 mV	100 mV	200 mV
$t_{\text{err,det,RX}}$	32% T_{bit}	32% T_{bit}	32% T_{bit}	28% T_{bit}	28% T_{bit}
$t_{\text{err,tot,RX}}$	40.5% T_{bit}	40.5% T_{bit}	40.5% T_{bit}	36.5% T_{bit}	36.5% T_{bit}

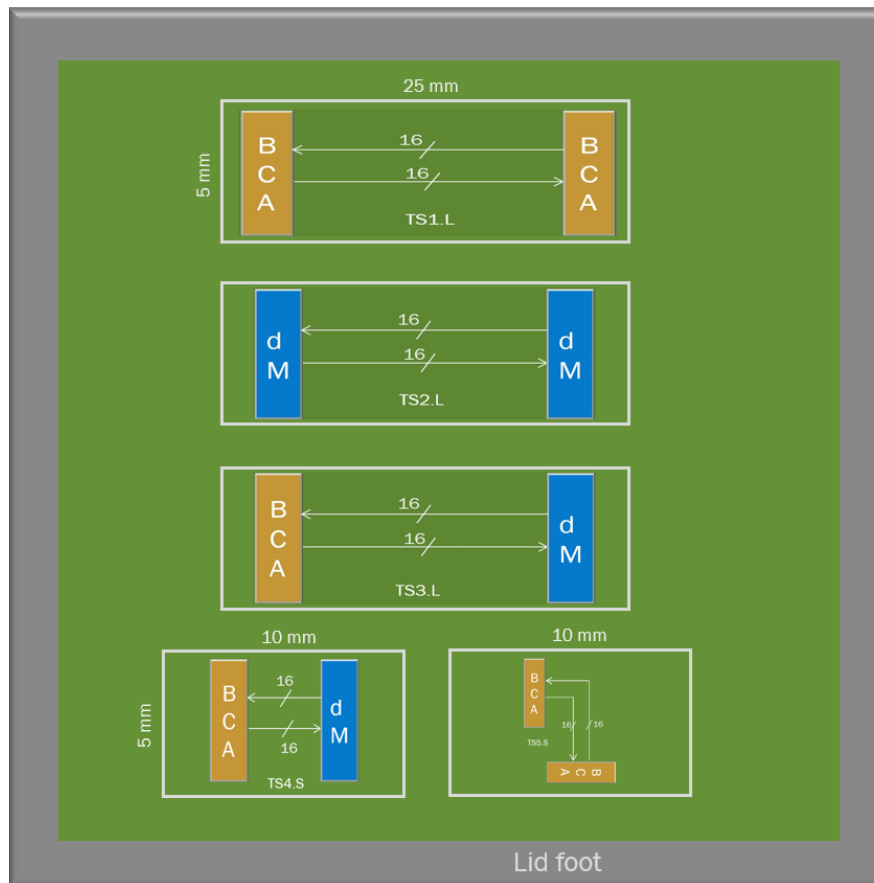
BoW Channel Compliance

- Channel compliance defined by performance achieved with reference TX/RX
- Open source software for compliance checking and system simulation will be released in the near future
- Multiple reference channel designs / models and associated SI analysis results publicly available



BoW “Plugfest”

- Community-driven effort to accelerate adoption via multi-vendor interoperability testing and validation



S.No	Package Design Attribute	Value
1	# dies per package	10 (BCA – 6, dMatrix – 4)
2	Die Technology	BCA – 12 nm TSMC , dMatrix – 6 nm TSMC
3	Die size	BCA : 2.5 x 2.6 mm dMatrix : 1.284 mm x 3.264 mm
4	Package size	40 x 40 mm FCBGA
5	Layer count	5-2-5
6	Bump pitch	130 um
7	BGA Ball Pitch	0.8 mm
8	Package build up dielectric	GL102
9	# Test Sites	5 .L – 20 mm long .S – 5 mm long

Status (1)

- Draft specification has been publicly available since the inception of the working group
 - Voting on final approval of the specification happening right now
- An ecosystem has already formed, and BoW is being designed into products today
 - Known PHY implementations in 65nm, 22nm, 16nm, 12nm, 6nm, and 5nm
 - 7 companies have announced IP and/or chiplet products based on BoW
 - At least 4 more companies known to have internal projects based on BoW

Status (2)

- Open standard for link layer enabling disaggregation of on-die AMBA buses (such as AXI and CHI) nearing completion
- Development of next generations of BoW well under way
 - 24 – 32 Gb/s (BoW-384 & BoW-512) at <750fJ/bit
 - Improved energy-proportionality without sacrificing bandwidth density
 - Reduced width slices to support the most cost-sensitive applications

Summary

- BoW is uniquely designed to allow adopters to select and trade off between package, process, performance and complexity without needing to switch D2D PHY standards
- BoW is available now and is being actively adopted for die disaggregation applications
- BoW is openly licensed and available to anyone for adoption
 - Beyond adoption, you can participate in the growing ecosystem by:
 - Participating in the test package “plugfest” development effort
 - Joining the working group and providing feedback on the current spec
 - Joining the working group and defining the next generation
 - See <https://github.com/opencomputeproject/ODSA-BoW> and <https://www.opencompute.org/wiki/Server/ODSA> for additional resources/information



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Questions