THE PATH TO A CHIPLET ECOSYSTEM

Ramune Nagisetty
Senior Principal Engineer
Director, Process and Product Integration
Intel CTO Office
This presentation contains the general insights and opinions of Intel Corporation (“Intel”). The information in this presentation is provided for information only and is not to be relied upon for any other purpose than educational. Statements in this document that refer to Intel's plans and expectations for the quarter, the year, and the future, are forward-looking statements that involve a number of risks and uncertainties. A detailed discussion of the factors that could affect Intel's results and plans is included in Intel's SEC filings, including the annual report on Form 10-K.

Any forecasts of goods and services needed for Intel's operations are provided for discussion purposes only. Intel will have no liability to make any purchase in connection with forecasts published in this document. Intel accepts no duty to update this presentation based on more current information. Intel is not liable for any damages, direct or indirect, consequential or otherwise, that may arise, directly or indirectly, from the use or misuse of the information in this presentation. Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Learn more at intel.com, or from the OEM or retailer.

Copyright © 2019 Intel Corporation.
Intel, the Intel logo, are trademarks of Intel Corporation in the U.S. and/or other countries.
*Other names and brands may be claimed as the property of others
Rapidly changing workloads and applications are driving new innovation paradigms.

Data, AI, and Infrastructure

Rise of Disruptive Architectures

I/O Variety & Complexity

Higher Complexity, Shorter Life, More Variety

Standard Protocol Trends

- Memory
  - DDR3
  - DDR4
  - HBM
  - DDR-3DS
  - HMC
- Interface
  - PCIe Gen1
  - PCIe Gen2
  - PCIe Gen3
  - PCIe Gen4
- Fabric
  - AMBA® 3 AXI®
  - AMBA® 4 CHI
  - AMBA® 4 ACE®
  - AMBA® 4 AXI®

Increasing Bandwidth Requirements

Source: Cadence
PACKAGE IS A PLATFORM FOR INNOVATION & AGILITY

TECHNOLOGY DRIVERS
(e.g. heterogeneous integration, reticle limited die, IP porting)

MARKET REQUIREMENTS
(e.g. form factor, accelerators, 3rd party IP, custom solutions)

8th Gen Intel® Core™
Intel high-performance CPU, HBM2 and AMD* discrete graphics

Intel® Stratix® 10 FPGA
HBM + RF XCVR

Intel® Lakefield
3D die stacking
ITRS 2.0 Roadmap Focuses on Heterogeneous Integration and Connectivity

Multivendor Interoperable HBM (High Bandwidth Memory)

27% CAGR in 2.5D/3D Packaging
**ADVANCED MCP LANDSCAPE**

- Key Feature Scaling Metrics:
  - IO/mm/Layer (Escape Density)
  - IO/mm² (Die Area)

Technologies with silicon back-end wiring have the highest wire densities.
EMIB Technology

Flip chip bump pitch 100 um

HBM μ bump pitch 55 um
Localized high density wiring
No practical limits to die size
Standard assembly process
Bridge manufacturing much simpler
Bridge silicon costs < Silicon interposer
  • No TSVs, Significantly less silicon area
Increased package manufacturing complexity

CTE Matched with Si
Excellent chip-attach alignment
Pitch scaling
Interposer size is typically limited by reticle field
  • Efforts in place to develop larger than reticle interposers
TSV capacitance impacts signal integrity of off-package links
Interposer attach adds an extra chip attach step
<table>
<thead>
<tr>
<th></th>
<th>On-board</th>
<th>On-package (FCxGA)</th>
<th>EMIB</th>
<th>On-die</th>
</tr>
</thead>
<tbody>
<tr>
<td>Distance (mm)</td>
<td>1000</td>
<td>2-50</td>
<td>1-3</td>
<td>&lt; 1</td>
</tr>
<tr>
<td>Wire Density (lines/mm/layer)</td>
<td>Up to 15</td>
<td>35</td>
<td>1000+</td>
<td>1000+</td>
</tr>
<tr>
<td>Power (pJ/bit)</td>
<td>7-20</td>
<td>1-2</td>
<td>&lt;1</td>
<td>.1</td>
</tr>
<tr>
<td>BW/shoreline (Gbps/mm)</td>
<td>200</td>
<td>250</td>
<td>1000+</td>
<td></td>
</tr>
<tr>
<td>Standards</td>
<td>PCIe, DDR</td>
<td>AIB*, HBM</td>
<td>AMBA, ...</td>
<td></td>
</tr>
</tbody>
</table>

*royalty-free license announced in July 2018
INDUSTRY HAS REACHED AN INFLECTION POINT

Rapidly Emerging New Workloads & Disruptive Architectures
Breakthroughs in Packaging Capabilities Approach On-Die Solutions
New Interface Standards for Package-Level Integration

WE HAVE AN OPPORTUNITY TO SCALE ECOSYSTEM INNOVATION THROUGH PACKAGE LEVEL INTEGRATION OF CHIPLETS
<table>
<thead>
<tr>
<th></th>
<th>Kaby Lake G</th>
<th>Stratix 10 FPGA</th>
<th>Lakefield</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon</td>
<td>Multiple foundries and nodes</td>
<td>Multiple foundries and nodes</td>
<td>Internal silicon on various nodes</td>
</tr>
</tbody>
</table>
| Interface                      | • Industry standard  
• HBM (over EMIB)  
• PCIe (over Std Pckg) | • Industry standard  
• HBM (over EMIB)  
• AIB (over EMIB) | • Proprietary interfaces  
• Logic on logic 3D stacking |
| Comments                        | • Smaller form factor  
• Best in class IP  
• Same die can be used on board  
or in package  
• Most flexible and quickest TTM | • AIB die2die PHY supports EMIB & CoWoS  
• FPGA can be configured for different protocols  
• Mix-n-match approach | • Top and bottom die co-design for floor planning and thermals  
• Limited interoperability and re-use |

---

**DEMORSTRATED RANGE OF CHIPLET SOLUTIONS**
LEVEL OF INTEGRATION DETERMINED BY CAPABILITIES AND REQUIREMENTS. ENABLED BY STANDARDS AND BUSINESS MODELS.

Standardized motherboard interfaces enable the PC ecosystem

Standardized chiplet interfaces enable a package-level integration ecosystem

Standardized SOC interfaces (AMBA/AXI) enable foundry ecosystem

<table>
<thead>
<tr>
<th>From Board to Package</th>
<th>To Package from SOC</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Benefits</strong></td>
<td><strong>Benefits</strong></td>
</tr>
<tr>
<td>Smaller form factor</td>
<td>IP portability/suitability</td>
</tr>
<tr>
<td>Higher bandwidth, lower latency</td>
<td>Potential lower NRE cost &amp; TTM</td>
</tr>
<tr>
<td>Power efficiency</td>
<td>Address reticle size limits, yield</td>
</tr>
<tr>
<td><strong>Challenges</strong></td>
<td><strong>Challenges</strong></td>
</tr>
<tr>
<td>Business models</td>
<td>Form factor, bandwidth, latency,</td>
</tr>
<tr>
<td>Known good die, cost</td>
<td>Silicon area/power overhead</td>
</tr>
<tr>
<td>Thermal limits</td>
<td>Manufacturing cost</td>
</tr>
</tbody>
</table>
Heterogeneous integration drives the need for true KGD
- Comprehensive content at wafer sort

Extremely challenging to probe fine pitch bumps
- Achieve desired coverage without contacting micro-bumps
- Develop HVM methods for Micro-Bump probe

Thermal challenges driven by power, power density, and thermal cross-talk
- Need thermal co-design, improved TIMs + power/thermal management
CHIPLET INTEROPERABILITY ENABLED BY SPECIFICATIONS AND TOOLS

Mechanical
- Bump and wire sizes
- Bonding footprint
- xyz constraints

Power/Thermal
- Power & thermal modeling and cooling solutions

Electrical
- Power delivery
- Noise margin
- Capacitance

Functional
- Data/transaction specifications
- Management: power, security, debug, etc.
- Configuration & statistics
- Manufacturing test access

Lower productization and NRE cost
Industry standard test and DFX
Functional safety, certification, and traceability
Business model and supply chain enablement
Easy to use Tools/Flows/Methods

To minimize area/power/cost and support industry scale interoperability.
CHIPLET INTEROPERABILITY ENABLED BY SPECIFICATIONS AND TOOLS

Mechanical
- Bump and wire sizes
- Bonding footprint
- xyz constraints

Power/Thermal
- Power & thermal modeling and cooling solutions

Electrical
- Power delivery
- Noise margin
- Capacitance

Functional
- Data/transaction specifications
- Management: power, security, debug, etc.
- Configuration & statistics
- Manufacturing test access

New IEEE 2416 standard for power modeling

To minimize area/power/cost and support industry scale interoperability
CHIPLET INTEROPERABILITY ENABLED BY SPECIFICATIONS AND TOOLS

**Mechanical**
- Bump and wire sizes
- Bonding footprint
- xyz constraints

**Power/Thermal**
- Power & thermal modeling and cooling solutions
- New IEEE 2416 standard for power modeling

**Electrical**
- Power delivery
- Noise margin
- Capacitance

**Functional**
- Data/transaction specifications
- Management: power, security, debug, etc.
- Configuration & statistics
- Manufacturing test access
- New PIPE V5.2 support for configurable short reach PHY

To minimize area/power/cost and support industry scale interoperability
Standardized interoperable system-level power model

- Independent of voltage & temp
- Allows many different levels of abstraction from IP Block > chiplet > SOC/SIP
- Early insight into electro-thermal effects

Common modeling language targets 3 classes of users

- Model producers: those developing power models
- Model consumers: those using power models to estimate power
- Tool developers: those building EDA power modeling tools

Future: include static/dynamic thermal modeling & process variation
**PIPE V5.2 SUPPORT FOR SHORT REACH APPLICATIONS**

<table>
<thead>
<tr>
<th>Application</th>
<th>Firmware infrastructure for:</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>accelerator use, host integration¹</td>
</tr>
<tr>
<td>Memory Management</td>
<td>CCIX²/TileLink² for Sync memory traffic</td>
</tr>
<tr>
<td>Link</td>
<td>Instruction-Driven Switch Fabric (ISF)¹ for Async memory traffic</td>
</tr>
<tr>
<td>PCIe PIPE</td>
<td>Shared link layer (E.g. PCIe², TileLink² or Light Link Layer¹)</td>
</tr>
<tr>
<td>PHY</td>
<td>PCIe² Adapter, PIPE Adapter, PIPE Adapter</td>
</tr>
<tr>
<td>PHY</td>
<td>XSR², USR SerDes, AIB, Bunch of Wires (BoW)</td>
</tr>
<tr>
<td>Substrate</td>
<td>Organic substrate packaging¹ + interconnect</td>
</tr>
<tr>
<td>Chiplet</td>
<td>NFP, RISC², FPGA, ML ASIC, SerDes, ...</td>
</tr>
</tbody>
</table>

¹ New Open IP/Specification
² Existing Open Standard

### Configurable Short Reach PHY (sec 2.6)
- Potentially 50% active power reduction
- Reduce power state transition times & reduce cost by moving from AC coupling to DC coupling

### Carry over board-level ecosystem
- Same Si could be used for both board-level & package-level integration
- Mature ecosystems for Si, validation, software, etc.
- Multi-vendor interoperability
- Supports PCIe, CXL, DMI, UPI, CCIX, SATA, USB3.x & DisplayPort
SUMMARY & CONCLUSION

PACKAGING IS A PLATFORM FOR INNOVATION, AGILITY, FLEXIBILITY

ADVANCED PACKAGING APPROACHING MONOLITHIC SOC

A DEMONSTRATED RANGE OF INTEGRATION SOLUTIONS

MORE TO BE DONE ON STANDARDS, TOOLS, AND BUSINESS MODELS TO BUILD THE FOUNDATION OF THE EMERGING CHIPLET ECOSYSTEM