THE PATH TO A CHIPLET ECOSYSTEM

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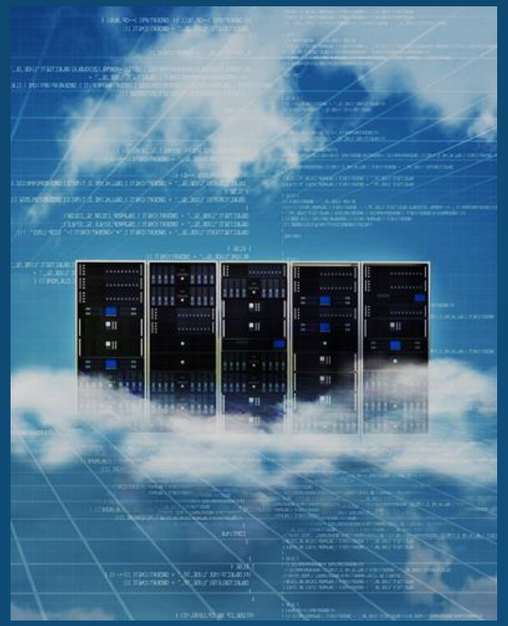
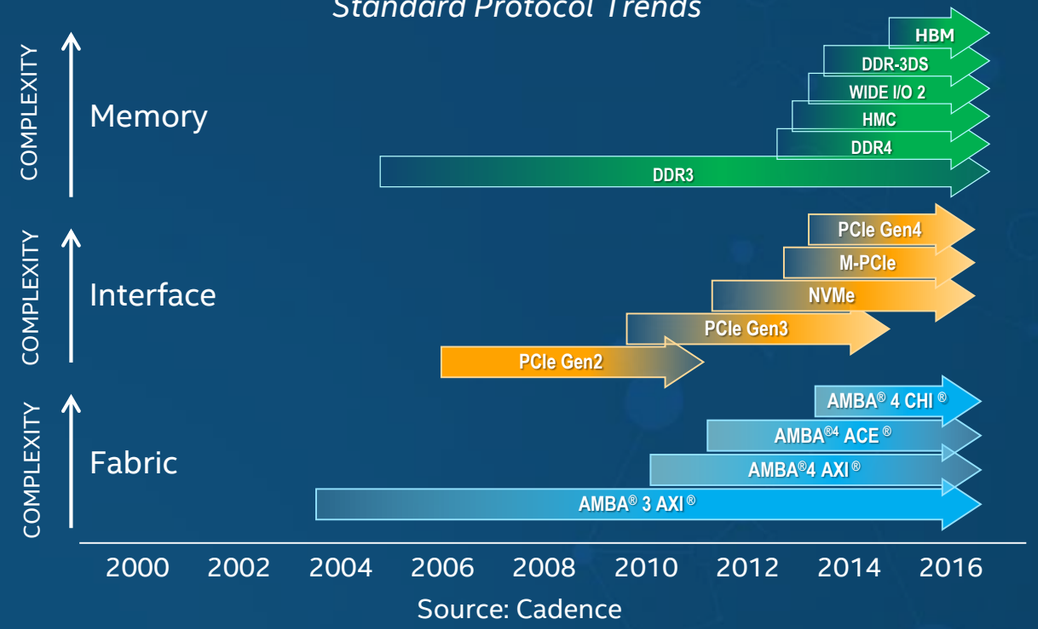
RAPIDLY CHANGING WORKLOADS AND APPLICATIONS

Data, AI, and Infrastructure



I/O Variety & Complexity



Rise of Disruptive Architectures

Increasing Bandwidth Requirements

... ARE DRIVING NEW INNOVATION PARADIGMS

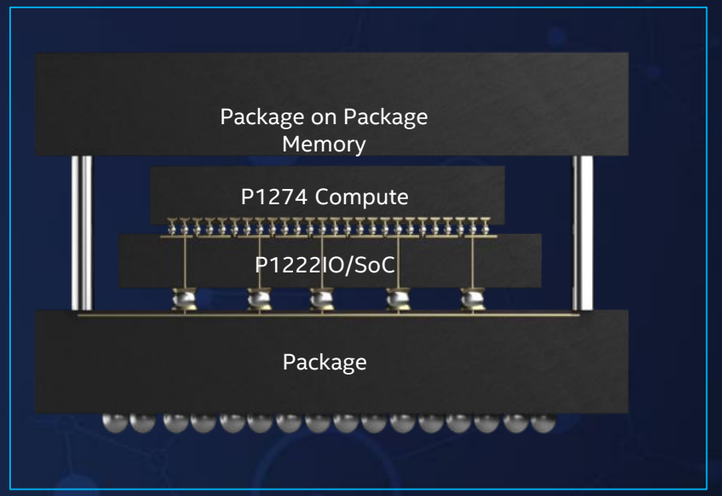
PACKAGE IS A PLATFORM FOR INNOVATION & AGILITY

TECHNOLOGY DRIVERS
(e.g. heterogeneous integration, reticle limited die, IP porting)

MARKET REQUIREMENTS
(e.g. form factor, accelerators, 3rd party IP, custom solutions)

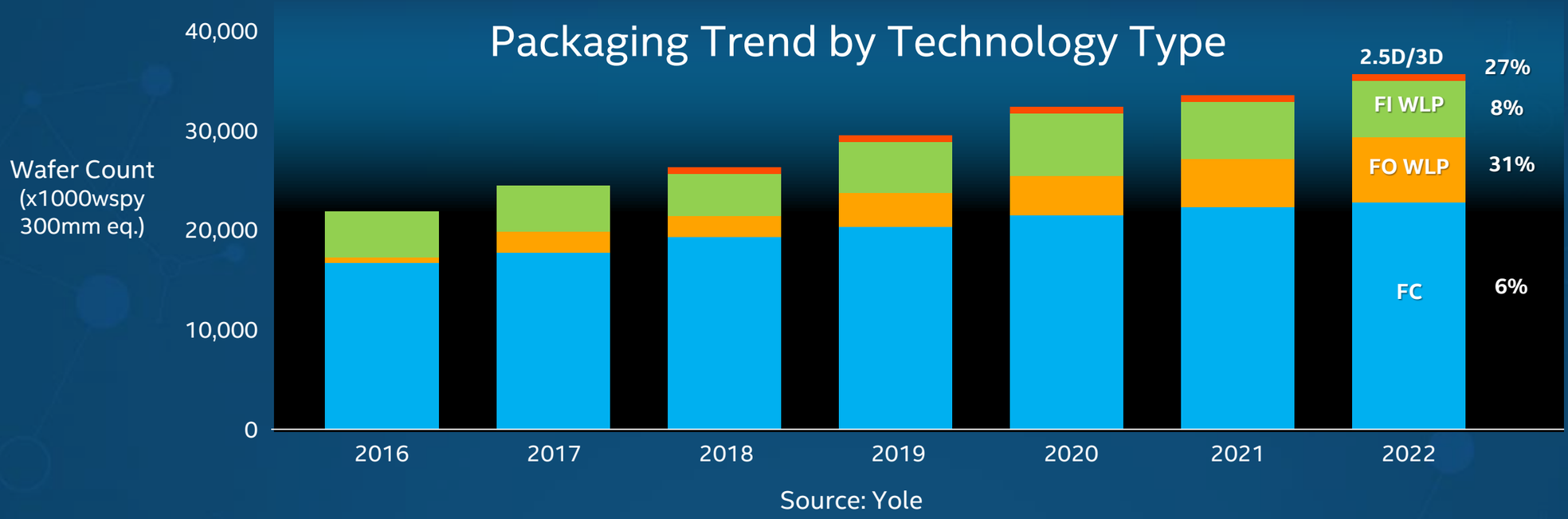
8th Gen Intel® Core™
Intel high-performance CPU, HBM2 and AMD* discrete graphics

Intel® Stratix® 10 FPGA
HBM + RF XCVR



Intel® Lakefield
3D die stacking

PACKAGE-LEVEL INTEGRATION EXPECTED TO GROW FURTHER

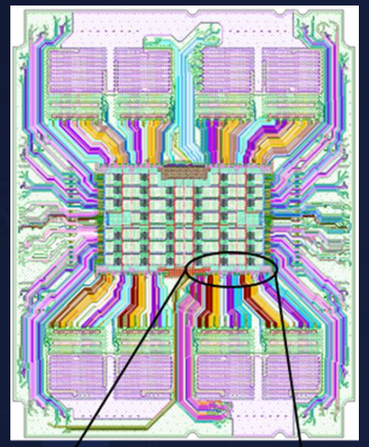


ITRS 2.0 Roadmap Focuses on Heterogeneous Integration and Connectivity

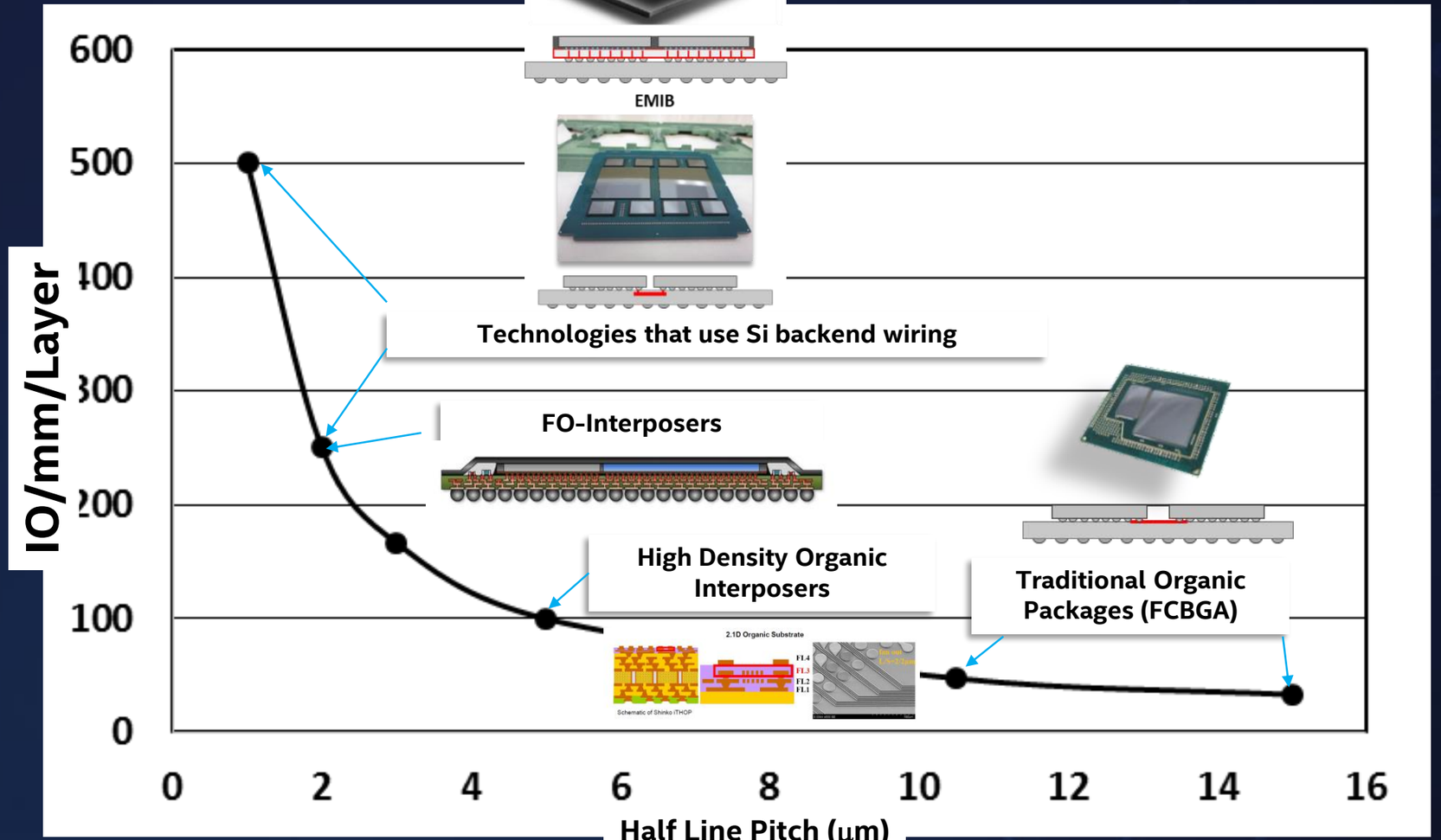
Multivendor Interoperable HBM (High Bandwidth Memory)

27% CAGR in 2.5D/3D Packaging

ADVANCED MCP LANDSCAPE

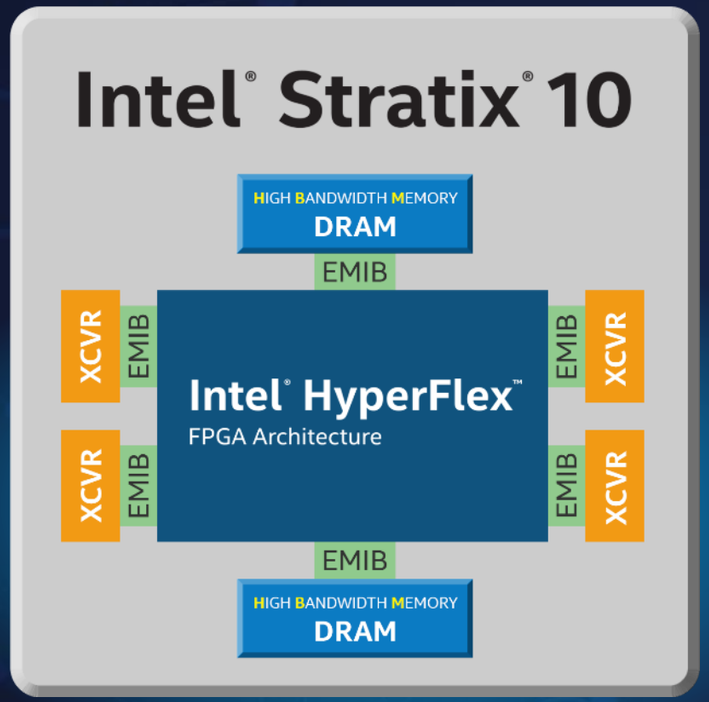


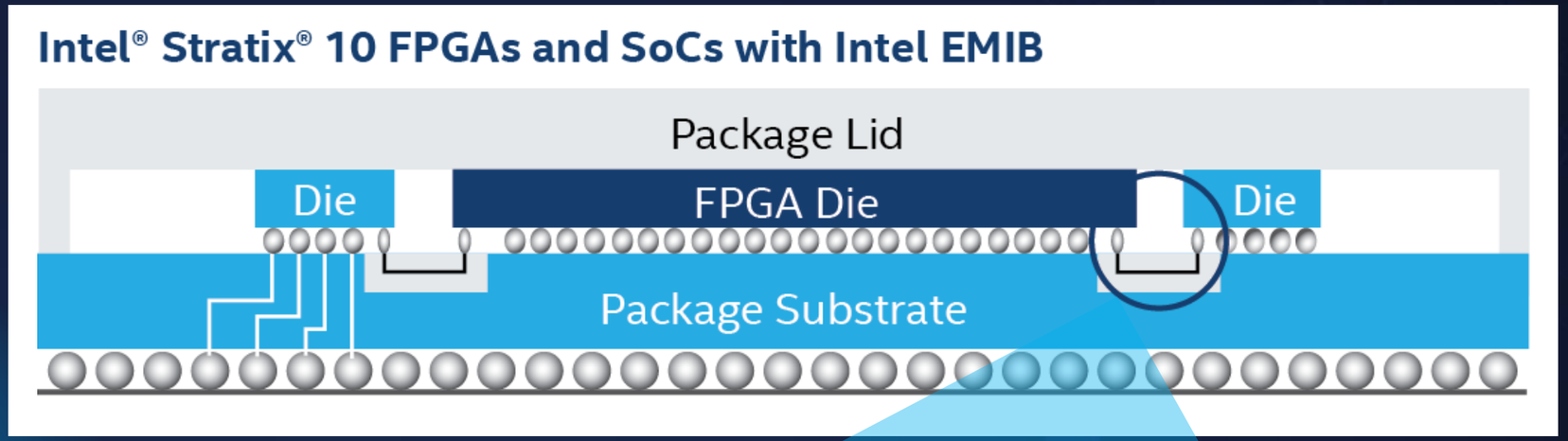
- Key Feature Scaling Metrics:
- IO/mm/Layer (Escape Density)
- IO/mm^2 (Die Area)



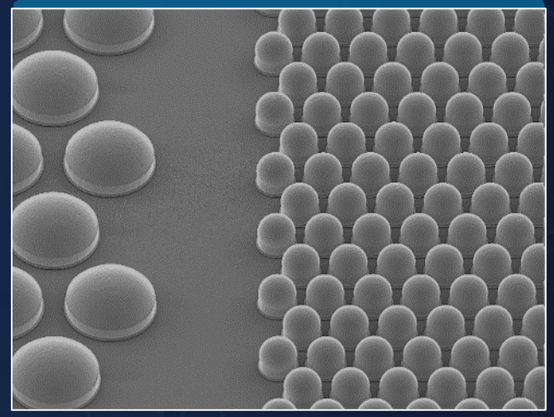
Technologies with silicon back-end wiring have the highest wire densities

INTEL® EMBEDDED MULTI-DIE INTERCONNECT BRIDGE (EMIB) Technology





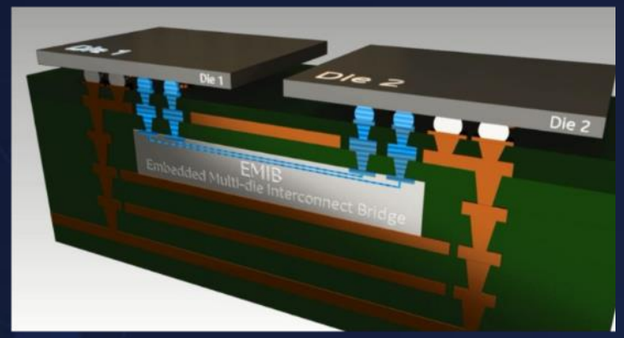
Flip chip bump pitch 100 um



HBM µ bump pitch 55 um

2D/2.5D DENSE MCP TECHNOLOGIES

EMIB



Localized high density wiring

No practical limits to die size

Standard assembly process

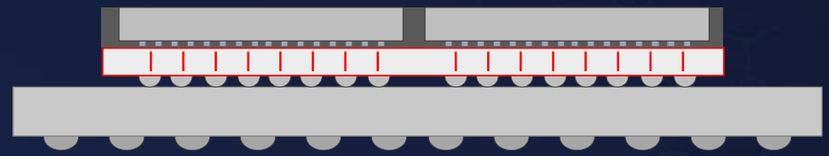
Bridge manufacturing much simpler

Bridge silicon costs < Silicon interposer

- No TSVs, Significantly less silicon area

Increased package manufacturing complexity

Silicon Interposer



CTE Matched with Si

Excellent chip-attach alignment

Pitch scaling

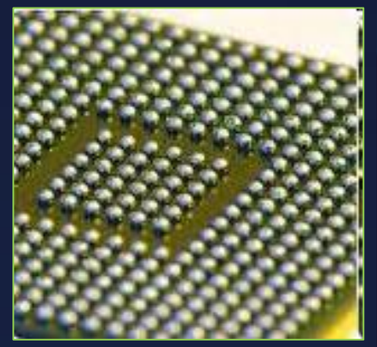
Interposer size is typically limited by reticle field

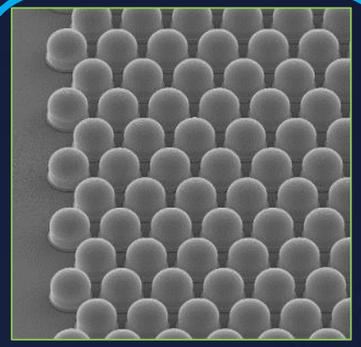
- Efforts in place to develop larger than reticle interposers

TSV capacitance impacts signal integrity of off-package links

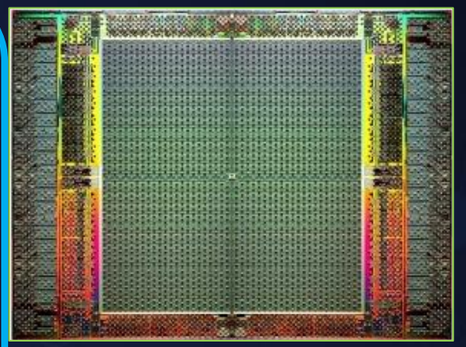
Interposer attach adds an extra chip attach step

NEW PACKAGING CAPABILITIES AND STANDARDS





≈ Near On-Die Capability



	On-board	On-package (FCxGA)	EMIB	On-die
Distance (mm)	1000	2-50	1-3	< 1
Wire Density (lines/mm/layer)	Up to 15	35	1000+	1000+
Power (pJ/bit)	7-20	1-2	<1	.1
BW/shoreline (Gbps/mm)	200	250	1000+	
Standards	PCIe, DDR		AIB*, HBM	AMBA, …

*royalty-free license announced in July 2018

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INDUSTRY HAS REACHED AN INFLECTION POINT

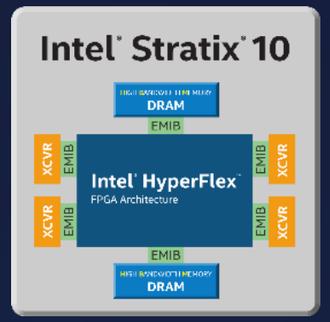
Rapidly Emerging New Workloads & Disruptive Architectures

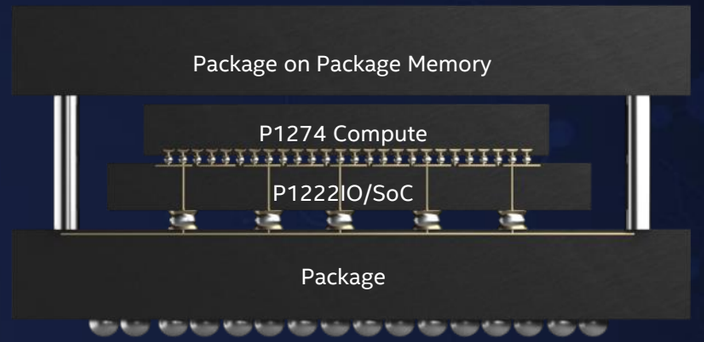
Breakthroughs in Packaging Capabilities Approach On-Die Solutions

New Interface Standards for Package-Level Integration

WE HAVE AN OPPORTUNITY TO SCALE ECOSYSTEM INNOVATION THROUGH PACKAGE LEVEL INTEGRATION OF CHIPLETS

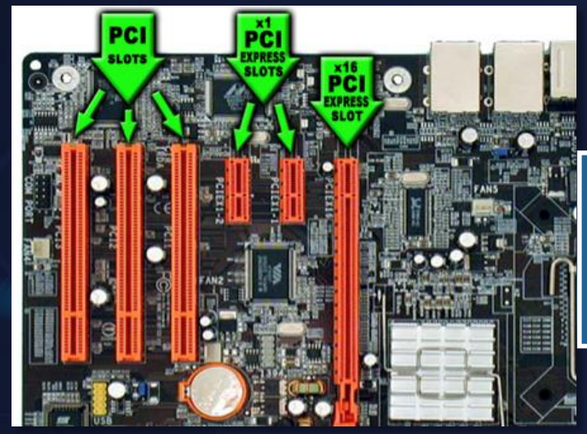
DEMONSTRATED RANGE OF CHIPLET SOLUTIONS





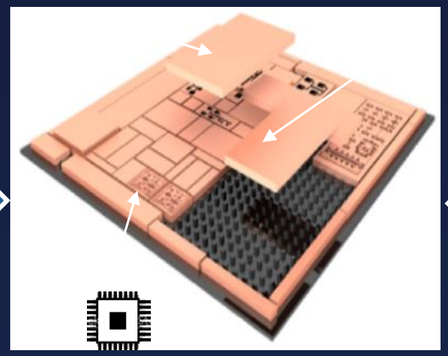
	Kaby Lake G	Stratix 10 FPGA	Lakefield
Silicon	Multiple foundries and nodes	Multiple foundries and nodes	Internal silicon on various nodes
Interface	• Industry standard • HBM (over EMIB) • PCIe (over Std Pckg)	• Industry standard • HBM (over EMIB) • AIB (over EMIB)	• Proprietary interfaces • Logic on logic 3D stacking
Comments	• Smaller form factor • Best in class IP • Same die can be used on board or in package • Most flexible and quickest TTM	• AIB die2die PHY supports EMIB & CoWoS • FPGA can be configured for different protocols • Mix-n-match approach	• Top and bottom die co-design for floor planning and thermals • Limited interoperability and re-use

LEVEL OF INTEGRATION DETERMINED BY CAPABILITIES AND REQUIREMENTS. ENABLED BY STANDARDS AND BUSINESS MODELS.



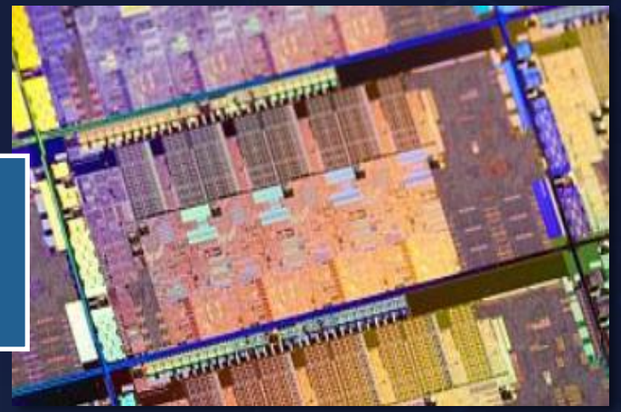
Standardized motherboard interfaces enable the PC ecosystem

Package Level Integration



Standardized chiplet interfaces enable a package-level integration ecosystem

SOC Disaggregation



Standardized SOC interfaces (AMBA/AXI) enable foundry ecosystem

From Board to Package	
Benefits	Smaller form factor Higher bandwidth, lower latency Power efficiency
Challenges	Business models Known good die, cost Thermal limits

To Package from SOC	
Benefits	IP portability/suitability Potential lower NRE cost & TTM Address reticle size limits, yield
Challenges	Form factor, bandwidth, latency, Silicon area/power overhead Manufacturing cost

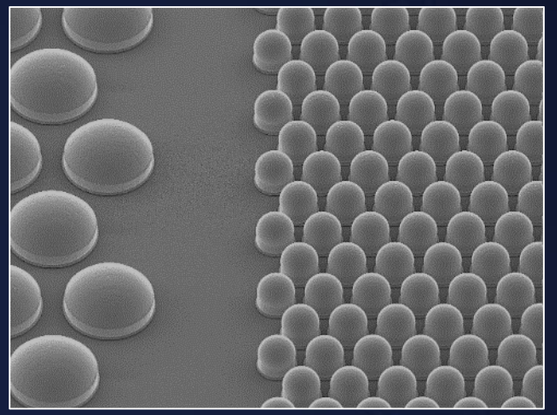
TEST AND THERMAL CHALLENGES

Heterogeneous integration drives the need for true KGD

- Comprehensive content at wafer sort

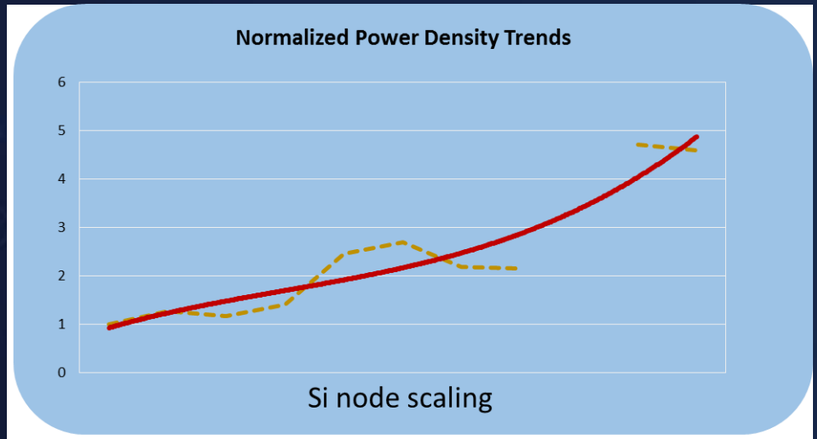
Extremely challenging to probe fine pitch bumps

- Achieve desired coverage without contacting micro-bumps
- Develop HVM methods for Micro-Bump probe

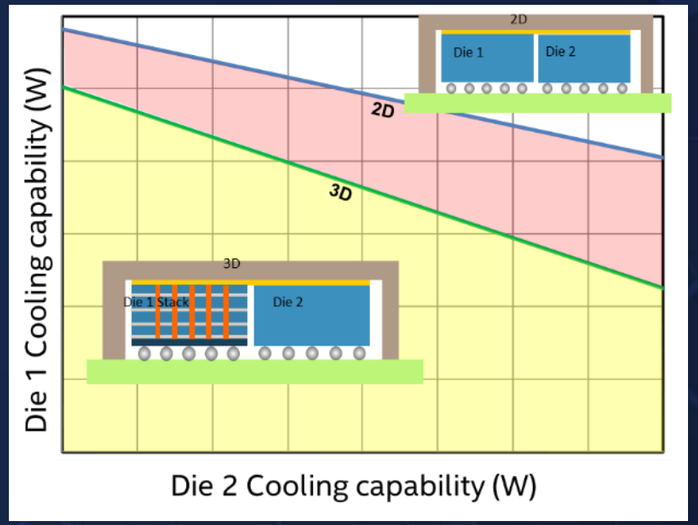


Thermal challenges driven by power, power density, and thermal cross-talk

- Need thermal co-design, improved TIMs + power/thermal management

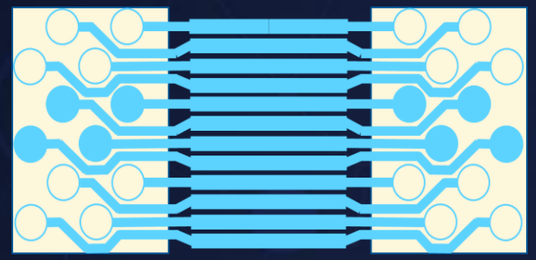


Local hotspot density increasing gen-o-gen; likely to hit thermal wall ahead of power delivery wall



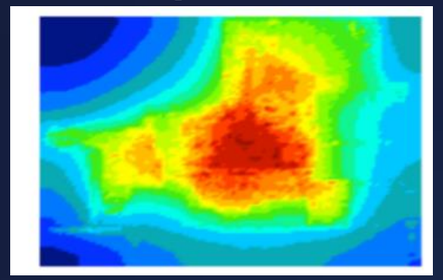
CHIPLET INTEROPERABILITY ENABLED BY SPECIFICATIONS AND TOOLS

Mechanical



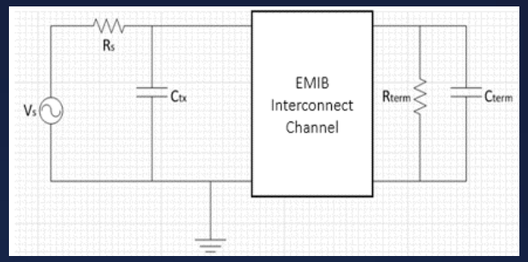
- Bump and wire sizes
- Bonding footprint
- xyz constraints

Power/Thermal



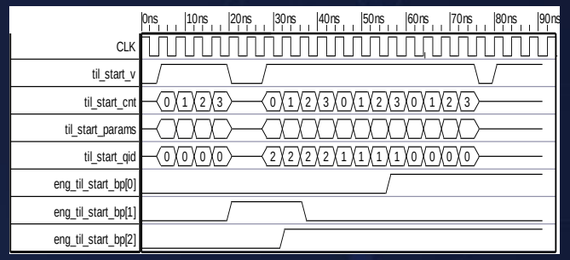
- Power & thermal modeling and cooling solutions

Electrical



- Power delivery
- Noise margin
- Capacitance

Functional



- Data/transaction specifications
- Management: power, security, debug, etc.
- Configuration & statistics
- Manufacturing test access

- Lower productization and NRE cost
- Industry standard test and DFX
- Functional safety, certification, and traceability
- Business model and supply chain enablement
- Easy to use Tools/Flows/Methods

.To minimize area/power/cost and support industry scale interoperability

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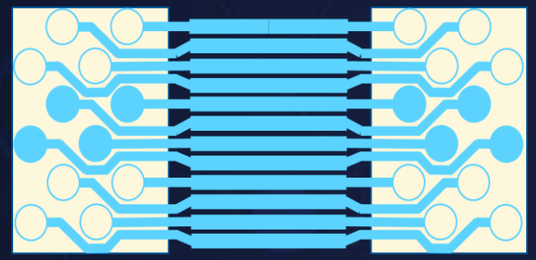

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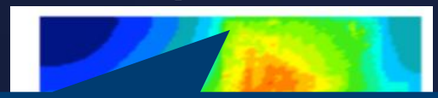

New IEEE 2416 standard for power modeling

- Power & thermal modeling and cooling solutions

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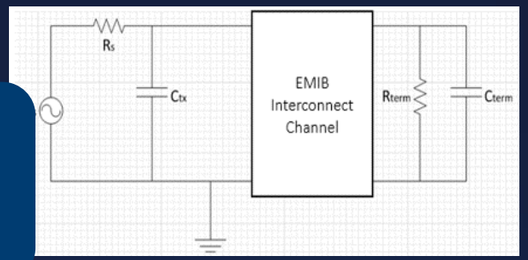

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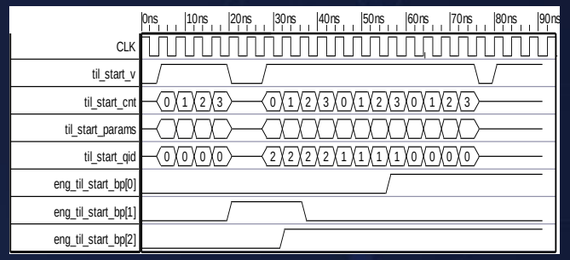

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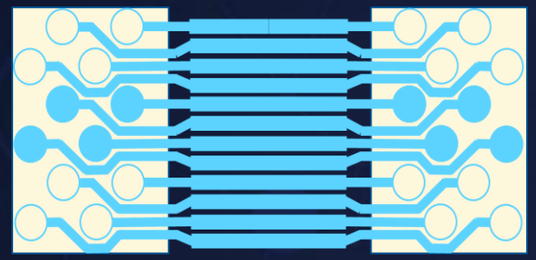

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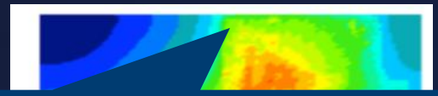

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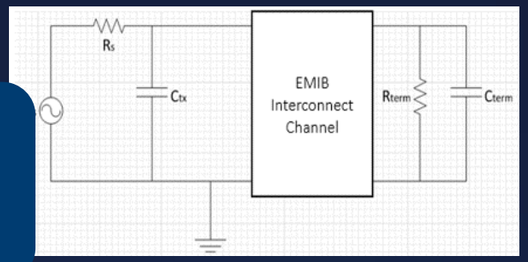

- Power delivery
- Noise margin
- Capacitance

Functional

New PIPE V5.2 support for configurable short reach PHY

- Data/transaction specifications
- Management: power, security, debug, etc.
- Configuration & statistics
- Manufacturing test access

- Lower productization and NRE cost
- Industry standard test and DFX
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POWER MODELING STANDARD IEEE 2416-2019

IEEE P2416 WG: ARM, Cadence, IBM, Intel, Si2

Si2 UPM WG: ANSYS, Cadence, Entasys, IBM, Intel, Thrace Systems

Standardized interoperable system-level power model

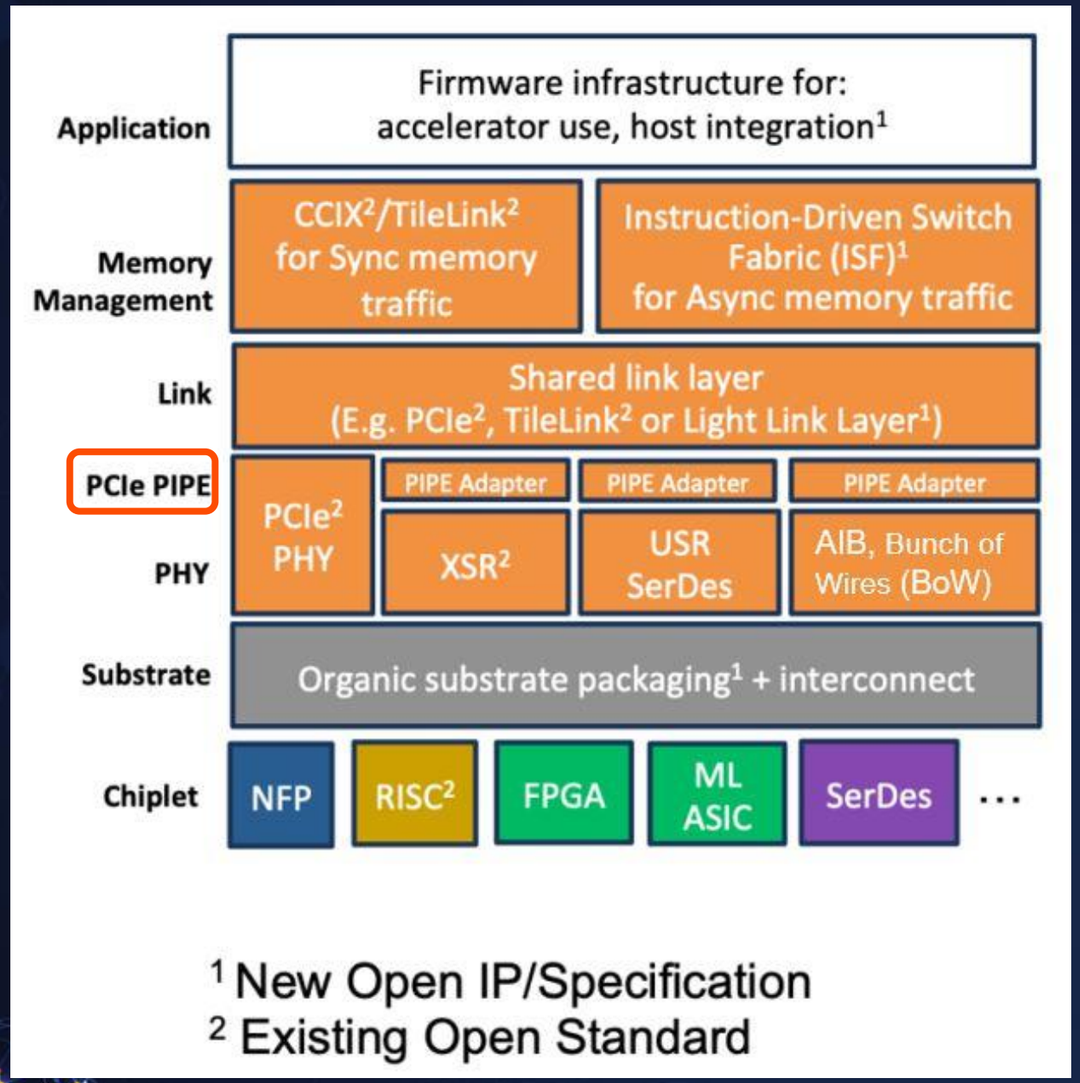
- Independent of voltage & temp
- Allows many different levels of abstraction from IP Block > chiplet > SOC/SIP
- Early insight into electro-thermal effects

Common modeling language targets 3 classes of users

- *Model producers*: those developing power models
- *Model consumers*: those using power models to estimate power
- *Tool developers*: those building EDA power modeling tools

Future: include static/dynamic thermal modeling & process variation

PIPE V5.2 SUPPORT FOR SHORT REACH APPLICATIONS



- Configurable Short Reach PHY (sec 2.6)
  - Potentially 50% active power reduction
  - Reduce power state transition times & reduce cost by moving from AC coupling to DC coupling
- Carry over board-level ecosystem
  - Same Si could be used for both board-level & package-level integration
  - Mature ecosystems for Si, validation, software, etc.
  - Multi-vendor interoperability
  - Supports PCIe, CXL, DMI, UPI, CCIX, SATA, USB3.x & DisplayPort

SUMMARY & CONCLUSION

PACKAGING IS A PLATFORM FOR INNOVATION, AGILITY, FLEXIBILITY

ADVANCED PACKAGING APPROACHING MONOLITHIC SOC

A DEMONSTRATED RANGE OF INTEGRATION SOLUTIONS

MORE TO BE DONE ON STANDARDS, TOOLS, AND BUSINESS MODELS TO BUILD THE FOUNDATION OF THE EMERGING CHIPLET ECOSYSTEM

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