Chiplet Data Exchange Service

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ODSA Meeting

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Consume. Collaborate. Contribute.

Problem Statement

Chiplet Selection

Designer need a number of design collaterals to make a choice of components for a given application and to complete a design. These include at minimum;

- Product Briefs
- Data Sheets
- PCB/Substrate Design Resources

With complicated chips, traditional PCB type design flows are limiting and will not easily scale. Also there are too many ways to describe chiplets.

Chiplet Design Data Exchange

There is no one standard way to express basic information: A standard format should be simple and usable across different tools

- Design Entry tools
- Layout tools
- Simulators (PI/SI, Thermal, Behavioral)
- Test

BUT There is a question of what info people are willing to share. Hence we did a survey.

Survey Question Overview

1. I can share what my chiplet's function is (i.e. a high-level description of what the chip does):
2. I can share the number and value of voltage rails:
3. I can share pin-by-pin functional information (i.e. EC table / AbsMax):
4. I can share the size (X and Y dimensions) of my chiplet:
5. I can share bump physicals (pitch, location, thickness, and tolerances) of my chiplet:
6. I can share height (Z dimension) of my chiplet:
7. I can share a heat map of my chiplet:
8. I can share what mechanisms I provide to test for chip functionality prior to assembly:
9. I can share what mechanisms I provide to test for chip functionality post assembly:
10. I can share my business model (wafer with known good die map vs. individual die or other):

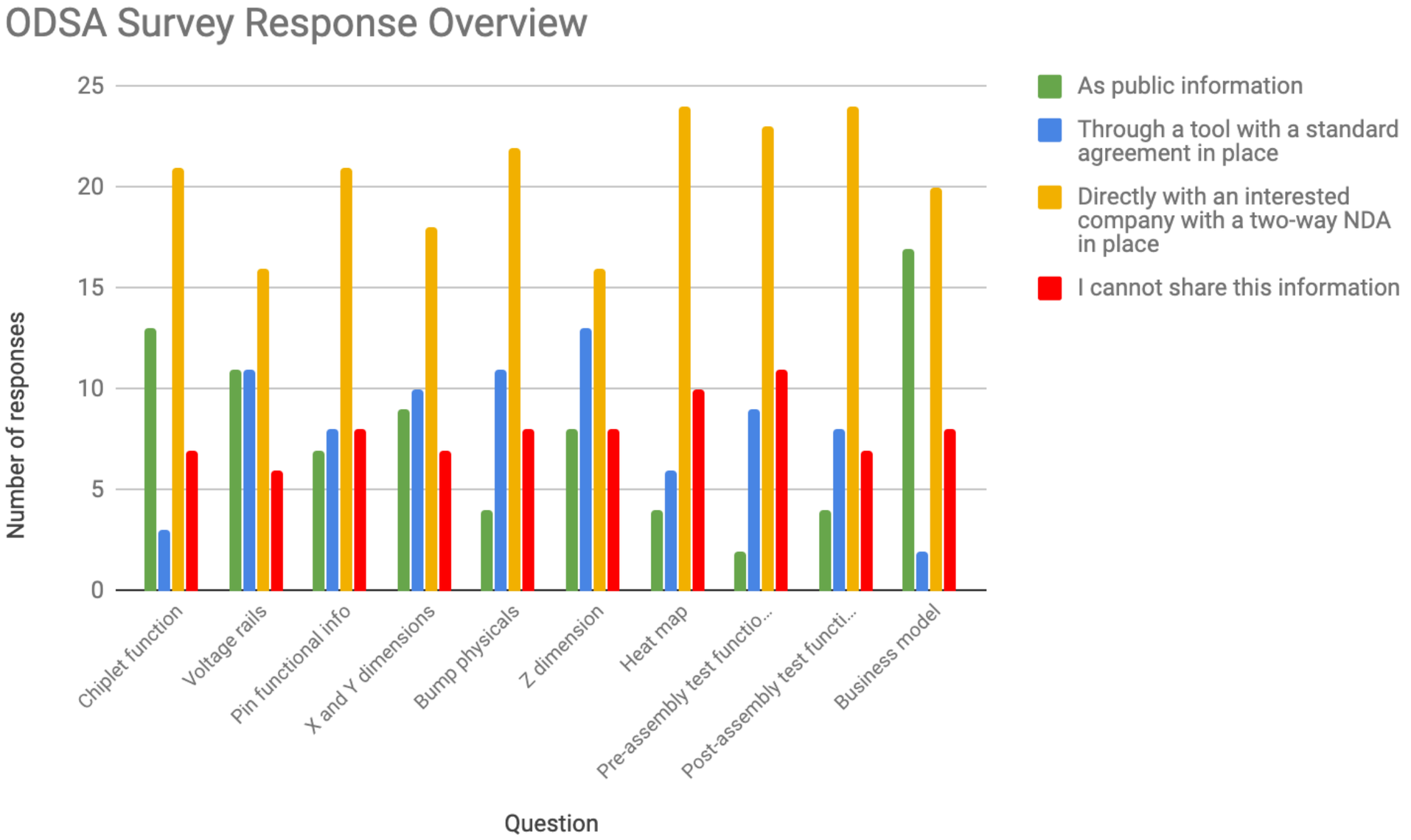
a) As public information
b) Through a tool with a standard agreement in place
c) Directly with an interested company with a two-way NDA in place
d) I cannot share this information

Survey Respondents: An Overview

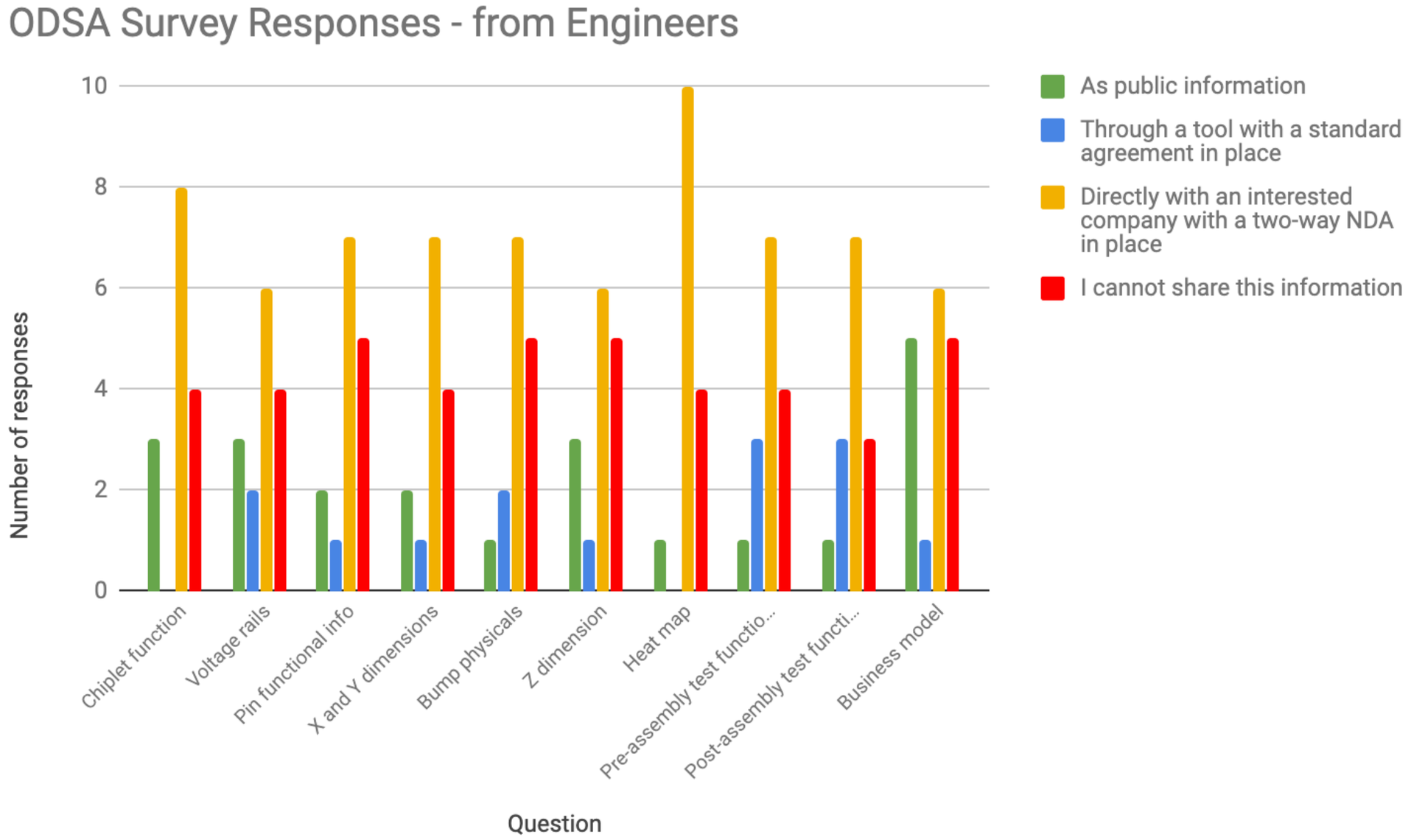
- 50 responses
- 38 familiar with ODSA and/or chiplets, 10 familiar with chips, 2 not familiar
- Job functions:

Architect	15	“Architects”
Executive Management	10	“Exec Mgmt, BD, & Mktg”
Business Development and Marketing	6	
Engineering Management	9	“Engineers”
Mechanical Engineer	3	
Electrical Engineer	4	
Hardware Engineer	1	
Cloud Provider	1	

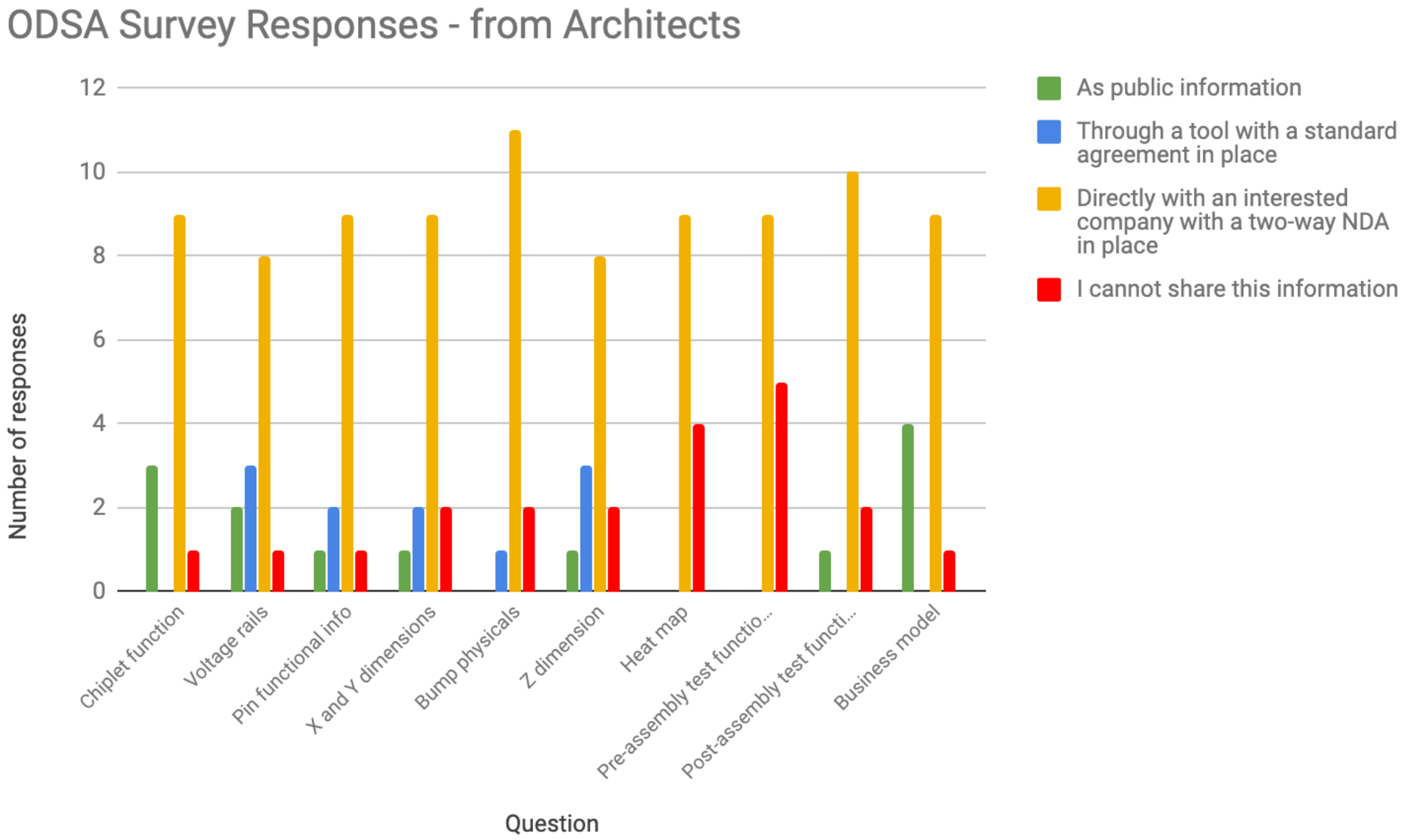
Survey Results: An Overview



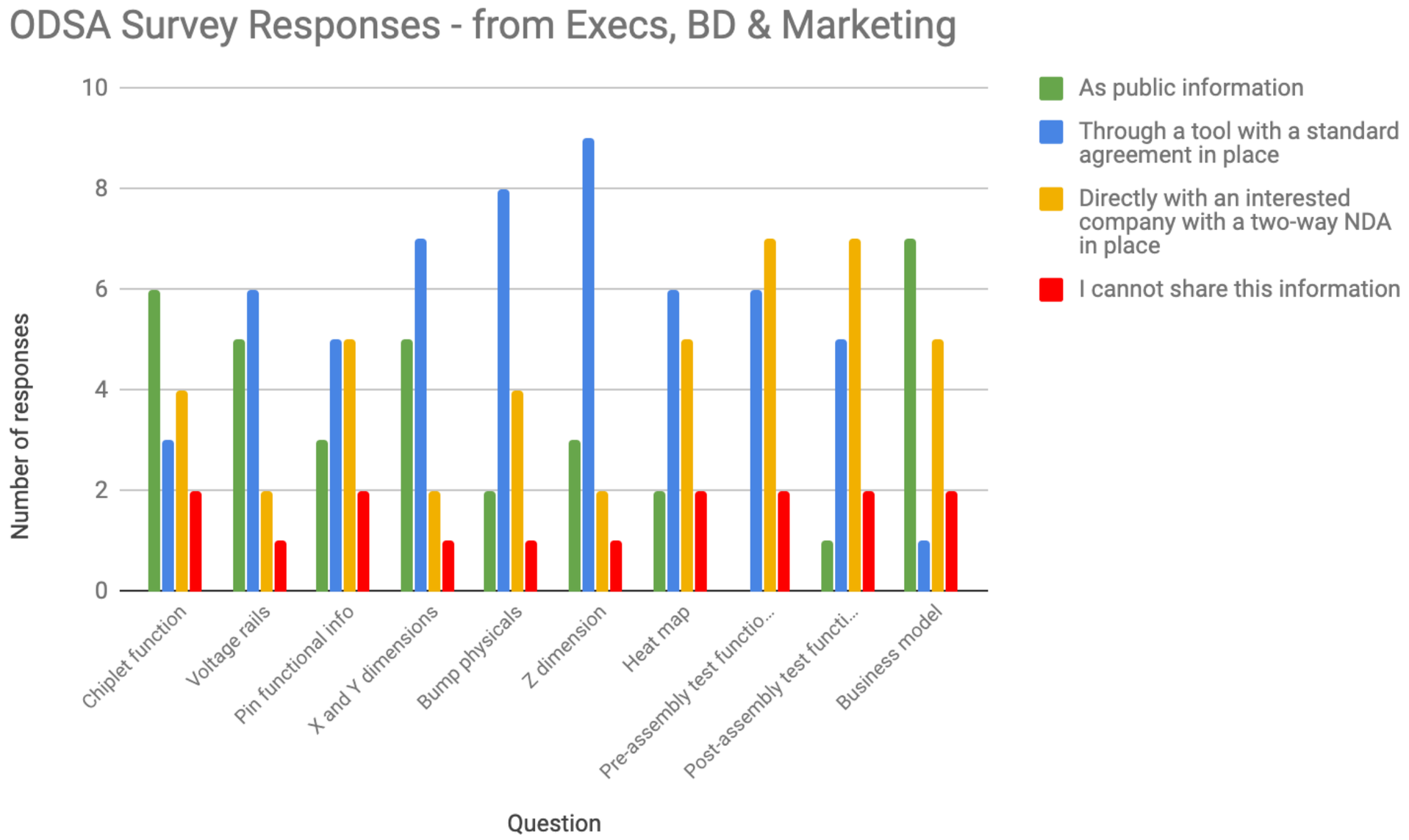
Survey Results: Engineers



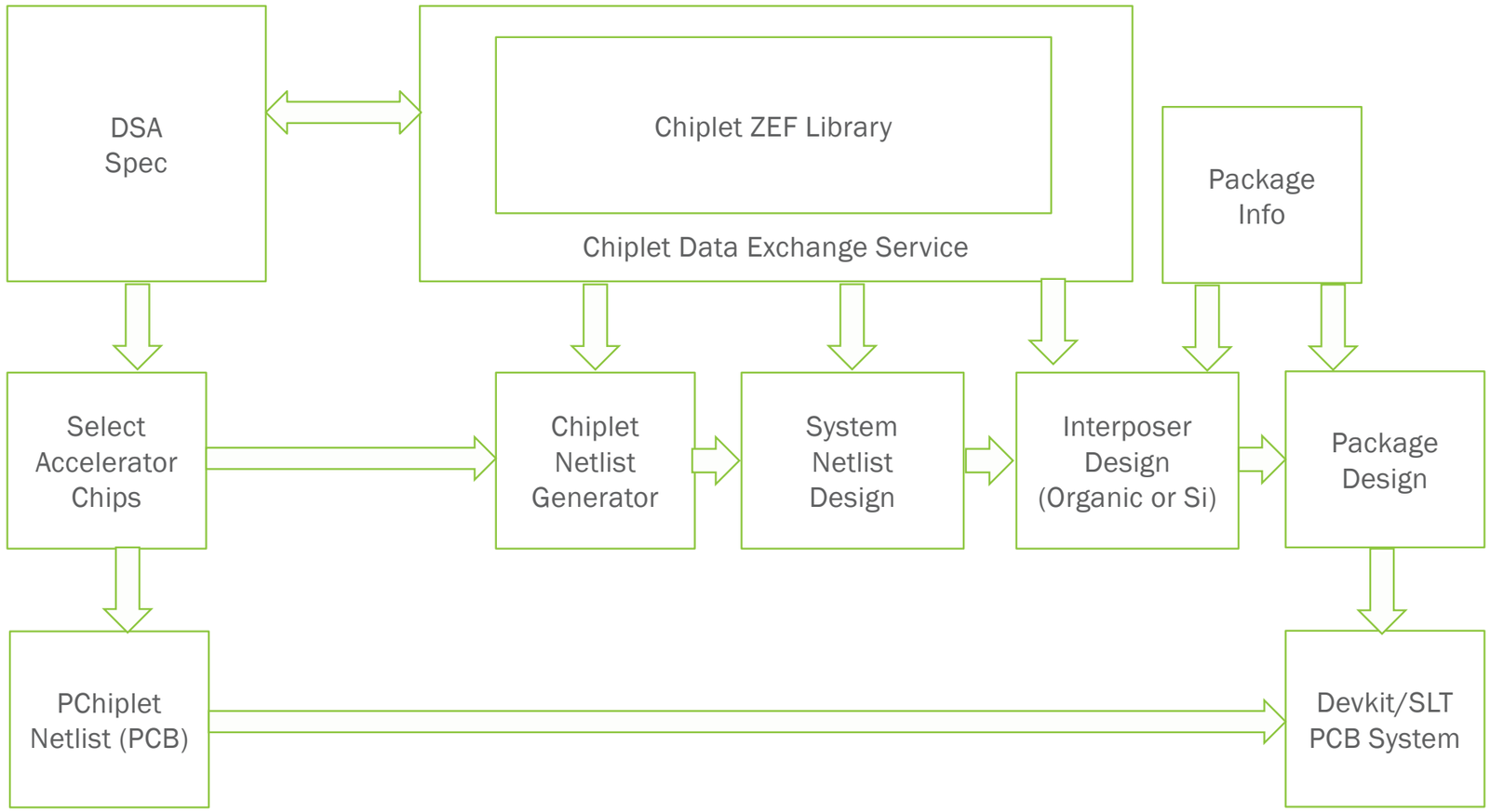
Survey Results: Architects



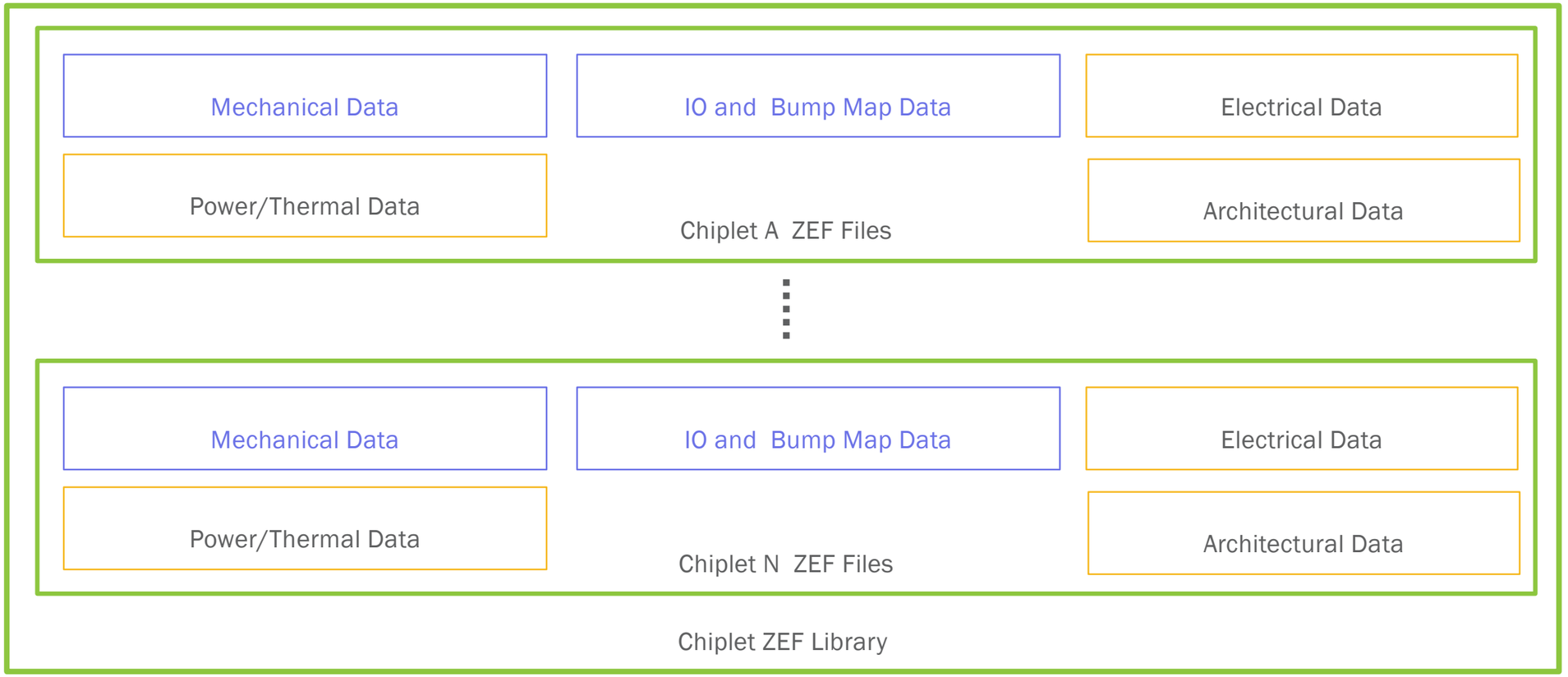
Survey Results: Execs, BD & Mktg



Chiplet Data Exchange Design Process



Chiplet Data Exchange Service



Through a tool with a standard agreement in place

Directly with an interested company with a two-way NDA in place

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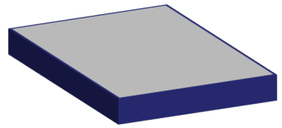
ZEF – Mechanical Format

The Data to be provided in a CSV format with a number of standardized variable names;

For Example Try Reading the following Chiplet

x	y	z
1280	1790	520



A More Complete Mechanical :
Reference, Part_value, MPN, Order_Number, Container, Pieces_per_unit, Name, Pkg_type, Pkg_IPC_code, SMT_compatible, Width_x, Width_tolerance, Length_y, Length_tolerance, Thickness_z, Thickness_tolerance, Count_IO, Bump_pitch, Bump_pitch_tol, Bump_dia, Bump_dia_tol, Bump_thickness, Bump_thickness_tol, Bump_material, Mold Material, Reflow Profile

More details at https://github.com/zglue/ZEF

Next Steps

- Further Develop Chiplet Data Exchange Service Concept
- Plan Meetings with leading IDM, Foundry and Packaging Companies – Review survey results
- Issue CDX template for providers and users to review/adopt

Backup

ZEF – IO Format

For Example Try Reading the following Chiplets

Pnum	Pname	Sig Type	IO Type	Diameter	X center	Y Center
A3	CS#	DI	BALL	0.2	0.3	0.4
B2	GND	V	BALL	0.2	0	0.2
C1	RESET#/SIO3	DIO	BALL	0.2	-0.3	0

A More Complete Mechanical :
IO_Name, IO_Reference, Signal_type, IO_mechanical_type, Populated, Solder_Type, Ball_dia, Ball_thickness, Land_dia, Land_x, Land_y, SMD_clearance, Center_x, Center_y, Signal_type, Singal_group, Netlist_name, Vdd, Gnd, Vmax, Vnom, Vmin, Imax, Inom, Imin, Pmax, Pnom, Pmin, Rmax, Rnom, Rmin, Lmax, Lnom, Lmin, Cmax, Cnom, Cmin, Tmax, Tnom, Tmin, Count_Modes, Mode_Name, Is_RF, Controlled_Impedance, ESD_type, Is_DFT, Overloade_num