

OPEN POSSIBILITIES.

DC-SCM 2.0 LVDS Tunneling Protocol & Interface (LTPI) Introduction



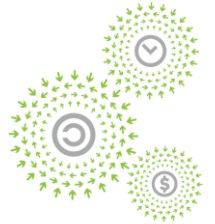
OCP
GLOBAL
SUMMIT

NOVEMBER 9-10, 2021

DC-SCM 2.0 LVDS Tunneling Protocol & Interface (LTPI) Introduction

John Leung, Principal Engineer, Intel
Kasper Wszolek, Principal Engineer, Intel
Yi (Roy) Zeng, Principal Engineer, Intel

OPEN POSSIBILITIES.



OPEN
PLATINUM™



Agenda

- Background
- LTPI Introduction
- Key features
- Call to Action



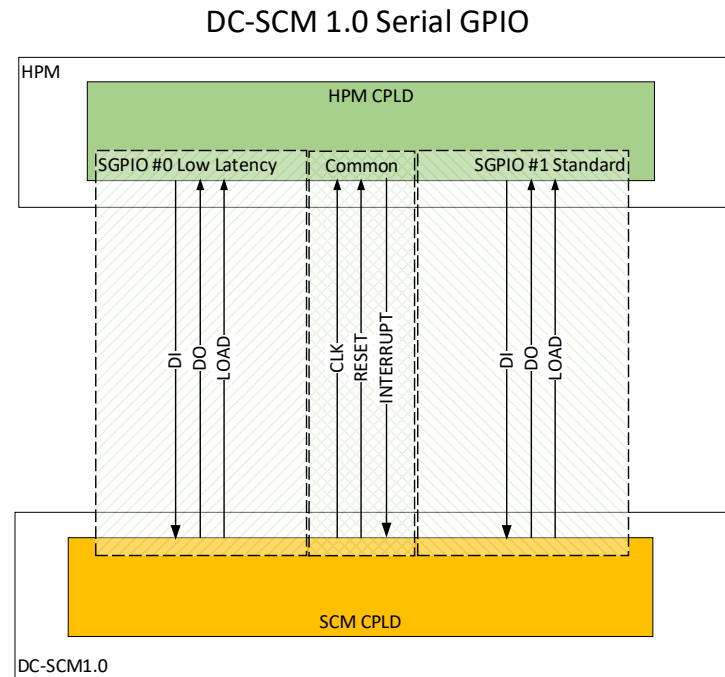
SERVER

OPEN POSSIBILITIES.



Background

- DC-SCM modular designs moves substantial part of server platform on a module (BMC, Root Of Trust, Front Panel, SPI Flashes & TPM)
- DC-SCM 1.0/2.0 SFF-TA1002 4C+ connector is limited to 168 pins and cannot accommodate all low speed and high pin count interfaces
- 2 x Serial GPIO (9 pins) interfaces are defined in DC-SCM 1.0 to tunnel GPIO signals between HPM platform and DC-SCM Module

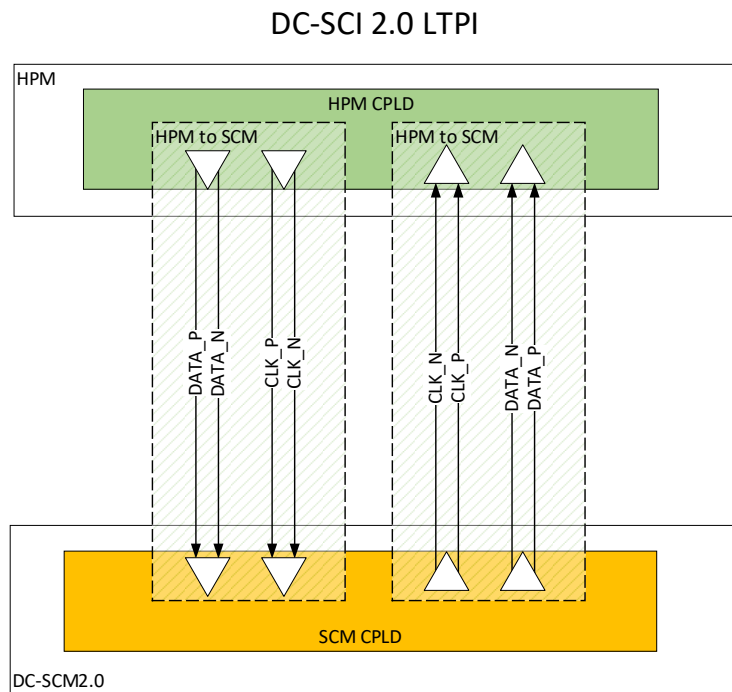


OPEN POSSIBILITIES.

LTPI Introduction

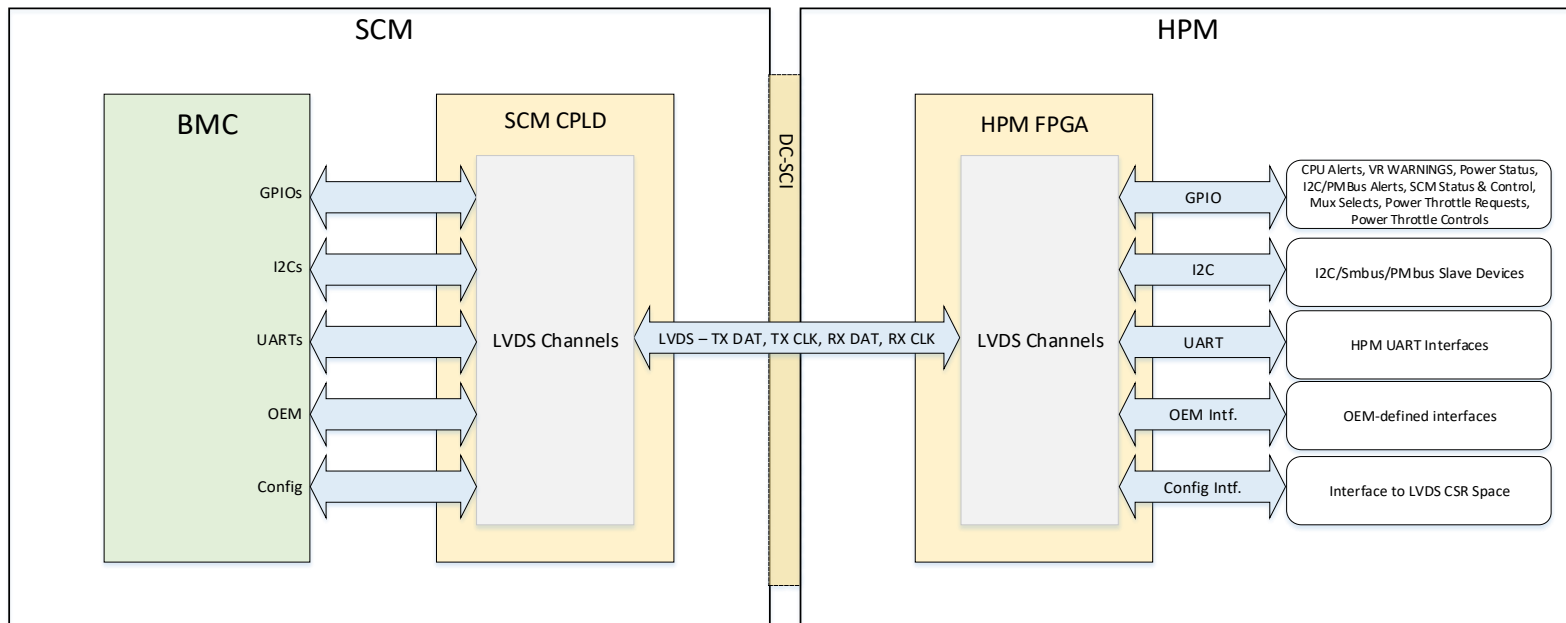
DC-SCM 2.0 LTPI:

- DC-SCM 2.0 introduces high-speed and scalable Low-voltage differential signaling Tunneling Protocol & Interface (LTPI)
- LTPI uses 4 differential links (8 pins) in place of 2 Serial GPIO interfaces from DC-SCM 1.0 and can be used to tunnel more than just GPIOs making room for DC-SCM evolution



OPEN POSSIBILITIES.

LTPI Overview



OPEN POSSIBILITIES.

Key features Re-cap

Key Features	Benefits and Value Add
LVDS I/O (Low-Voltage Differential Signaling)	<ul style="list-style-type: none">- Improved Signal Integrity and Bandwidth comparing to Single-ended- Supported by most of CPLD & FPGA
AC-coupling	<ul style="list-style-type: none">- Allows for multiple LVDS voltage standard use- Improved CPLD/FPGA interoperability
Multiple interfaces tunneling	<ul style="list-style-type: none">- Supports tunneling of more interfaces than just GPIO: SMBus/I2C, UART, Data Channel
High bandwidth capabilities	<ul style="list-style-type: none">- Reference designs running at 200Mbps- Latest FPGAs support LVDS at 1600 Mbps
Scalability & Flexibility	<ul style="list-style-type: none">- Specific designs can choose which interfaces are tunneled with LTPI- OEM Extensions can be added to LTPI as OEM channels- Data Channel allows for random access and data exchange between DC-SCM CPLD and HPM CPLD
Interoperability	<ul style="list-style-type: none">- Link training and capabilities exchange protocol defined- BMC controls the process of LTPI bring-up and configuration

OPEN POSSIBILITIES.



Call to Action

- Full LTPI Introduction on demand video is available on Virtual Summit Site
- Join us in Experience Center and Virtual EC to see the Demo of LTPI interface:
 - Intel Demo of LTPI Implementation on Intel Max10 CPLDs (Virtual EC only)
 - Lattice Demo of LTPI Implementation on Lattice MachXO3 FPGAs
- Provide feedback to OCP HW Management Module Subproject

Project Wiki with latest specification :

https://www.opencompute.org/wiki/Hardware_Management/Hardware_Management_Module

Mailing list: OCP-HWMgt-Module@OCP-All.groups.io

OPEN POSSIBILITIES.



Thank you!



NOVEMBER 9-10, 2021