DC-SCM 2.0 LVDS Tunneling Protocol & Interface (LTPI) Introduction
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Agenda

• Background
• LTPI Introduction
• Key features
• Call to Action
Background

- DC-SCM modular designs moves substantial part of server platform on a module (BMC, Root Of Trust, Front Panel, SPI Flashes & TPM)
- DC-SCM 1.0/2.0 SFF-TA1002 4C+ connector is limited to 168 pins and cannot accommodate all low speed and high pin count interfaces
- 2 x Serial GPIO (9 pins) interfaces are defined in DC-SCM 1.0 to tunnel GPIO signals between HPM platform and DC-SCM Module
**LTPI Introduction**

**DC-SCM 2.0 LTPI:**
- DC-SCM 2.0 introduces high-speed and scalable Low-voltage differential signaling Tunneling Protocol & Interface (LTPI)
- LTPI uses 4 differential links (8 pins) in place of 2 Serial GPIO interfaces from DC-SCM 1.0 and can be used to tunnel more than just GPIOs making room for DC-SCM evolution
LTPI Overview

**SCM**

- BMC
  - GPIOs
  - I2Cs
  - UARTs
  - OEM
  - Config

- SCM CPLD
  - LVDS Channels
  - LVDS – TX DAT, TX CLK, RX DAT, RX CLK

**HPM**

- HPM FPGA
  - GPIO
  - I2C
  - UART
  - OEM Intf.
  - Config Intf.
  - I2C/Smbus/PMbus Slave Devices
  - HPM UART Interfaces
  - OEM-defined interfaces
  - Interface to LVDS CSR Space

**CPU Alerts, VR WARNINGS, Power Status, I2C/PMBus Alerts, SCM Status & Control, Mux Selects, Power Throttle Requests, Power Throttle Controls**
## Key features Re-cap

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<tr>
<th>Key Features</th>
<th>Benefits and Value Add</th>
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<td><strong>LVDS I/O (Low-Voltage Differential Signaling)</strong></td>
<td>- Improved Signal Integrity and Bandwidth comparing to Single-ended&lt;br&gt; - Supported by most of CPLD &amp; FPGA</td>
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<td><strong>AC-coupling</strong></td>
<td>- Allows for multiple LVDS voltage standard use&lt;br&gt; - Improved CPLD/FPGA interoperability</td>
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<td><strong>Multiple interfaces tunneling</strong></td>
<td>- Supports tunneling of more interfaces than just GPIO: SMBus/I2C, UART, Data Channel</td>
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<td><strong>High bandwidth capabilities</strong></td>
<td>- Reference designs running at 200Mbps&lt;br&gt; - Latest FPGAs support LVDS at 1600 Mbps</td>
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<td><strong>Scalability &amp; Flexibility</strong></td>
<td>- Specific designs can choose which interfaces are tunneled with LTPI&lt;br&gt; - OEM Extensions can be added to LTPI as OEM channels&lt;br&gt; - Data Channel allows for random access and data exchange between DC-SCM CPLD and HPM CPLD</td>
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<td><strong>Interoperability</strong></td>
<td>- Link training and capabilities exchange protocol defined&lt;br&gt; - BMC controls the process of LTPI bring-up and configuration</td>
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Call to Action

• Full LTPI Introduction on demand video is available on Virtual Summit Site
• Join us in Experience Center and Virtual EC to see the Demo of LTPI interface:
  • Intel Demo of LTPI Implementation on Intel Max10 CPLDs (Virtual EC only)
  • Lattice Demo of LTPI Implementation on Lattice MachXO3 FPGAs
• Provide feedback to OCP HW Management Module Subproject

Project Wiki with latest specification:
https://www.opencompute.org/wiki/Hardware_Management/Hardware_Management_Module

Mailing list: OCP-HWMgt-Module@OCP-All.groups.io
Thank you!