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OMI, The Path to High Bandwidth, High Capacity Near Memory
OMI, The Path to High Bandwidth, High Capacity Near Memory
Jim Handy, Objective Analysis, https://objective-analysis.com
Preface: Near Memory vs. Far Memory

- **Near Memory** (1-10 ns, ~50 ns, <10 ns)
- **Far Memory** (150-500 ns)

Objective Analysis

- 3D XPoint
- SSD
- HDD
- Tape
- DRAM

Bandwidth vs. Price per Gigabyte

- OpenCAPI
- Inception
- CXL
- CCIX
- GenZ

HIGH PERFORMANCE COMPUTING

SERVER
Preface: Near Memory vs. Far Memory

- **Near Memory**:
  - L1: ~1ns
  - L2: 3-5ns
  - L3: ~50ns

- **Far Memory**:
  - DDR, HBM, OMI

- **Objective Analysis**

- **Bandwidth (MB/s)**
- **Price per Gigabyte**
Outline

• More Cores Need More Near Memory Bandwidth
• Today’s Problems Need Larger and Faster Near Memories
• Three Alternatives DDR, HBM, & OMI
• What Is a DDIMM?
• Supporting a Mix of Near Memories
• Conclusions

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Processor Trends Drive Near Memory Demands

- Clock speeds have stagnated
- Core count is skyrocketing

Data Source: Karl Rupp - https://www.karlrupp.net/2015/06/40-years-of-microprocessor-trend-data/
Processor Trends Drive Near Memory Demands

Net Result: Memory Bandwidth Requirements Are Ballooning!

Data Source: Karl Rupp - https://www.karlrupp.net/2015/06/40-years-of-microprocessor-trend-data/
Increasing Near Memory Bandwidth

• Improve the memory interface
  • DDR, DDR2, DDR3, DDR4, DDR5
• Increase the bus clock speed
  • 1600, 1866, 2133, 2400, 2666, 2933, 3200
  • But latency doesn’t change as clock speed increases
  • Higher clock speeds reduce DIMMs per channel
• Add Memory Channels
More Memory Channels Means More Processor Die Cost & Power

Each LRDIMM channel requires 152 processor pins
72 data bits + 18 address bits + 36 strobes + 26 command/other bits
6 Channels = 912 pins
8 Channels = 1,216 pins
The most expensive real estate in the system
Fast I/O is a power hog
Capacitance is the culprit!

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Three Near Memory Options

DDDR4
- Mainstream & inexpensive

HBM2E
- Costly, but fast
- 1,000-bit bus!

OMI
- Introduces SerDes into data path
- Supports high bandwidth and large memory capacities
OMI & IBM’s POWER10 CPU

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POWER10 Stats

Sixteen OMI channels
256 GB capacity per channel
1TB/s total memory bandwidth (read + write)
64GB/s per OMI channel
2.2mm² die area per channel
29.6GB/s/mm²

Nearly matches HBM
OMI DDIMM

Serial differential signaling
  ¼ the pins of DDR
  HBM-like bandwidth

Moves DRAM signaling away from main board, onto DDIMM
  Reduces processor’s I/O power
  Low latency penalty <4ns

Requires a controller
  Replaces LRDIMM buffers
  Processor no longer tied to one interface (DDR4) or one memory type (DRAM)

30mm² die area
  Can do on-DIMM processing (ECC, encryption…)

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Other Possibilities

- DDR4
- DDR5
- LPDDR
- XPoint
- MRAM
- ReRAM
- FRAM
- NRAM

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Near HBM Bandwidth at >DDR Capacities
Conclusions

Near Memory needs more bandwidth
Near Memory needs larger capacities
More Memory → DDR, Faster Speeds → HBM, Both → OMI
Near-HBM speeds at larger-than-DDR capacities
OMI can support a mix of Near Memory types
Call to Action

Visit the OMI Booth on the OCP Exhibit Floor

Consider adopting OMI as your near memory interface during your next processor design to get a low latency, high bandwidth and high capacity solution.
References

CXL Consortium, Introduction to Compute Express Link (CXL), 2019 Hot Interconnects.
Karl Rupp - https://www.karlrupp.net/2015/06/40-years-of-microprocessor-trend-data/
https://github.com/karlrupp/microprocessor-trend-data/blob/master/LICENSE.txt
Thank you!