Capacitor Array Block (Supercap) for Enhanced Power Delivery in High Power AI Applications

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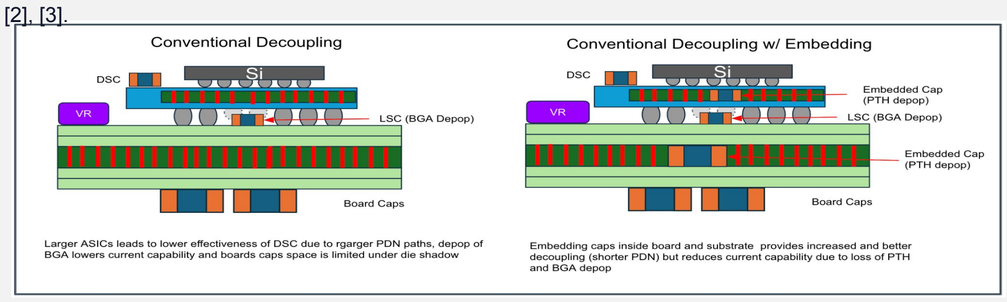
ABSTRACT

AI's growing computational needs strain power delivery (PDN) for high-frequency switching in processing cores. Reduced core voltage and increased current demands make effective PDN inductance a critical bottleneck, causing voltage droop and limiting stable operating frequency [1]. Embedding capacitors improves PDN but traditional single-side via connections limit PTHs. The proposed solution offers three key innovations:

1) Manufacturing method for dual-side MLCC connections to eliminate PTH loss;
2) Pre-embedded MLCC capacitor block with dual-side connections for easy PCB/substrate integration;
3) multi-faceted embedding topologies to improve 1st and 2nd order droops (demonstrated on PCB).

INTRODUCTION

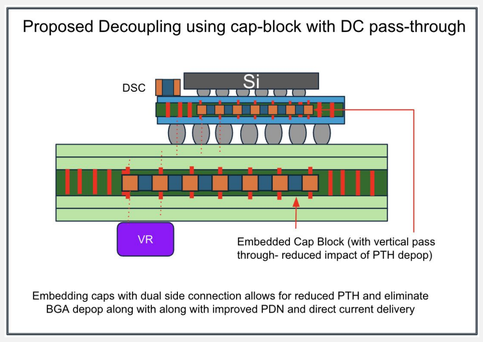
Conventional decoupling utilizes the core and build-up (BU) layers for current pass-throughs (PTHs) and structural support. This area can be better used to improve system functionality and PDN by embedding capacitors (MLCCs or Si caps). Past efforts, though effective (Si caps in substrate, MLCC in board), typically used single-side via connections from the top, resulting in PTH loss in embedded regions. While these concepts exist, proven implementation has been difficult. Kitamura et al. [5] showed similar architectures with lower density AI arrays, and Y. Min et al. [1] explored MLCC arrays with single-sided connections. Embedded capacitors have demonstrated better PDN and transient performance compared to backside SMT capacitors [2], [3].



THE NOVEL SOLUTION

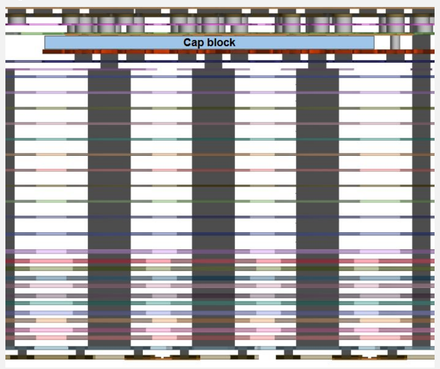
This work proposes a novel high-density capacitor block — the "Supercap" — featuring dual-side connections for embedding within the substrate or module board of high-power AI chips.

The Supercap preserves PTH current-carrying capability through vertical pass-through for currents, achieving capacitance densities >15 µF/mm² in components <800 µm high — critical for scaling AI performance at high powers and transient requirements.

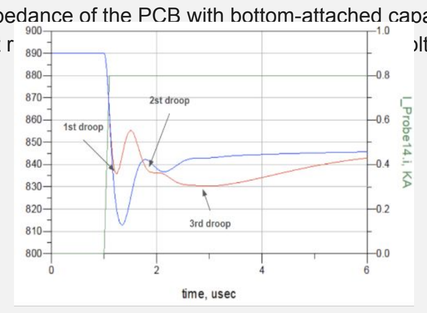


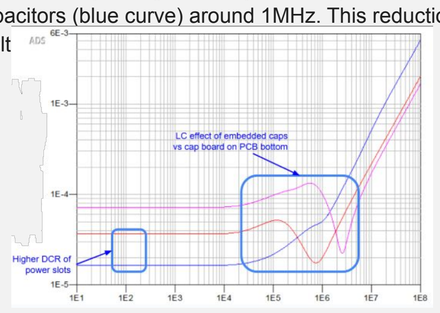
EMBEDDING TOPOLOGY & PDN IMPROVEMENT

While many embedding architectures are possible, we envision using these capacitor block components to be embedded inside of PCBs and/or substrates to provide efficient decoupling in the mid and high frequency regions. In our previous work [4], we demonstrated successful embedding of a large capacitor array inside of a board (in build-up layers) to improve the PDN response of the system (Figure). This study demonstrated successful dual side connections on a prefabricated capacitor array.



Simulations revealed that relocating capacitors from the backside of the PCB to an embedded configuration within the PCB significantly enhances the transient response, resulting in a 23mV improvement during the initial voltage droop. The observed degradation in the second and third voltage droops is attributable to the initial selection of the PCB embedding method. Detailed explanations of these results were presented at Designcon 2026 [4]. The red curve, representing the PCB with embedded capacitors, exhibits superior LC resonance characteristics, yielding a notably lower impedance of 20µΩ compared to the 50µΩ impedance of the PCB with bottom-attached capacitors (blue curve) around 1MHz. This reduction is beneficial for the transient r olt

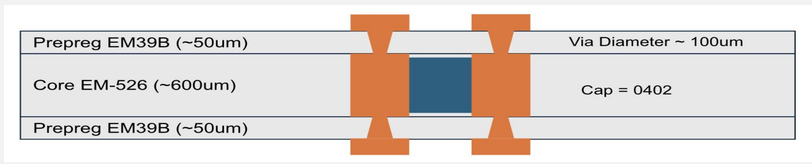




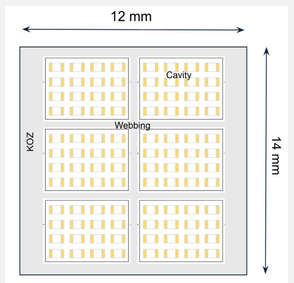
SUPERCAP STRUCTURE

Supercap in this context is defined as a standalone capacitor block component which is an array of MLCCs that are pre-embedded into a substrate with or without additional routing. This component acts as a giant capacitor but with the ability to have vertical pass-through connections (PTH type functionality) through the component to allow for vertical current hookups to VR and ASIC. The capacitors in the block are independent of each other but can be merged in parallel using additional build-up layers thus providing the ability to use the supercap block for multiple voltages as per the design. A simple supercap schematically would look something like below:

Initial test vehicle design focussed on using 22uf , 0402 Copper terminated caps in the supercap component. The cap "z" height was approximately 600 um. The unit size was set at 12 x 14mm, with a target thickness of less than 800um.

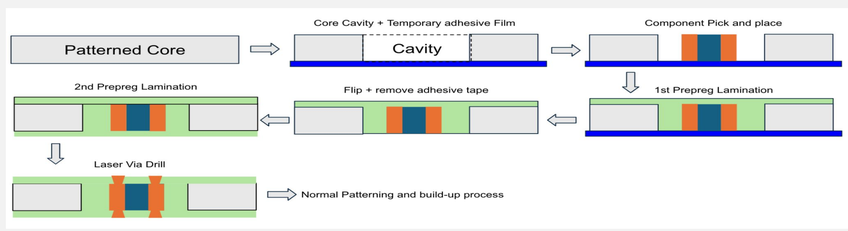


Supercap Construction



PROCESS DEVELOPMENT

A typical capacitor embedding flow is shown below. The fabrication starts with a patterned core of a substrate. A cavity is then cut or milled using a mechanical router or laser drilling process. The cavity size is chosen to accommodate the number of capacitors chosen to be embedded. The cavity size has to account for various dimensional tolerances like capacitor size, spacing and cavity edge component spacing. Additionally the empty regions after cap placement have to be managed for proper resin filling. After cavity creation, an adhesive film is attached to one side of the core. This provides a flat sticky surface for components to attach to to avoid component movement during resin fill. Components are then placed inside the cavity per design. Subsequently, prepreg with enough resin content and appropriate thickness is then laminated onto one side of the core. The resin flows into the cavities to fill the surrounding space around the cavity. This is followed by removal of the adhesive tape and second lamination on the backside. This creates a structure where a capas are embedded within the layers of prepreg and laser via drilling can then be performed on both sides to land a via (or multiple vias) connection on each of the terminals of the caps and the rest of the core layer. This can then be followed by a normal build up process that can be used to either create pads individually for the caps or merge various caps to serve various voltage rails.

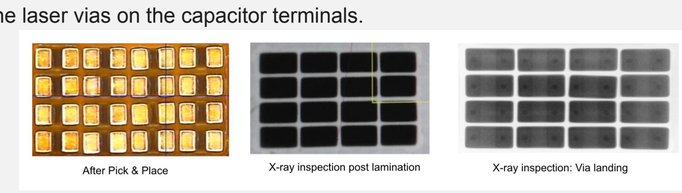


Key design parameters: cavity size, number of units per cavity, capacitor spacing, webbing size, edge exclusion/keep-out zone (KOZ). Multiple DOE variations optimized these parameters.

Manufacturing challenges addressed: pick-and-place accuracy, component displacement during lamination, incomplete resin fill, component height tolerance, laser via accuracy, and dual-sided via reliability.

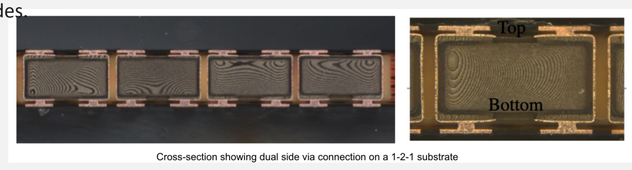
EXPERIMENTAL RESULTS

A series of experiments was performed to optimize various parameters—specifically cavity size, cavity design, component spacing, webbing size, adhesive tape selection and lamination conditions—to achieve optimal component placement accuracy both before and after the lamination process. Furthermore, parameters required meticulous tuning to guarantee complete resin fill and the absence of voids. Finally, the laser drilling recipe necessitated optimization to ensure accurate via registration in the x-y plane and to establish a robust electrical connection with the capacitor terminals (a challenge often complicated by inherent variations in capacitor height that impact laser drilling success). Following these multiple rounds of optimizations, the observed results confirmed accurate capacitor placement, the absence of component short circuits, and precise landing of the laser vias on the capacitor terminals.



After Pick & Place | X-ray inspection post lamination | X-ray inspection: Via landing

A cross-section analysis shows that vias made strong connections with the cap terminal from both sides.



Cross-section showing dual side via connection on a 1-2-1 substrate

- >4,500 components embedded and tested — 100% open-short yield
- All capacitances within specification
- Survived 20× reflow at 260°C peak and thermal stress at 288°C for 5 cycles
- No open/short failures or delaminations observed
- Strip warpage <1 mm for 54 × 60 mm strip; projected unit warpage <100 µm

CONCLUSION & REFERENCES

The integration of capacitors within Printed Circuit Boards (PCBs) and substrates offers the potential for substantial improvements in the power performance of high-power, high-current AI accelerators. Conventionally, embedding Multi-Layer Ceramic Capacitors (MLCCs) necessitates the removal of Plated Through Holes (PTHs) or power paths inside the substrates or PCBs, which consequently diminishes the substrate's or PCB's current carrying capacity. In response to this limitation, a novel integration methodology has been developed and its feasibility demonstrated. This method facilitates vertical passthrough for currents, thereby mitigating the typical loss of PTH current carrying capability. Reliable fabrication of large capacitor blocks (supercap) made of numerous MLCCs has been demonstrated which can yield capacitance densities upward of 15uf/mm2 in less than 800um high components. These prefabricated supercaps can be used in various decoupling locations inside an IC substrate or PCB to provide decoupling at various frequencies. Applications of these embedded dual-sided supercaps can extend to other applications such as mobile and vertical power delivery modules. While preliminary stress testing of these structures has yielded encouraging data, formal reliability testing encompassing both the components and their integration in final embedded applications has been planned to validate the scalability of this solution.

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[4] Louie Lu, Granthana Rangaswamy, Danny Singh, Greg Link, "Embedding of Capacitor Blocks within PCB for AI Accelerator," 2026 DesignCon Presentation
[5] T. Kitamura, T. Furukawa, S. Yamada, K. Himeda and A. Yamamoto, "Extremely Advanced Substrate as an integrated Package Solution (iPaS) for Next Generation High Performance Computing (HPC) applications," 2024 IEEE 74th Electronic Components and Technology Conference (ECTC), Denver, CO, USA, 2024, pp. 2053-2057, doi: 10.1109/ECTC51529.2024.00350. keywords: {Regulators;Power supplies;High performance computing;Capacitors;Capacitance;Topology;Polymers;power delivery network;embedded substrate;vertical power delivery;integrated voltage regulator},