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ODSA Proof of Concept (POC)

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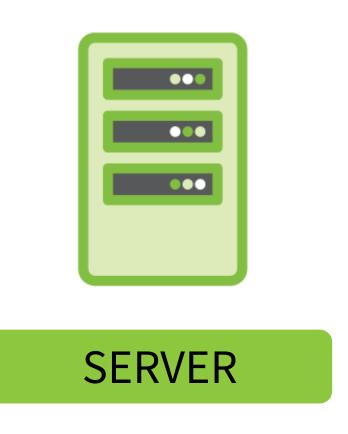


Big Picture

- **Vision:** ODSA success is an open marketplace where people offer their chiplets, and those chiplets have common interfaces to interoperate
- **Mission:** ODSA's role is to define and prove several aspects of the concept to enable companies to be willing to make investments for future multi-party chiplet products with common interfaces
- **Actions:** ODSA's POCs is to kick start the process
 - Tackle the chicken-and-egg problem by showing companies willing to make incrementally larger investments towards interoperable parts
 - Generate proof points to reduce resistance to making first real products (Making commercial products is beyond the scope of ODSA)

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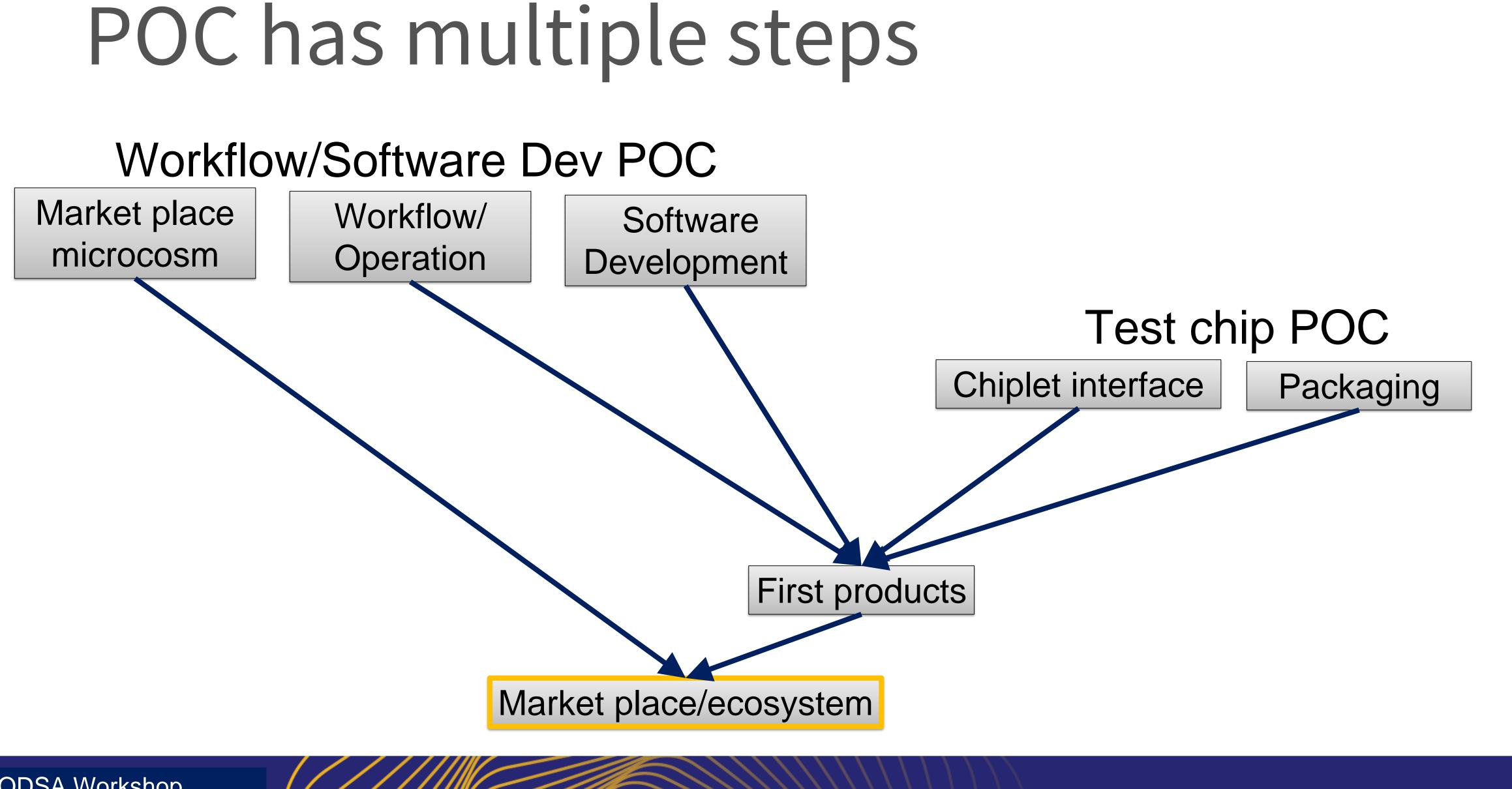
Workshops Summits

Multiple dimensions of POC effort

- Operations
 - Force information sharing at a bare die-level
 - Exposing issues of sharing sensitive business metrics
 - Validate risk and value sharing models
- Architectural
 - Validate interfaces protocols
 - Evaluate performance issues
 - Develop software programming models
- Work flow
 - Yield and cost modeling
 - Explore chiplet integration and packaging
 - Validate power distribution
 - Develop high-speed I/O solutions

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Objectives of Workflow POC

- Pathfinding with example workflow across companies and model for market place
 - Reusable cross-company workflow
 - Faster path in future for someone to build a domain-specific multi-chiplet solution
- Bootstrapping the system by building something tangible
 - Demonstrate commitment from all partners
 - Demonstrate credibility as a group
- Inspire by building accelerator (HW+SW) with contemporary performance
 - Need to attract end users
 - Show a path to real product

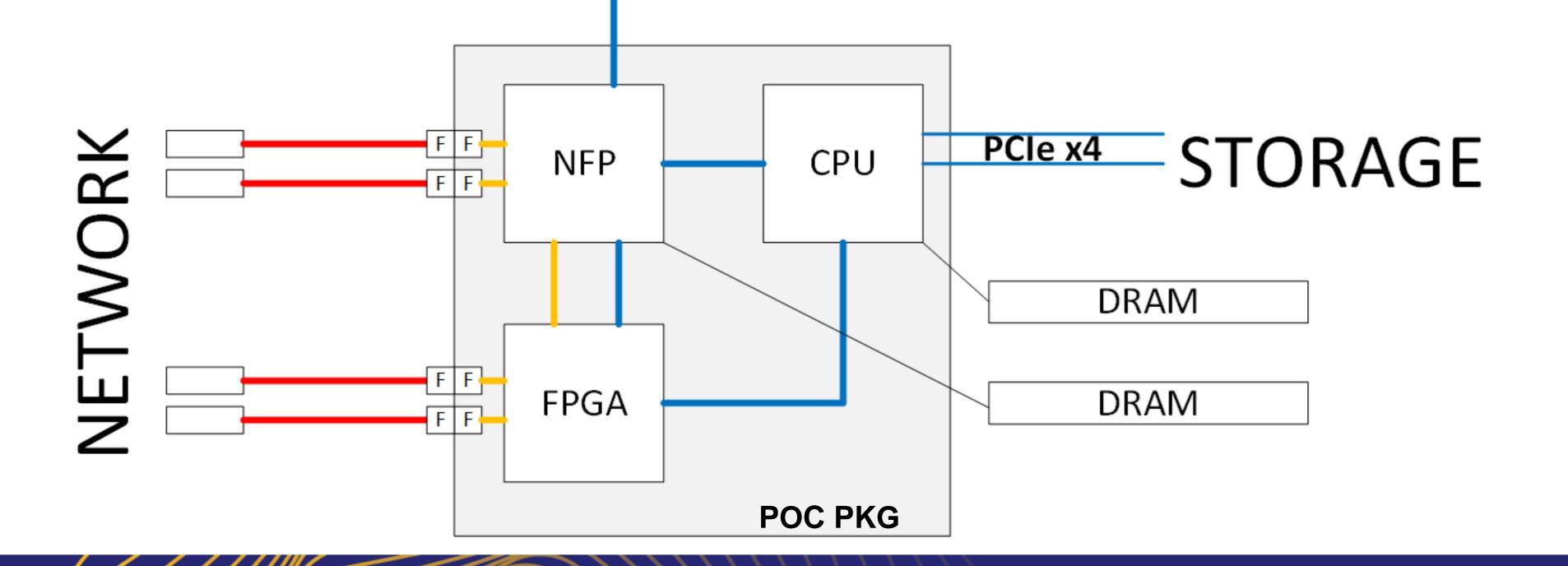
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Workflow POC First Thought

40G Ethernet copper — 40G Ethernet optical — X8 PCIe G3 (64Gbps) — HOST



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Working with legacy chips/interfaces

- **Explore** Operations
 - Working together
 - Sharing information
- **Building Something**
 - Making it real
 - Credible
- Create a microcosm for a chiplet market place
 - "Chiplet" suppliers
 - "Chiplet" integrators
 - Software suppliers
 - System builders

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- Engineering challenges **NOT** addressed by first POC (will be addressed with future test chips)
 - Validate new interface for chiplets
 - Packaging and board challenges of new generation of chiplets





PChiplet (pronounced "Pichlet")

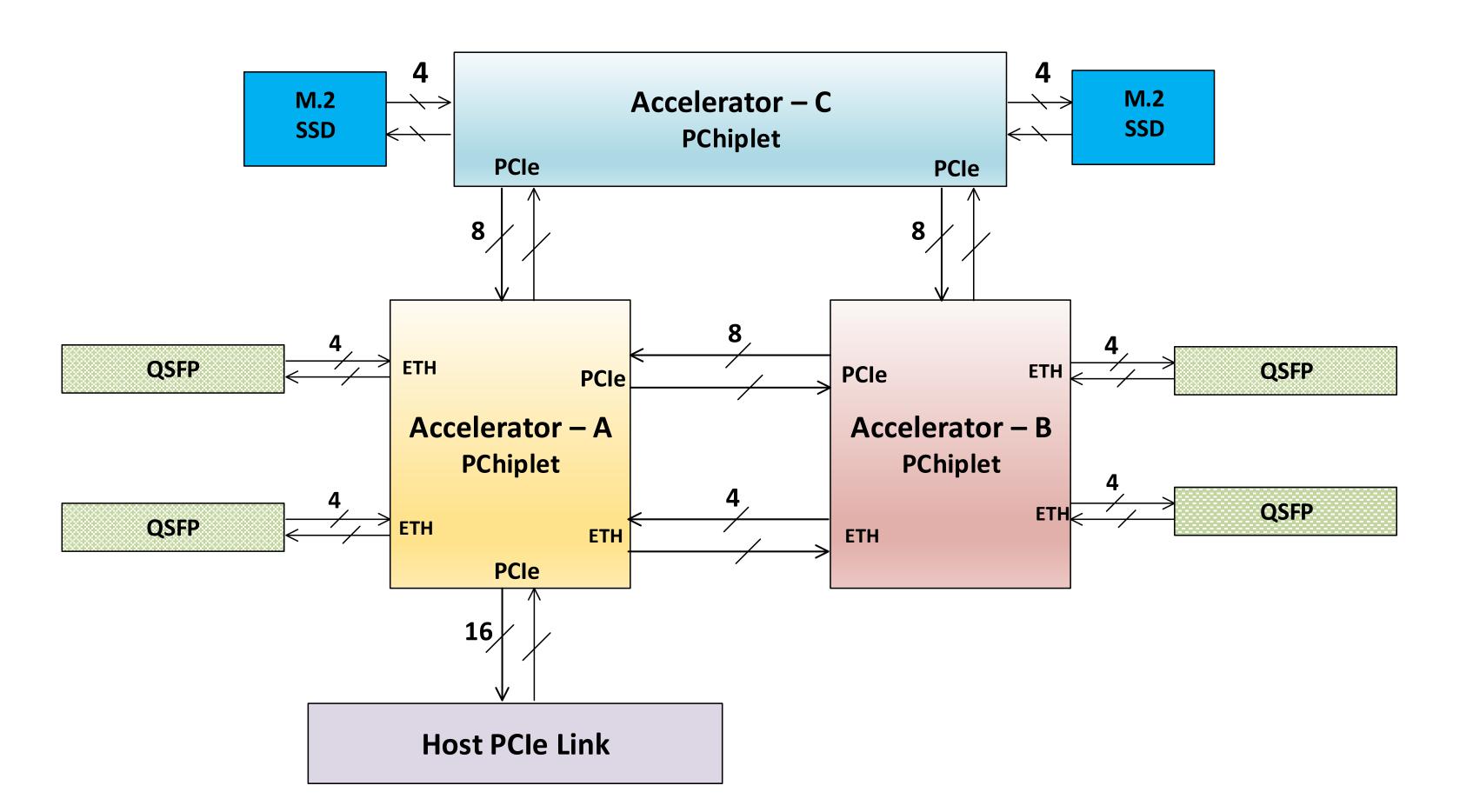
- Innovative way to take a first step
- A small PCB analogy of a chiplet
- A large PCB analogy of a substrate and package

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Workflow POC Platform Architecture

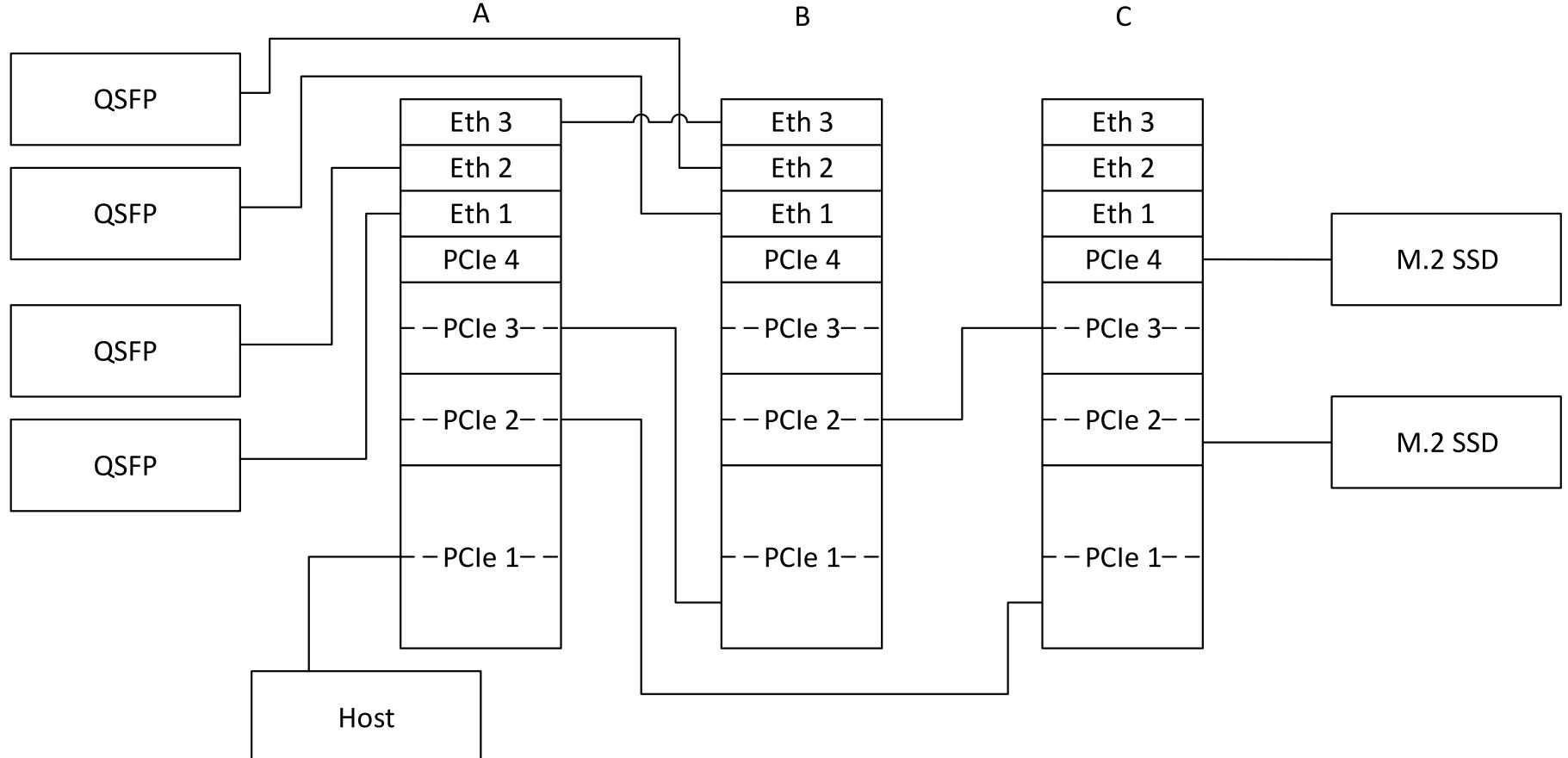


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Supports multiple configurations



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First PChiplets

Port	Netronome NFP	Achro		
Ethernet 3	YES	YES		
Ethernet 2	YES	YES		
Ethernet 1	YES	YES		
PCIe 4 x4	NO	NO		
PCIe 3 x8	YES x8	NO		
PCIe 2 x8	YES x8	YES x		
PCIe 1 x16	YES x8 only	YES x		

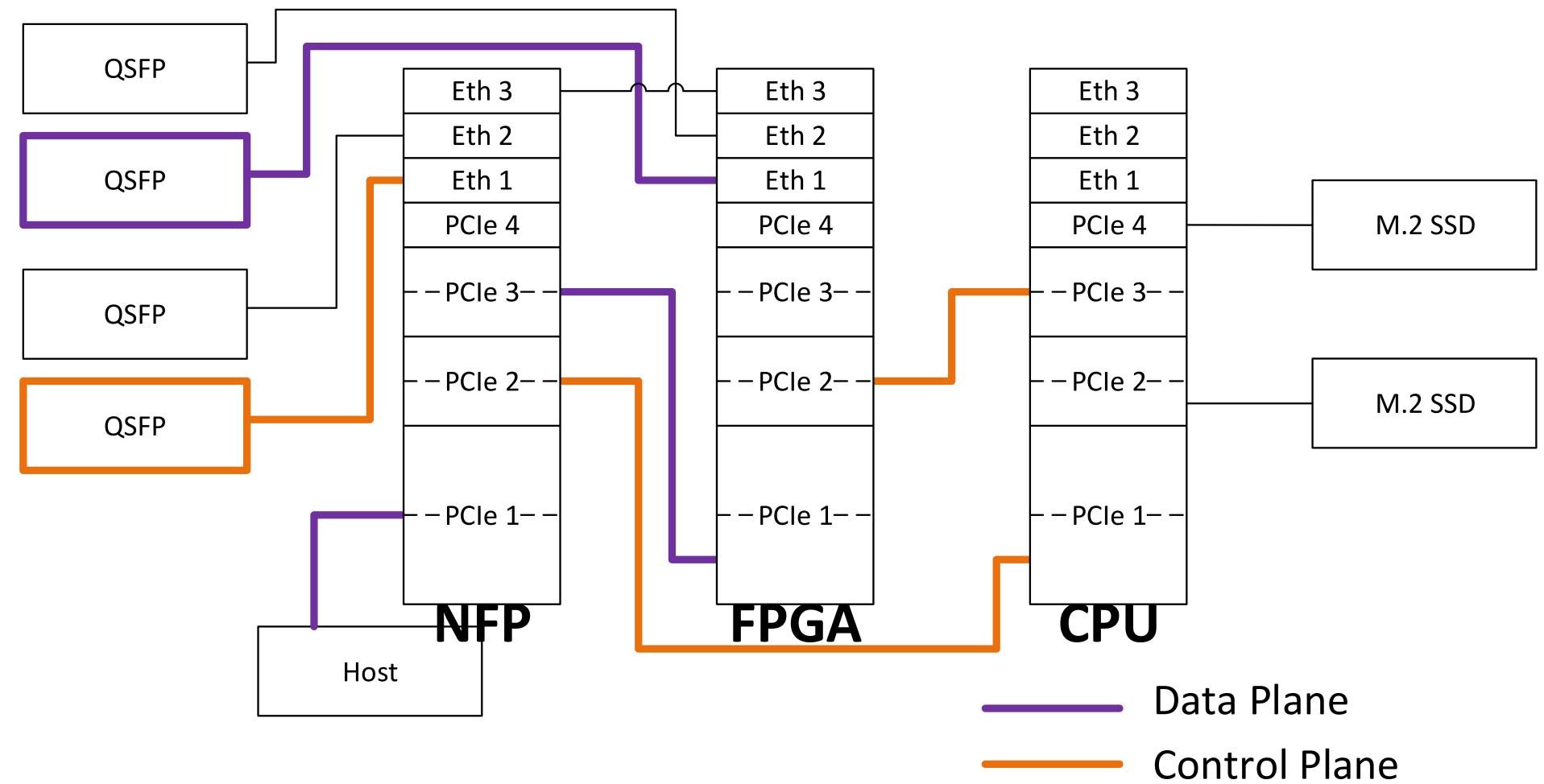
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NXP CPU onix FPGA **SSD** Jumper NO NO YES Jumper YES x4 Jumper YES x4 only Jumper **8** YES x4 only YES x8 x8 only



Example: Smart NIC bump-in-wire

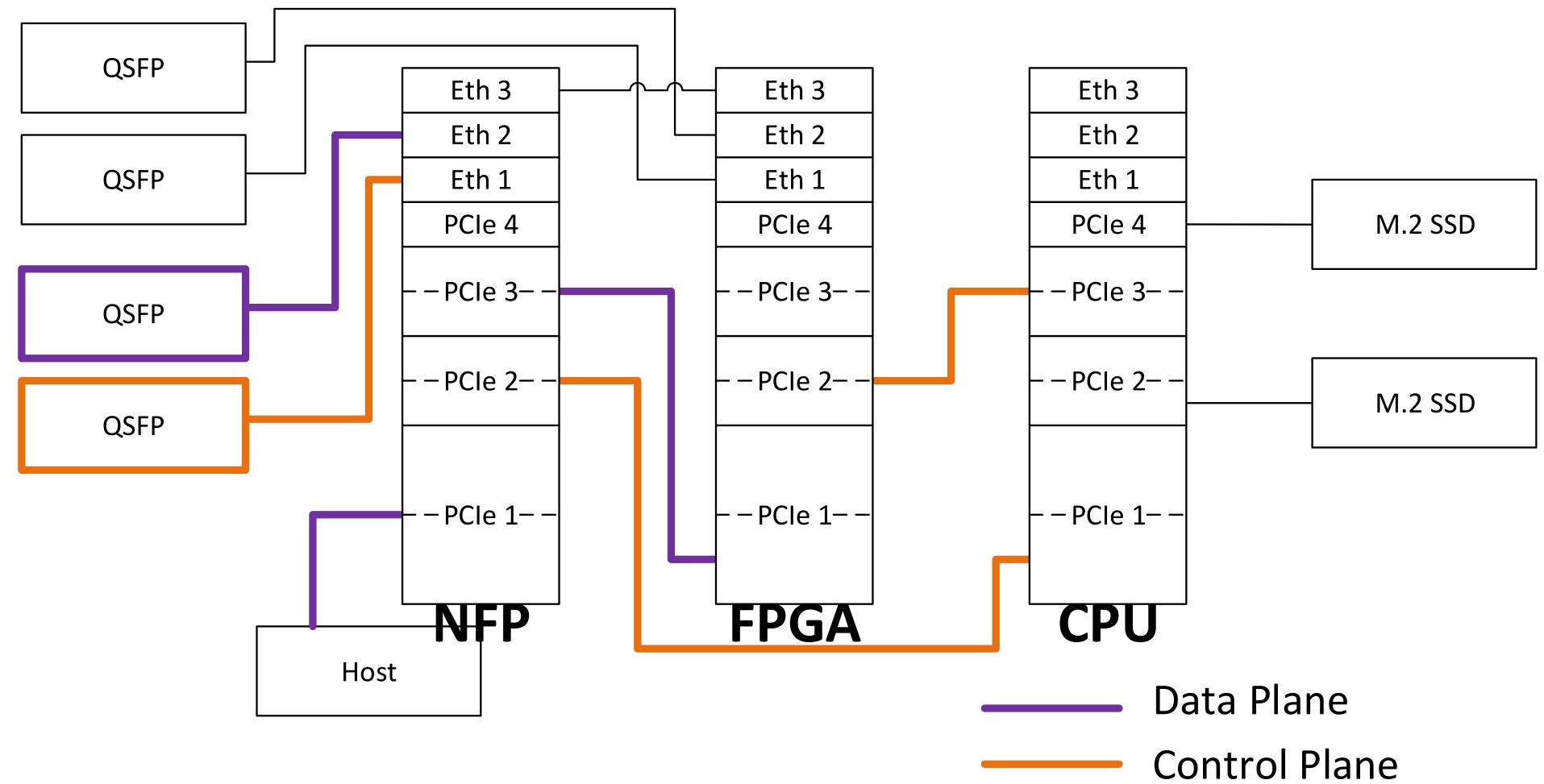


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Example: Smart NIC Side-car



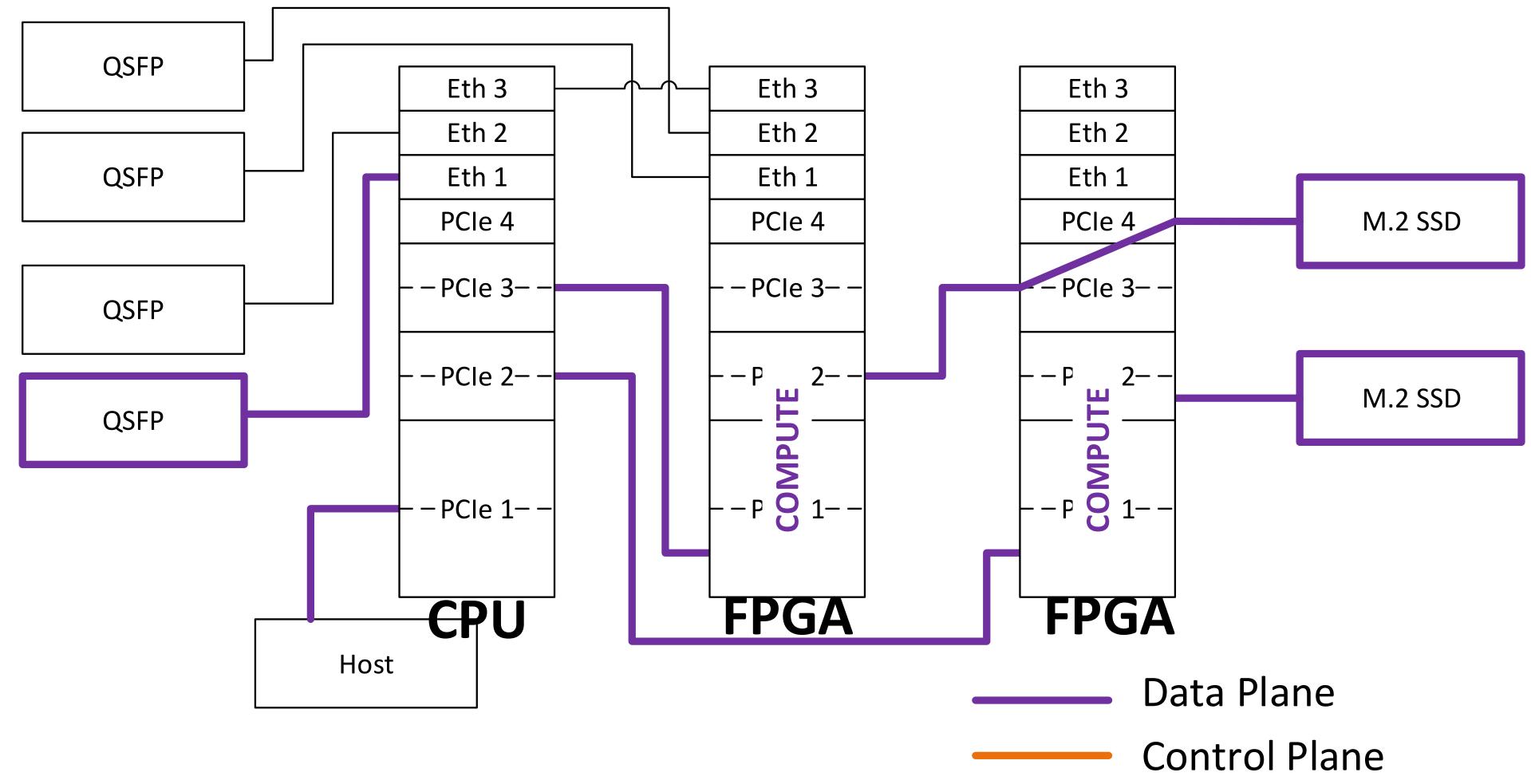
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Example: Computational Storage



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Workflow POC physical implementation

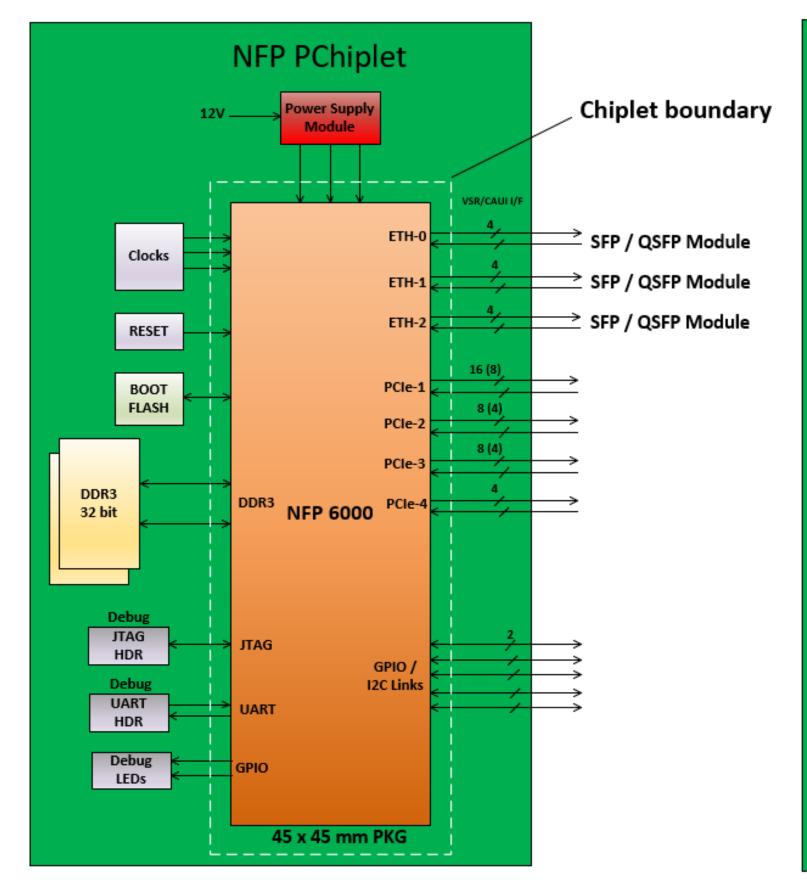


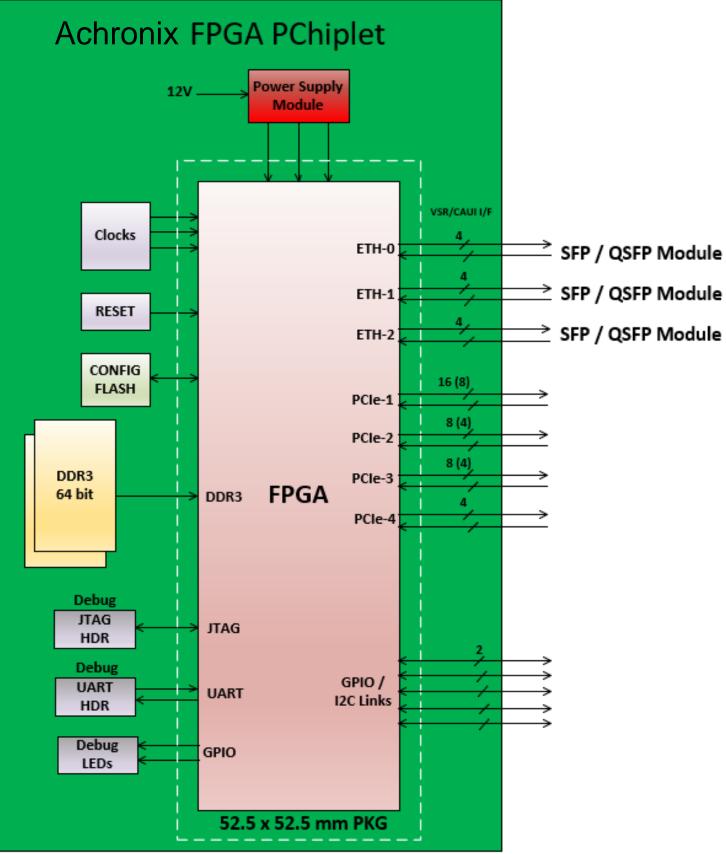
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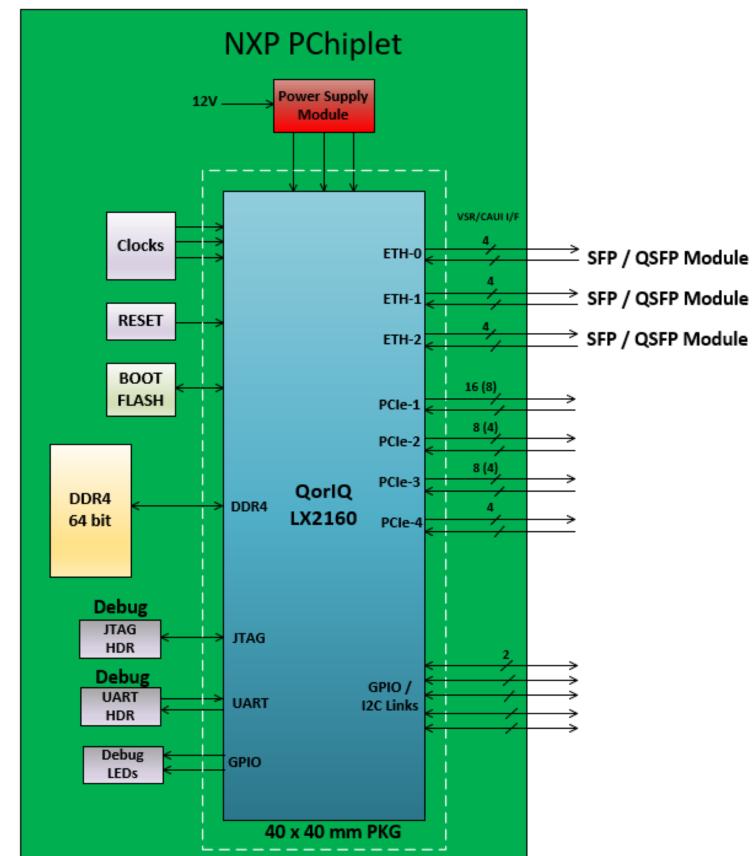
Workflow POC Pchiplets





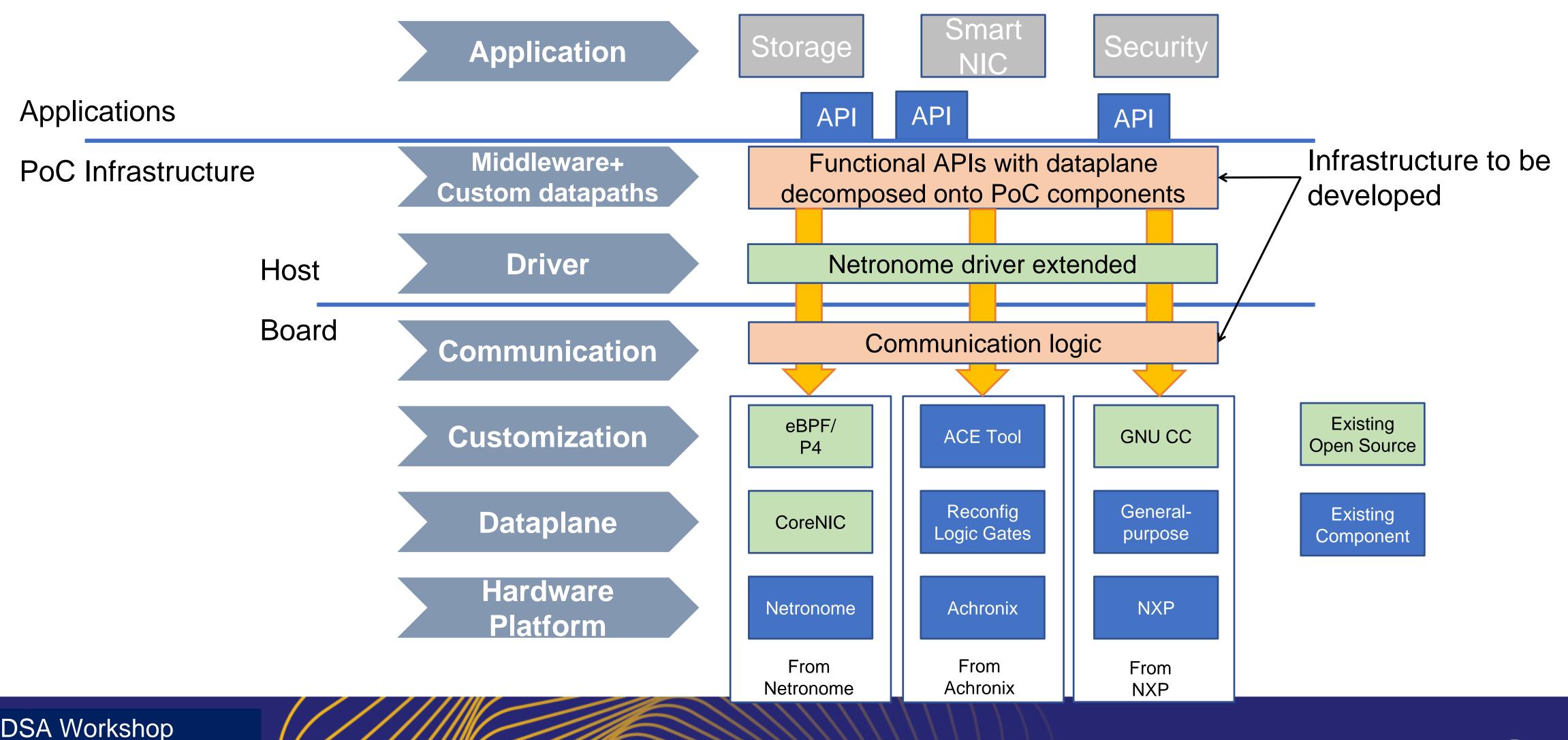
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Software and Application Development

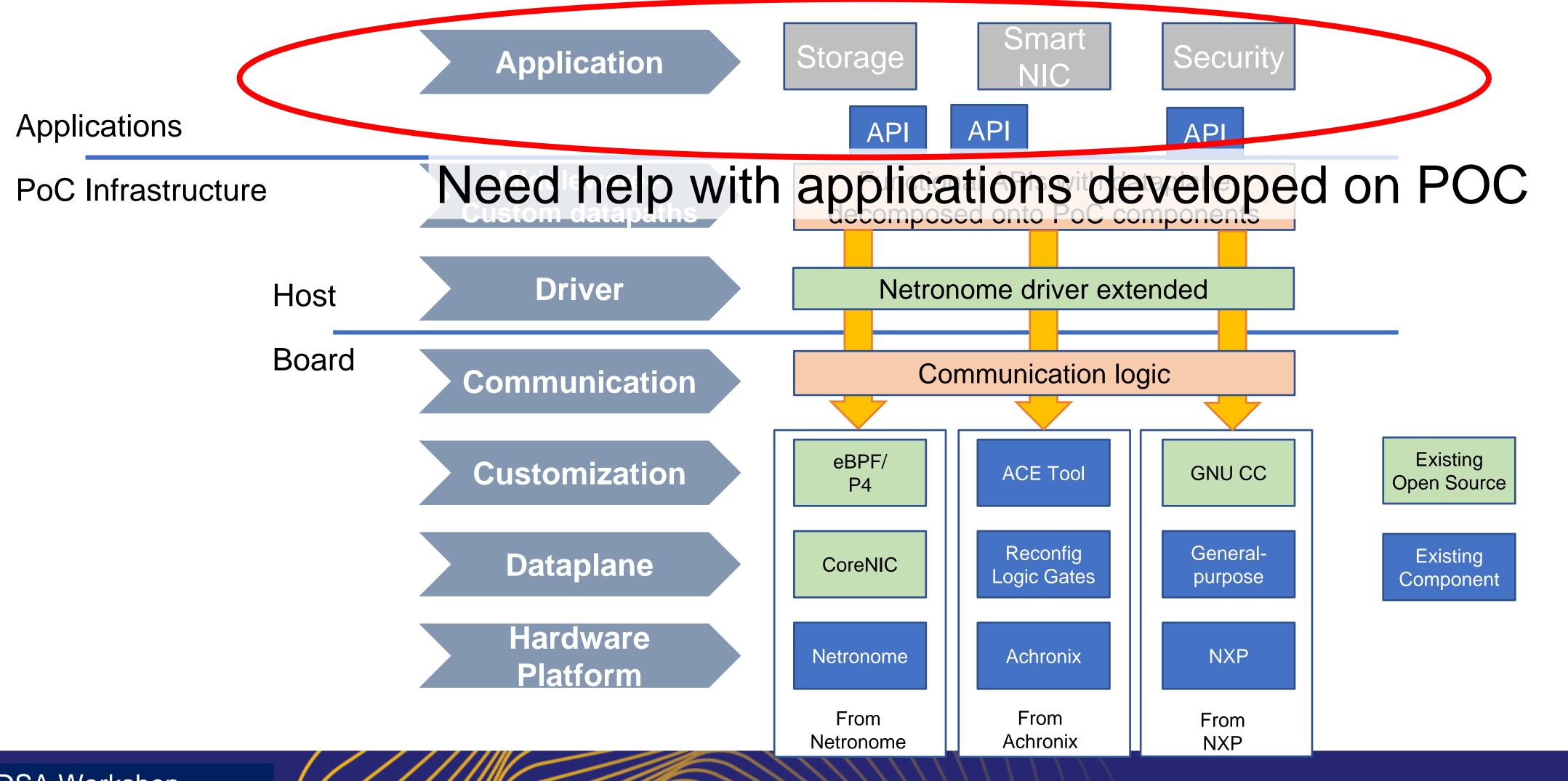
Application



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Software and Application Development



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POC Schedule

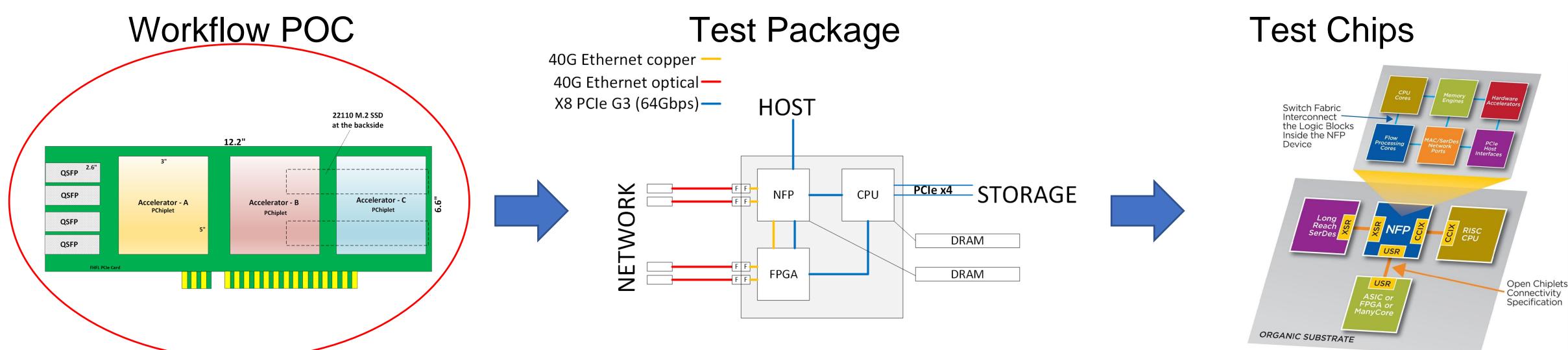
		2019									2020		
Tasks	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Jan	Feb	Mar
Architecture and Overall	Con	nponent S	Selection,	Arch									
PoC SDV Design				Schemat	cics	Layout	Mfg	Bring Up)				
PoC Package Design							Desigr	า					
Packge Manufacturing										\mathbb{N}	lfg		
Software/Firmware (Bring UP and demo)												Bring UP	

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Raising additional funds for POC



Made a lot of progress and partners are making substantial contributions Need additional funding to complete POC projects Priority today is funds to complete Workflow POC Funding partners will get early access to PoC development platform (first hardware)

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Please Join Us

We are looking for fellow travelers for all areas

- Specification Write Ups
- System Netlist Verification
- Board Design
- Software Development
- Application Porting
- Board Bring Up
- Package Design
- System Level Test Development
- Sponsor Board Manufacturing
- Sponsor Package Manufacturing

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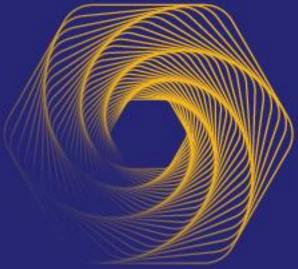


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Reach out to jawad@zglue.com







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