ODSA Proof of Concept (POC)

Quinn Jacobson, Achronix
Jawad Nasrullah, zGlue
Jayaprakash Balachandran, Cisco
Big Picture

- **Vision:** ODSA success is an open marketplace where people offer their chiplets, and those chiplets have common interfaces to interoperate.

- **Mission:** ODSA’s role is to define and prove several aspects of the concept to enable companies to be willing to make investments for future multi-party chiplet products with common interfaces.

- **Actions:** ODSA’s POCs is to kick start the process.
  - Tackle the chicken-and-egg problem by showing companies willing to make incrementally larger investments towards interoperable parts.
  - Generate proof points to reduce resistance to making first real products (Making commercial products is beyond the scope of ODSA).
Multiple dimensions of POC effort

- Operations
  - Force information sharing at a bare die-level
  - Exposing issues of sharing sensitive business metrics
  - Validate risk and value sharing models

- Architectural
  - Validate interfaces protocols
  - Evaluate performance issues
  - Develop software programming models

- Work flow
  - Yield and cost modeling
  - Explore chiplet integration and packaging
  - Validate power distribution
  - Develop high-speed I/O solutions
POC has multiple steps

Workflow/Software Dev POC
- Market place microcosm
- Workflow/Operation
- Software Development

Test chip POC
- Chiplet interface
- Packaging

First products

Market place/ecosystem
Objectives of Workflow POC

• Pathfinding with example workflow across companies and model for market place
  • Reusable cross-company workflow
  • Faster path in future for someone to build a domain-specific multi-chiplet solution
• Bootstrapping the system by building something tangible
  • Demonstrate commitment from all partners
  • Demonstrate credibility as a group
• Inspire by building accelerator (HW+SW) with contemporary performance
  • Need to attract end users
  • Show a path to real product
Workflow POC First Thought

40G Ethernet copper
40G Ethernet optical
X8 PCIe G3 (64Gbps)
Working with legacy chips/interfaces

- Explore Operations
- Working together
- Sharing information
- Building Something
- Making it real
- Credible
- Create a microcosm for a chiplet marketplace
  - “Chiplet” suppliers
  - “Chiplet” integrators
  - Software suppliers
  - System builders

- Engineering challenges NOT addressed by first POC (will be addressed with future test chips)
  - Validate new interface for chiplets
  - Packaging and board challenges of new generation of chiplets
PChiplet (pronounced “Pichlet”)

• Innovative way to take a first step
• A small PCB analogy of a chiplet
• A large PCB analogy of a substrate and package
Workflow POC Platform Architecture
Supports multiple configurations
# First PChiplets

<table>
<thead>
<tr>
<th>Port</th>
<th>Netronome NFP</th>
<th>Achronix FPGA</th>
<th>NXP CPU</th>
<th>SSD Jumper</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ethernet 3</td>
<td>YES</td>
<td>YES</td>
<td>NO</td>
<td></td>
</tr>
<tr>
<td>Ethernet 2</td>
<td>YES</td>
<td>YES</td>
<td>NO</td>
<td></td>
</tr>
<tr>
<td>Ethernet 1</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td></td>
</tr>
<tr>
<td>PCIe 4 x4</td>
<td>NO</td>
<td>NO</td>
<td>YES x4</td>
<td></td>
</tr>
<tr>
<td>PCIe 3 x8</td>
<td>YES x8</td>
<td>NO</td>
<td>YES x4 only</td>
<td></td>
</tr>
<tr>
<td>PCIe 2 x8</td>
<td>YES x8</td>
<td>YES x8</td>
<td>YES x4 only</td>
<td></td>
</tr>
<tr>
<td>PCIe 1 x16</td>
<td>YES x8 only</td>
<td>YES x8 only</td>
<td>YES x8</td>
<td></td>
</tr>
</tbody>
</table>

**Jumper**
Example: Smart NIC bump-in-wire
Example: Smart NIC Side-car

Host

PCIe 1
PCIe 2
PCIe 3
PCIe 4

Eth 1
Eth 2
Eth 3

QSFP

NFP

Data Plane

FPGA

Control Plane

CPU

M.2 SSD

M.2 SSD

Open. Together.
Example: Computational Storage

![Diagram showing a network with CPU, FPGA, QSFP, and M.2 SSD connections.](image-url)
Workflow POC physical implementation
Workflow POC Pchiplets

NFP PChiplet
- Chiplet boundary
- Power Supply Module
- Clocks
- SFP / QSFP Module
- DDR3 32 MB
- GPIO / I2C Links
- JTAG
- UART
- Debug
- LEDs
- 45 x 45 mm PKG

Achronix FPGA PChiplet
- Power Supply Module
- Clocks
- SFP / QSFP Module
- DDR3 64 MB
- GPIO / I2C Links
- JTAG
- UART
- Debug
- LEDs
- 52.5 x 52.5 mm PKG

NXP PChiplet
- Power Supply Module
- Clocks
- SFP / QSFP Module
- DDR4 64 MB
- GPIO / I2C Links
- JTAG
- UART
- Debug
- LEDs
- 40 x 40 mm PKG

Open. Together.
Software and Application Development

PoC Infrastructure

- Middleware+ Custom datapaths
- Driver
- Communication
- Customization
- Dataplane
- Hardware Platform

Applications

- Application
- Storage
- Smart NIC
- Security

API

Functional APIs with dataplane decomposed onto PoC components

Netronome driver extended

Communication logic

- eBPF/P4
- ACE Tool
- GNU CC
- CoreNIC
- Reconfig Logic Gates
- General-purpose
- Netronome
- Achronix
- NXP

Infrastructure to be developed

- From Netronome
- From Achronix
- From NXP

Existing Open Source

Existing Component

- From

ODSA Workshop
September 12, 2019
Hosted by IBM
Software and Application Development

Applications

PoC Infrastructure

Host

Board

Application

Storage

Smart NIC

Security

API

API

API

Netronome driver extended

Communication logic

eBPF/P4

ACE Tool

GNU CC

CoreNIC

Reconfig Logic Gates

General-purpose

Netronome

Achronix

NXP

From Netronome

From Achronix

From NXP

Need help with applications developed on POC

From Netronome

From Achronix

From NXP
## POC Schedule

<table>
<thead>
<tr>
<th>Tasks</th>
<th>Mar</th>
<th>Apr</th>
<th>May</th>
<th>Jun</th>
<th>Jul</th>
<th>Aug</th>
<th>Sep</th>
<th>Oct</th>
<th>Nov</th>
<th>Dec</th>
<th>Jan</th>
<th>Feb</th>
<th>Mar</th>
</tr>
</thead>
<tbody>
<tr>
<td>Architecture and Overall</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Component Selection, Arch</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PoC SDV Design</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Schematics</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Layout</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mfg</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bring Up</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PoC Package Design</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Design</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package Manufacturing</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mfg</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Software/Firmware (Bring UP and demo)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bring UP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**2019**

**2020**
Raising additional funds for POC

Made a lot of progress and partners are making substantial contributions
Need additional funding to complete POC projects
Priority today is funds to complete Workflow POC
Funding partners will get early access to PoC development platform (first hardware)
Please Join Us

We are looking for fellow travelers for all areas

• Specification Write Ups
• System Netlist Verification
• Board Design
• Software Development
• Application Porting
• Board Bring Up
• Package Design
• System Level Test Development
• Sponsor Board Manufacturing
• Sponsor Package Manufacturing

Reach out to jawad@zglue.com