OPEN Compute Project®

OCP – ODSA Project

Community Led Hyperscale Open Innovation

Commercialization Use Case

cadence®

UltraLink D2D PHY & OHBI

Rishi Chugh

Chiplet Examples for Heterogenous System Design

- New Design paradigm , from IP reuse to Chiplet reuse
- Primary drivers for chiplet functionality:

- Multi-Core
- GPGPU
- CPU + Workload accelerator
- Scientific computing

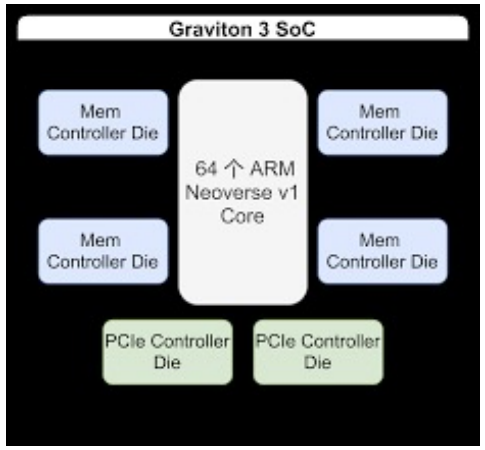
Processor

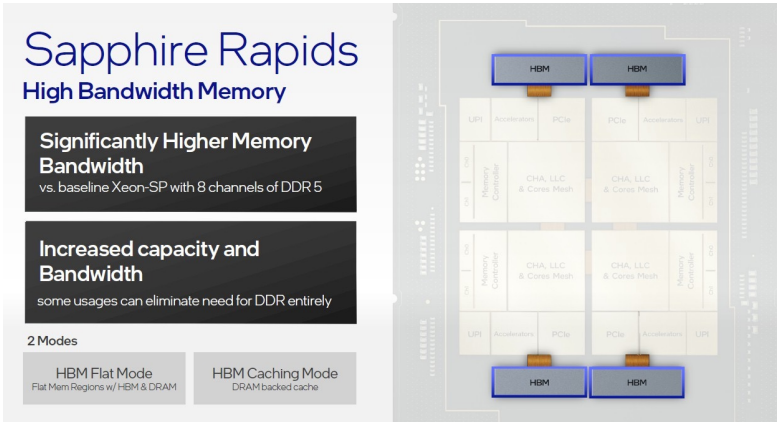
- HBM - Cache Extensions
- PIM (Processing In Memory)
- Packet Buffering / Look Ups
- Data Analytics / Cache Ext

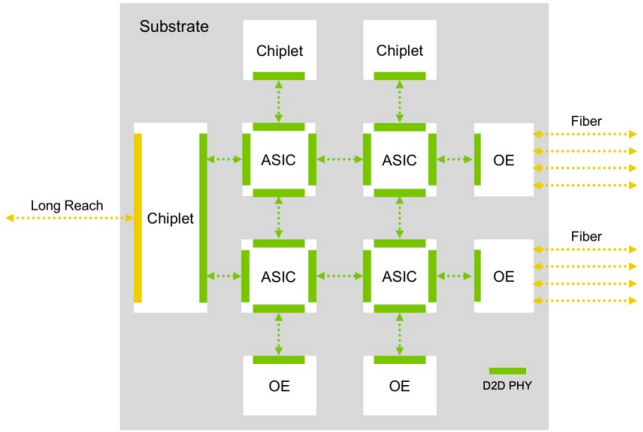
Memory / Storage

- Host / Client / IO Peripherals
- NoC (Chip / Interposer)
- Server SoC (CPU+Chipsets)
- WEB servers , Fabric , NIC

CONNECTIVITY







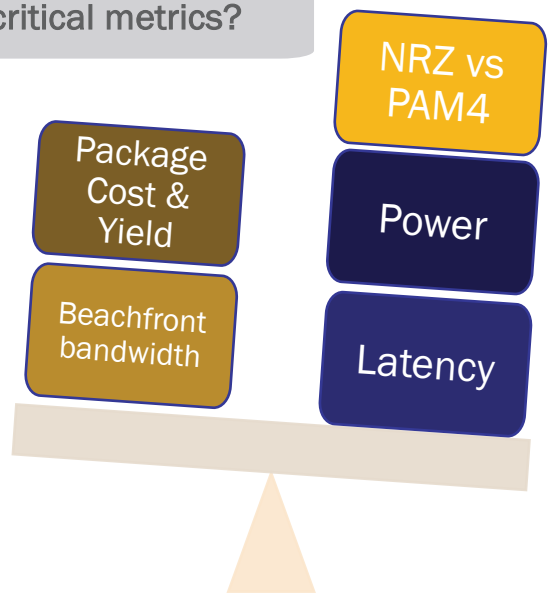
High Speed Connectivity & Chiplets Strategy

- Investment for Chiplet based design driven by SoC Application & Scaling

What are the most critical metrics?

Can we avoid using high-cost packaging? (e.g.silicon interposer or InFO)

Is the system proprietary or we need an eco-system?



Parallel Interface	NRZ Serial Interface	PAM4 Serial Interface
Ex: AIB, HBM, HBI (2-4Gbps NRZ)	Ex: 20-30Gbps NRZ	112G-PAM4
Required by advanced packaging – silicon interposer or InFo	Pros: Support organic substrate, easy routing, low latency	Pros: Industry standard (CIE-OIF-XSR112G)
Pros: Lowest power, low latency, must-have for HBM	Cons: Higher power, design complexity	Cons: Requires FEC for "error-free" links, higher latency, higher power
Cons: High wire count, high package cost, low yield, reliability issue	Fastest, higher bandwidth, low latency	

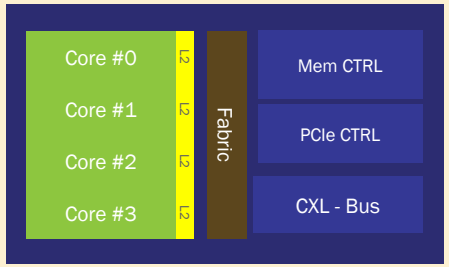
There's NO one size fits all solution for D2D connectivity

OHBI D2D / BoW XSR

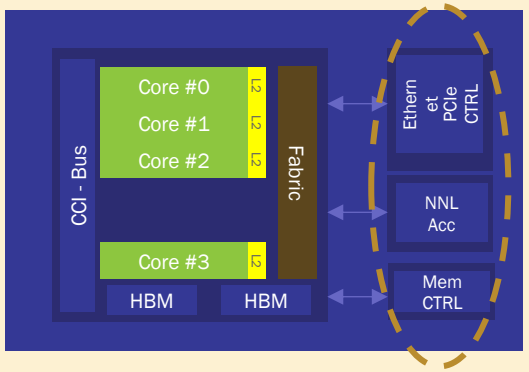
Chiplet Landscape (OEM , Close Box , High Barrier To Entry)

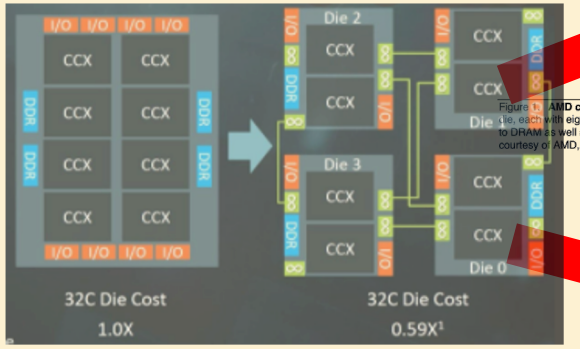
Processors

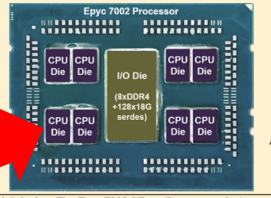
Legacy CPU



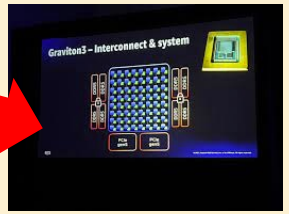
Workload Optimized CPU





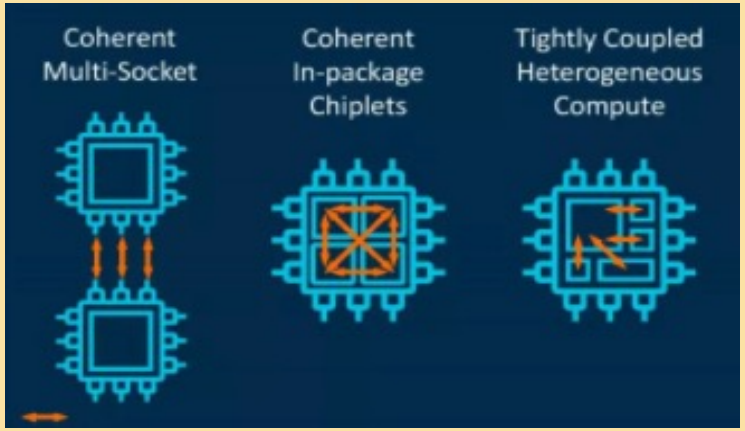


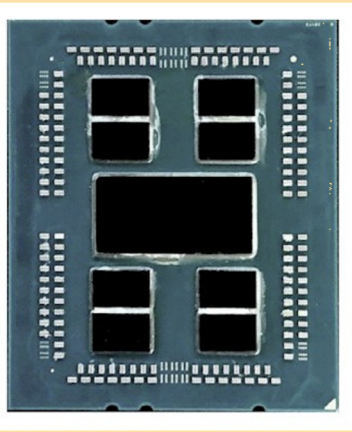
AMD chiplet design. The Epyc 7002 ("Rome") processor features eight 74mm² CPU die, each with eight x86 cores and 32MB of cache. The I/O die measures 410mm² and connects to DRAM as well as high-speed peripherals. The organic package measures 58x78mm. (Photo courtesy of AMD, overlay by The Linley Group)

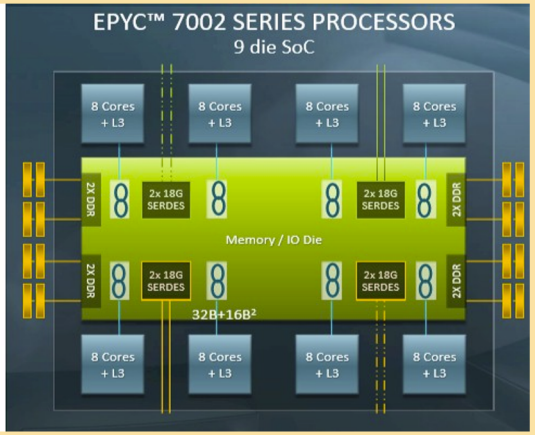


AMD intel Google AMPERE aws NVIDIA

Memory & Storage



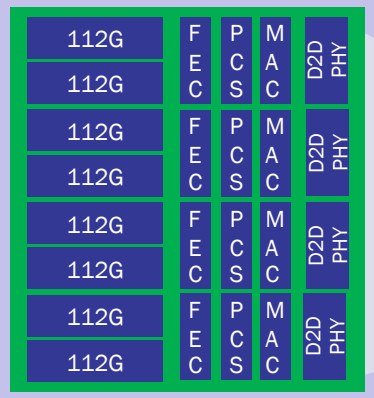


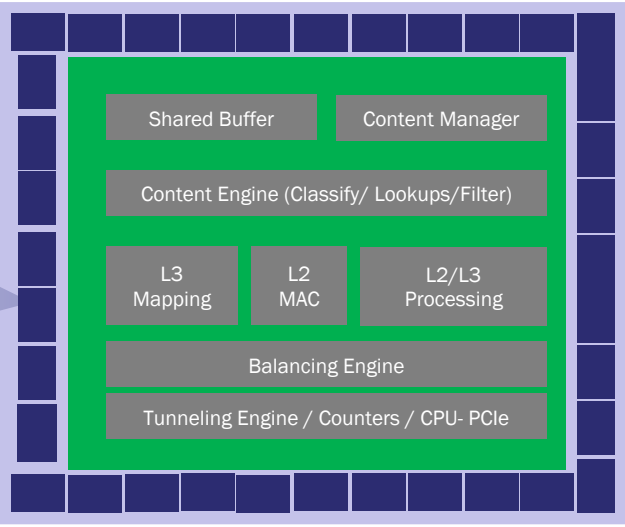


Facebook Google intel Micron AMD NVIDIA

Chiplet Landscape (CDNS has all these IP + System know how)

Connectivity

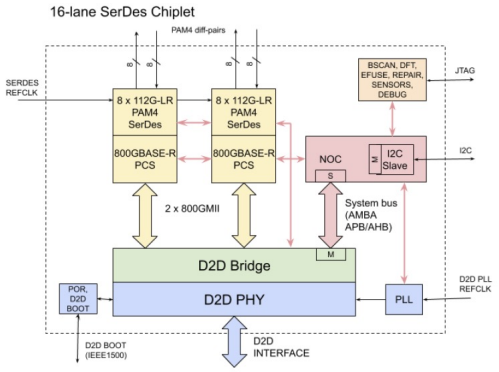




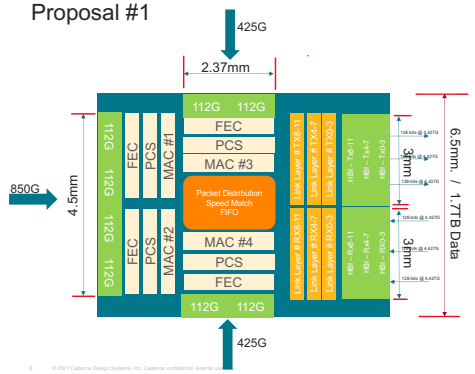
- L0/L1 layer implemented on the chiplet
- Provides optimal fabric design flexibility –
  - scalability , larger buffer for high bandwidth
  - i.e. 25T+ on monolithic die
- Can be potentially extended to enable GB , FEX & Multi-Channel features on the chiplet

CISCO aws

Block Diagram



Proposal #1



Each HBI – Tx0-3 => 128-bit @ 4.8G → 614.4G
Total 3 stacks → 384-bit @ 4.8G → 1.8432Tbps

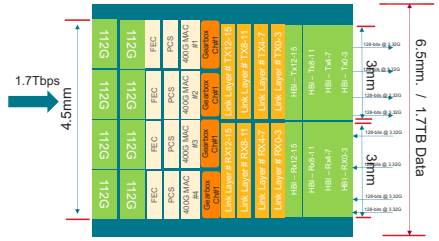
Design Requirement → 1.7Tbps
HBI link speed → 4.4270833Gbps

Not the best architecture due to channel mismatch

- Total 4 x 400G pipe's
- HBI 3 stack mapping → 3 channels (HBI side)
- Mapping HBI → 112G channels is not clean
- **Each stack of HBI → 566.666G** (@ 4.42G), not integer multiple of 106.25G

Mapping Requirement/Math :
- 24-bits of HBI → Each 112G PHY link
- However Dword block is 32-bit and makes this mapping coMplex adding latency / FIFO

Proposal #2B



Each HBI – Tx0-3 => 128-bit @ 4.8G → 614.4G
Total 4 stacks → 512-bit @ 4.8G → 2.4576Tbps

Design Requirement → 1.7Tbps
HBI link speed → 3.3203125Gbps

Not the best architecture due to channel mismatch

- Total 4 x 400G pipe's
- HBI 4 stack mapping → 4 channels (HBI side)
- Mapping HBI → 112G channels is clean (1:1)
- Each 128-bit @ 3.3203125G → 4 x 106.25G (425G)
- **Each stack of HBI → 425G** (@ 3.32G)

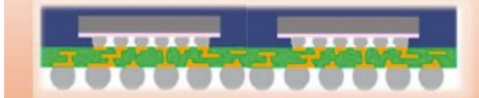
Mapping Requirement/Math :
- 128-bits of HBI → Each 112G PHY link

SoC–Advance Package Integration To Chiplet Partitioning

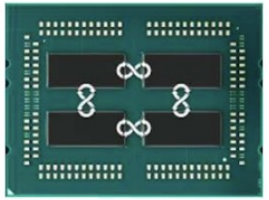
Advanced Integration

SiP

Multi-Chip-Module



Interconnect density: 100µm x 100µm



Source: AMD EPYC 7260, 4-chiplet chip

System-in-Package

Home > Packaging, Test & Materials > Getting Down To Business On Chiplets

PACKAGING, TEST & MATERIALS

Getting Down To Business On Chiplets

60 Shares

Consortiums seek ways to ensure interoperability of hardened IP as way of cutting costs, time-to-market, but it's not going to be easy.

NOVEMBER 26TH, 2018 - BY: ED SPERLING

Government agencies, industry groups and individual companies are beginning to rally around various chiplet models, setting the stage for complex chips that are quicker and cheaper to build using standardized interfaces and components.

The idea of putting together different modules like LEGOs has been talked about for the better part of a decade. So far, only Marvell has used this

https://semiengineering.com/semiconductor-industry-getting-serious-about-ch

Source: Micron High-Bandwidth-Memory

2.5D

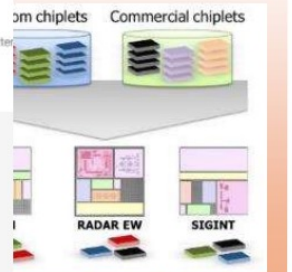
Opinion: Chiplets to drive the future of Semis

Some of the more interesting advancements in the semiconductor world are now occurring in inter packaging technologies

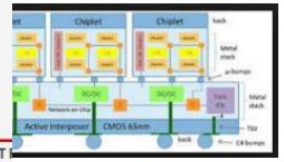
In context: A classic way for engineers to solve a particularly vexing technical problem is to move things in a completely different direction—typically by "thinking outside the box." Such is the case with challenges facing the semiconductor industry. With the laws of physics quickly closing in on them, the traditional brute force means of maintaining Moore's Law, by shrinking the size of transistors, is quickly coming to an end. Whether things stall at the current 7nm (nanometer) size, drop down to 5nm, or at best, reach 4nm, the reality of a nearly insurmountable wall is fast approaching today's leading vendors.

https://www.techspot.com/news/77397-opinion-chiplets-drive-future-semis.html

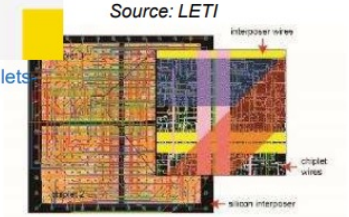
CHIPLET partitioning



Source: DARPA



Source: LETI



Source: GeorgiaTech

3D Integrated-Circuit (3D IC)

Cadence / ODSA

- Cadence contributing and carving industry path towards chiplet based SoC design
- Full 3D tool support working on close partnership with OCP as well as leading multiple foundry house
- Successful commercial deployments of chiplet based SoC architectures
- Closely contributing , following and enabling industry on BoW & OHBI standards
  - Existing UltraLink offering similar to BoW architecture
  - OHBI under development for industry enablement

Comparison: Technical Specifications

Metrics	Die-to-Die	112G-XSR	HBI* v1.1
Line Rate	20-40Gbps	112Gbps	16Gbps
Number of wires in a macro	6 Rx or Tx	Up to 8	64 to 1024 bits
Max Beachfront Bandwidth (Gbps/mm) (single row)	500 Gbps/mm	500 Gbps/mm	>4 Tbps/mm (Tx + Rx aggregated)
Insertion Loss @ Nyquist	8db @ 20GHz	10db @ 28GHz	<3db @ 16GHz
Signaling	Single Ended, NRZ	Differential, PAM4	Single Ended Data, Differential Strobe
Power (pj/bit)	1.5pJ/bit	1.87pJ/bit	0.5pJ/bit
Lane Area (one TX+RX)	0.67mm^2 (240G Rx + 240G Tx, half duplex)	0.31mm^2 (112G Rx + 112G Tx, full duplex)	0.168mm^2 (512G Rx + 512G Tx, half duplex)
Area/Tbps	2.8 mm^2/Tbps	2.76 mm^2/Tbps	0.22 mm^2/Tbps
Clocking	Forwarded Clock	Independent clock (CDR)	Forwarded Clock Strobe
PMA Latency	5.4ns (Rx+Tx @ 40Gbps)	8.4ns (Rx+Tx @ 112Gbps)	<5 ns Tx “DFI”->Pad <5 ns Rx Pad -> “DFI”
Per Bit Alignment	Per bit Phase adjustment	CDR	Per bit Phase adjustment
Raw BER	1e-15, no-FEC	1e-9 (pre-FEC)	1e-15 (pre-ECC/FEC)
Process	7nm & 5nm	7nm	N3
Bump pitch	130u	130u	40.3/40/70um (diag/X/2Y)
Other	Line Rate flexible for optimal Performance & Power tradeoff	Compatible with Standard Ethernet PMA (OIF-112G-XSR)	0.3V IO

cadence®