Full Width HPM Form Factor (M-FLW) Base Specification

Part of the
Datacenter – Modular Hardware Systems (DC-MHS) Rev 1.0 Family
Version 0.7
April 22nd, 2022
Revision 1.0 Authors/Contributors:

Dell, Inc: Corey Hartman, Sanjiv Sinha, Shawn Dube

Google LLC: Siamak Tavallaei, Jim Levins, Mike Branch

Hewlett Packard Enterprise Company: Vincent Nguyen, David Paquin, Binh Nguyen

Intel Corporation: Brian Aspnes, Drew Damm, Gene Young, Brendan Pavelek, Cliff Dubay

Meta Platforms, Inc: Damien Weng Kong Chong, Todd Westhauser, Michael Haken

Microsoft Corporation: Priscilla Lam, Mark Shaw; Priya Raghu, Luke Gregory

Note: For questions about this specification please contact Corey Hartman and / or Brian Aspnes at dcmhs@opencompute.org
## Table of Contents

1. License ........................................................................................................................................ 7
   1.1. Open Web Foundation (OWF) CLA ....................................................................................... 7
   1.2. Acknowledgements ............................................................................................................. 8

2. Version Table ................................................................................................................................ 9

3. Scope ............................................................................................................................................. 10
   3.1. Items Not in Scope of Specification ..................................................................................... 10
   3.2. Typical OCP Sections Not Applicable ................................................................................. 10

4. Overview ...................................................................................................................................... 11

5. References .................................................................................................................................... 11

6. Terminology .................................................................................................................................. 13

7. Background and Assumptions ...................................................................................................... 14
   7.1. Rear Management (ie, OEM) Architecture Specific Assumptions ...................................... 14
   7.2. Front Management (ie, Hyperscale) Architecture Specific Assumptions: ......................... 15

8. HPM Layout .................................................................................................................................. 16
   8.1. Two Socket (CPU) Assumptions .......................................................................................... 17
   8.2. One Socket Assumptions .................................................................................................... 17

9. Mechanical Requirements ............................................................................................................. 18
   9.1. HPM Outline ..................................................................................................................... 18
   9.2. Board Datum and Mounting holes ...................................................................................... 19
   9.3. HPM Board and Assembly Thickness ................................................................................ 20
   9.4. HPM to Chassis Retention .................................................................................................. 22
      9.4.1. Keep out zone for Retention Hardware ........................................................................ 22
   9.5. HPM Handling ................................................................................................................... 23
   9.6. Common Peripheral Location Requirements ...................................................................... 25
      9.6.1. Near Edge Peripheral Locations .................................................................................. 25
      9.6.2. Far Edge Peripheral Connections ................................................................................ 26
   9.7. Internal USB Connection .................................................................................................... 27
   9.8. Intrusion Switch Connection ............................................................................................... 28
   9.9. Boot Storage Peripheral Connection .................................................................................. 29
   9.10. Near IO Riser-Cable Connector Placement ....................................................................... 30
      9.10.1. Near IO Riser Cable Connector Requirements .......................................................... 30
      9.10.2. Near IO Riser Cable Connector Recommendations and Guidance ......................... 31

Date: 04/22/2022
9.11. Far Side IO Connector Placement ..............................................................................34
9.12. Mounting Hole Requirements for IO Module Retention ...........................................34
9.13. Primary Side Component Height Restriction Zones ..................................................36
  9.14.1. Overall Secondary side Keep In Zone Requirements ................................................37
  9.14.2. Chassis-to-Board Bracket (Board Pan) Requirements, and KOZs .........................37
9.15. Liquid Cooling Bracketry Keep Out Zones .................................................................39
9.16. Cabling Enablement Keep Out Zones .......................................................................40
10. Power Delivery ..................................................................................................................41
  10.1. HPM Power Zones ..................................................................................................41
    10.1.1. Zone A – M-CRPS Connector ........................................................................42
    10.1.2. Zone B – 2x6+12s PICPWR ........................................................................43
  10.1.3. Zone C – Near Side Riser PICPWR Egress ..........................................................45
  10.1.4. Zone D – DC-SCM R2.0 ..................................................................................45
  10.1.5. Zone E – OCP NIC R3.0 and Platform Custom Zone ...........................................45
10.2. HPM Power Planes ....................................................................................................46
11. I/O System (Electrical Interfaces) ....................................................................................48
  11.1. High Speed IO (HSIO) connectors .........................................................................48
  11.2. Internal USB .........................................................................................................48
  11.3. MHS Intrusion Switch ............................................................................................48
  11.4. MHS Boot Storage Peripheral Connection .............................................................48
12. Adapted FLW HPMs ........................................................................................................49
  12.1. UBB / Blade FLW Adapted HPM Requirements .......................................................49
    12.1.1. UBB Blade FLW HPM Outline ......................................................................49
    12.1.2. Blade High Speed IO connector .....................................................................50
    12.1.3. Ingress Power Connector ...............................................................................52
    12.1.4. Blade Minimum Power Plane Capacity Requirements ....................................52
    12.1.5. Blade Mechanical Guide Pin ...........................................................................53
13. Supplemental Information ..............................................................................................54
  13.1. Alternate HPM Outlines for OCP NIC R3.0 .............................................................54
14. Rack and Chassis Depth Stackup Assumptions .................................................................56
  13.3. 1U and 2U PCIe Slot Typical Configurations ..........................................................57
  13.4. Additional Information on Near IO Riser Retention Holes ........................................59

Date: 04/22/2022

4
13.5. Reference System Architecture in 21” Chassis ..........................................................60
13.6. Chassis Base Geometry for Chassis-to-Board Bracket interface .................................60
13.7. CAD files ..................................................................................................................61
14. Appendix A - Checklist for IC approval of this specification (to be completed by contributor(s) of this Spec) ..........................................................................................................................61
15. Appendix B-<supplier name>- OCP Supplier Information and Hardware Product Recognition Checklist ..........................................................................................................................61
Table of Figures

105  Figure 1.  Full Width HPM Layout Diagram ..........................................................16
     Figure 2.  First CPU position relative to OCP NIC R3.0 and DC SCM R2.0 ..................17
     Figure 3.  Full Width HPM Outline ...........................................................................18
     Figure 4.  Board Mounting Holes ............................................................................19
     Figure 5.  Board and Chassis Stackup Considerations ................................................20
110  Figure 6.  HPM thickness and Straddle Mount Peripheral Offsets .................................21
     Figure 7.  HPM Assembly to Chassis Retention Enablement .....................................22
     Figure 8.  HPM Handling Feature ............................................................................23
     Figure 9.  HPM Handling Feature Location ................................................................24
     Figure 10.  Centerline Locations of OCP NIC R3.0 and DC-SCM R2.0 ......................25
115  Figure 11.  Control Panel Connection Locations .......................................................26
     Figure 12.  USB Connection Placement Zone ..............................................................27
     Figure 13.  Placement Zone for Intrusion Switch Connector .........................................28
     Figure 14.  Placement Zone for Boot Peripheral Connector .........................................29
     Figure 15.  Near IO Riser-Cable Connector Keep In Zone for Risers .............................31
120  Figure 16.  Reference Locations of Recommended Near IOs for Amphenol G03V213X2HR .33
     Figure 17.  1U IO Module Retention Enablement Holes .............................................35
     Figure 18.  2U IO Module Retention Enablement Holes .............................................35
     Figure 19.  Zones for Primary Side Component Height Restrictions .........................36
     Figure 20.  Example of Chassis-to-Board Bracket (Board Pan) ....................................37
125  Figure 21.  Motherboard Secondary Side HPM Zero-Height Keep Out Zones for Chassis to Board Bracketry .................................................................38
     Figure 22.  Liquid Cooling Bracket Keep Outs ..............................................................39
     Figure 23.  HPM Power Zone locations .....................................................................41
     Figure 24.  M-CRPS Power Connector .....................................................................42
130  Figure 25.  M-CRPS Connector Location Requirements ............................................43
     Figure 26.  2x6+12s PICPWR Power Connectors .......................................................44
     Figure 27.  PICPWR connector (2x6+12s) Location Requirement (6 locations) ...........44
     Figure 28.  Power Plane (and supplementary power delivery mechanisms) Checkpoint Areas ..........................................................47
     Figure 29.  Full Width HPM Outline for UBB and Blade FLW ........................................50
135  Figure 30.  Examax 4x8 connector ...........................................................................51
     Figure 31.  Examax 6x8 connector ...........................................................................51
     Figure 32.  Power Blade Plus Ingress Power Connector .............................................52
     Figure 33.  Blade Power Plane Checkpoint Areas .........................................................53
     Figure 34.  Outline Cutout modification to Enable Cabled OCP NIC R3.0 in Base Outline ....55
140  Figure 35.  Alternate Outline to Enable OCP NIC R3.0 LFF ..........................................55
     Figure 36.  Rack Depth Constraints ...........................................................................56
     Figure 37.  Typical 1U and 2U PCIe Slot Configurations for Rear Management System ...57
     Figure 38.  Typical 1U and 2U PCIe Slot Configurations for Front Management System ...58
     Figure 39.  Riser Retention Holes and Associated Near XIO Locations ........................59
145  Figure 40.  Base Outline HPM used in 21” Reference Chassis .......................................60
     Figure 41.  Chassis Base Geometry to Interface Chassis-to-Board Bracketry ..................61
1. License

1.1. Open Web Foundation (OWF) CLA

Contributions to this Specification are made under the terms and conditions set forth in Open Web Foundation Modified Contributor License Agreement (“OWF CLA 1.0”) (“Contribution License”) by:

- Dell, Inc
- Intel Corporation
- Hewlett Packard Enterprise Company
- Meta Platforms, Inc
- Google LLC
- Microsoft Corporation

Usage of this Specification is governed by the terms and conditions set forth in Open Web Foundation Modified Final Specification Agreement (“OWFa 1.0”) (“Specification License”).

You can review the applicable OWFa 1.0 Specification License(s) referenced above by the contributors to this Specification on the OCP website at http://www.opencompute.org/participate/legal-documents/. For actual executed copies of either agreement, please contact OCP directly.

Notes:

1) The above license does not apply to the Appendix or Appendices. The information in the Appendix or Appendices is for reference only and non-normative in nature.

NOTWITHSTANDING THE FOREGOING LICENSES, THIS SPECIFICATION IS PROVIDED BY OCP "AS IS" AND OCP EXPRESSLY DISCLAIMS ANY WARRANTIES (EXPRESS, IMPLIED, OR OTHERWISE), INCLUDING IMPLIED WARRANTIES OF MERCHANTABILITY, NONINFRINGEMENT, FITNESS FOR A PARTICULAR PURPOSE, OR TITLE, RELATED TO THE SPECIFICATION. NOTICE IS HEREBY GIVEN, THAT OTHER RIGHTS NOT GRANTED AS SET FORTH ABOVE, INCLUDING WITHOUT LIMITATION, RIGHTS OF THIRD PARTIES WHO DID NOT EXECUTE THE ABOVE LICENSES, MAY BE IMPLICATED BY THE IMPLEMENTATION OF OR COMPLIANCE WITH THIS SPECIFICATION. OCP IS NOT RESPONSIBLE FOR IDENTIFYING RIGHTS FOR WHICH A LICENSE MAY BE REQUIRED IN ORDER TO IMPLEMENT THIS SPECIFICATION. THE ENTIRE RISK AS TO IMPLEMENTING OR OTHERWISE USING THE SPECIFICATION IS ASSUMED BY YOU. IN NO EVENT WILL OCP BE LIABLE TO YOU FOR ANY MONETARY DAMAGES WITH RESPECT TO ANY CLAIMS RELATED TO, OR ARISING OUT OF YOUR USE OF THIS SPECIFICATION, INCLUDING BUT NOT LIMITED TO ANY LIABILITY FOR LOST PROFITS OR ANY CONSEQUENTIAL, INCIDENTAL, INDIRECT, SPECIAL OR PUNITIVE DAMAGES OF ANY CHARACTER FROM ANY CAUSES OF ACTION OF ANY KIND WITH RESPECT TO THIS SPECIFICATION, WHETHER BASED ON BREACH OF CONTRACT, TORT (INCLUDING NEGLIGENCE), OR OTHERWISE, AND EVEN IF OCP HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.
1.2. Acknowledgements
The Contributors of this Specification would like to acknowledge the following companies for their feedback:

List all companies or individuals who may have assisted you with the specification by providing feedback and suggestions but did not provide any IP.

<<blank>>
## 2. Version Table

<table>
<thead>
<tr>
<th>Date</th>
<th>Version #</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4/22/2022</td>
<td>0.7</td>
<td>Initial Public Release</td>
</tr>
</tbody>
</table>
3. **Scope**

This document defines technical specifications for the Server Product used in Open Compute Project. This document shall comprise the hardware product types complete technical specification. Any supplier seeking OCP recognition for a hardware product based on this spec must be 100% compliant with any and all features or requirements described in this specification.

3.1. **Items Not in Scope of Specification**

- Compute Core (CPU/Memory/Voltage Regulators/SMP routing between CPUs)
- JTAG/Debug connectors for the Compute Core
- CPU, Memory, Heatsink, Liquid and any other thermal solutions
- Reliability requirements and design-in details

3.2. **Typical OCP Sections Not Applicable**

Open Compute documents are typically expected and desired to contain common document Sections. The DC-MHS specifications are comprised of Base Form Factor Specifications and Supporting Platform Connectivity specifications, and are structured such that the typical OCP document structure does not apply to this Base Form Factor Spec. This specification will not contain the following Sections.

- Rack Compatibility (See **Sections 7 and 13.2**)
- Physical Specifications
- Thermal Design Requirements
- Rear Side Power, I/O, Expansion
- Onboard Power System
- Environmental Regulations/Requirements
- Prescribed Materials
- Software Support
- System Firmware
- Hardware Management
- Security

The content expected in these subject areas is expected to be documented in future private and/or public Design Specifications and/or Product Specifications.
4. **Overview**

The objective of this specification is to specify the requirements of a Full Width Host Processor Module (HPM). This is for use within products designed for minimum 19” rack, also known as compliant with EIA-310-D but can also accommodate larger 21” racks. This form factor enables a full width HPM usage for CPUs, DIMMs, and related features. This full width form factor generally allows for maximum IO of the CPUs to be offered and brought to accessible slots (although exceptions could occur in the future). This specification will NOT reference a specific CPU or memory technologies. The goals and success criteria of this specification is so that multiple generations of CPU/Memory (Compute Core) designs can be designed into this form factor specification, so that chassis and system designs can be reused as desired. This should have the benefits of reduced design investment, reduced validation investment, and faster development cycle time.

This specification shall define attributes and design requirements that are common and critical to the use and deployment of customers and vendors of Enterprise and Cloud Full Width Server rack products. Examples include mechanical form factor, placement guidance of common subsystems and placement guidance of motherboard Input-Output (IO) connections.

5. **References**

The **Data Center – Modular Hardware System (DC-MHS)** family of specifications are written to enable interoperability between key elements of datacenter and enterprise infrastructure by providing consistent interfaces and form factors among modular building blocks. At the time of this publication there are the following specification workstreams:

- **M-FLW** (Modular Hardware System Full Width Specification) – Host Processor Module (HPM) form factor specification optimized for using the full width of a Standard EIA-310-D Rack mountable server. The specification is not limited to use within the EIA-310 Rack but is used to serve as a template for a common target where the design is expected to be utilized.

- **M-DNO** (Modular Hardware System Partial Width Density Optimized Specification) – Host Processor Module (HPM) specification targeted to partial width (i.e. ½ width or ¾ width) form factors. Such form factors are often depth challenged and found not only in enterprise applications but also in Telecommunications, Cloud and Edge Deployments. While the EIA-310 Rack implementation is chosen as a key test case for use, the specification is not limited to use within the EIA-310-D Rack but is used to serve as a template for a common target where the design is expected to be utilized.

- **M-CRPS** (Modular Hardware System Common Redundant Power Supply Specification) – Specifies the power supply solutions and signaling expected to be utilized by DC-MHS compatible systems.

- **M-PIC** (Modular Hardware System Platform Infrastructure Connectivity Specification) – Specifies common elements needed to interface a Host Processor Module (HPM) to the platform/chassis infrastructure elements/subsystems. Examples include power management, control panel and cooling amongst others.
• **M-XIO (Modular Hardware System Extensible I/O)** – Specifies the high-speed connector hardware strategy. An M-XIO source connector enables entry and exit points between sources such as Motherboards, Host Processor Modules & RAID Controllers with peripheral subsystems such as PCIe risers, backplanes, etc. M-XIO includes the connector, high speed and management signal interface details and supported pinouts.

• **M-PESTI (Modular Hardware System Peripheral Sideband Tunneling Interface)** – Specifies a standard method for discovery of subsystems, self-describing attributes, and status (e.g., versus a priori knowledge/hard coding firmware and BIOS for fixed/limited configurations). Examples: vendor/module class, physical connectivity descriptions, add-in card presence, precise source to destination cable coupling determination.

To access additional DC-MHS specification please visit OCP Server WIKI

**Additional References**

This specification also relies on the following Open Compute Project specifications

• OCP Server Network Interface Card (NIC) R3.0 – Specifies NIC card form factors targeting a broad ecosystem of NIC solutions and system use cases.
  - Mezz (NIC) » Open Compute Project

• OCP Datacenter Secure Control Module (DC-SCM) R2.0 – Specifies a SCM designed to interface to an HPM to enable a common management and security infrastructure across platforms within a data center.
  - Hardware Management/Hardware Management Module - OpenCompute
6. Terminology

<table>
<thead>
<tr>
<th>Standardized Term</th>
<th>Meaning</th>
<th>Alternative Terms</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shall</td>
<td>Indicates a requirement for spec compliance</td>
<td></td>
</tr>
<tr>
<td>HPM (Host Processor Module)</td>
<td>PCB or PCBA form-factor being defined by this spec</td>
<td>Motherboard, board</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
<td></td>
</tr>
<tr>
<td>DC-SCM</td>
<td>Datacenter Secure Control Module Rev 2.0 as defined by OCP DC-SCM Rev 2.0 spec</td>
<td></td>
</tr>
<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
<td></td>
</tr>
<tr>
<td>IO</td>
<td>Input Output, commonly referring to high speed connections to a CPU socket.</td>
<td></td>
</tr>
<tr>
<td>PCIe</td>
<td>Peripheral Component Interconnect Express</td>
<td></td>
</tr>
<tr>
<td>CXL</td>
<td>Compute Express Link, open standard for CPU to device and CPU to Memory connections.</td>
<td>Board Pan Sub-pan</td>
</tr>
<tr>
<td>Chassis-Board Bracket</td>
<td>Bracket that attaches to a HPM assembly, that enables a variety of board outlines and hole locations to change over time, and still fit within same chassis base.</td>
<td></td>
</tr>
<tr>
<td>Near</td>
<td>Board location or zone, related to section of board containing DC-SCM Rev 2.0, Management subsystem</td>
<td></td>
</tr>
<tr>
<td>Far</td>
<td>Board location or zone, opposite of location of Management Subsystem</td>
<td></td>
</tr>
<tr>
<td>Platform</td>
<td>Complete system including HPM, power, peripherals, etc</td>
<td></td>
</tr>
<tr>
<td>Compute Core</td>
<td>Elements of board design that are critical to processor and memory support, inclusive of CPU and Memory sockets. Examples are Voltage Regulators, High Speed IO routing, High speed trace routing between multiple processors, high speed trace routing between processors and memory, etc</td>
<td></td>
</tr>
<tr>
<td>Platform Custom Zone</td>
<td>Area of system board where space is allotted for Platform designers to implement custom features.</td>
<td></td>
</tr>
<tr>
<td>HSIO</td>
<td>High Speed IO, commonly referring to PCIe routing, PCIe connectors, CXL routing/connectors, etc.</td>
<td></td>
</tr>
<tr>
<td>OEM</td>
<td>Open Compute Project</td>
<td></td>
</tr>
<tr>
<td>OEM</td>
<td>Original Equipment Manufacturer</td>
<td></td>
</tr>
<tr>
<td>Platform Infrastructure Connectivity Spec</td>
<td>A Specification that defines Platform Interconnect details for features that are common across many HPM Form Factors. Examples connectivity features include fans, backplanes, and control panels.</td>
<td>M-PIC spec</td>
</tr>
<tr>
<td>KOZ</td>
<td>Keep Out Zone, a design term for PCB designs that defines area of a board design where no components may be placed, usually to enable mechanical attachments or mechanical features.</td>
<td></td>
</tr>
<tr>
<td>KIZ</td>
<td>Keep In Zone, a design term for PCB designs that define an zone with a height restriction (such as a volume), which the components selected for that part of the board design must comply with the height restriction of that zone.</td>
<td></td>
</tr>
</tbody>
</table>
7. **Background and Assumptions**

This Full Width HPM Form Factor specification is created to enable typical platform feature sets for both Front and Rear Management, in 1U and 2U chassis applications. Some of the platform features that are common in the industry, and influence the Form Factor constraints are:

a. Chassis installation within minimum EIA-310-D racks (but not limited to).

b. PCIe (Version 5.0 and future) Card configurations typically offered by Enterprise OEMs/Hyperscalers. See **Figure 37. Typical 1U and 2U PCIe Slot Configurations**.

c. In the 1U PCIe offering, only Half-Length PCIe cards (167.6mm) are considered. This does not prevent Three-Quarter Length (254mm) cards, but support for Three-Quarter Length cards would require more restrictive Compute Core placement (not defined).

d. HPM enabled minimum 75W of power per PCIe slot, with ability to scale up to 600W for some slots (likely 3~4).

e. The specification details support for the Open Compute peripherals directly connected to board
   a. OCP NIC R3.0
   b. DC-SCM R2.0
   c. Note: A System is not limited to 1 device of each type; configurations with >1 OCP NIC R3.0 or DC-SCM R2.0 are possible, but outside the scope this specification will cover.

f. Thermal Design Points considerations includes keepout zone to enable air cooling thermal solutions that extend beyond the CPU and Memory sockets. Memory TDPs under consideration are 20W – 25W range.

g. Considerations for Liquid cooling solutions, including CPU cold plates and DIMM liquid cooling manifolds.

h. Considerations for Power Delivery to important chassis subsystems.

7.1. **Rear Management (ie, OEM) Architecture Specific Assumptions**

a. Chassis depth constraints in consideration of
   a. Power Distribution Units placed approximately 780mm from front EIA mounting flange.
   b. Enterprise Storage and Fan subsystems requiring approximately 220mm.
   c. See **Figure 36. Rack Depth Constraints**

b. Sliding rack rails that require a max overall chassis width of 434mm, with interior chassis width/opening of minimum 427mm.

c. Considerations for Power and High-Speed IO Cabling

d. Considerations for Ease of Installation and Removal of motherboard in a chassis.

e. Adequate delivery power through HPM to enable typical Storage configuration power loads (See **Section Power Delivery**)

Date: 04/22/2022
7.2. Front Management (ie, Hyperscale) Architecture Specific Assumptions:

a. 1070mm rack depth
b. All IO generally on cold aisle but may also include some architectures with hot aisle IO. Assuming Front/Near end of system supports IO devices such as PCI CEM, OCP NIC R3.0, SSD’s, etc.
c. PCIe also distributed at Far end, such as to backplane, OAI – Universal Baseboard, and other items.
d. AC or DC rack power supplied by rack from the hot aisle
e. If PSUs are used, they are not hot serviceable
8. HPM Layout

The following Figure 1 shows the layout and approximate locations of major subsystems in the Enterprise and Cloud Full Width HPM.

“Near” and “Far” are reference naming conventions to the side of the board and Compute Core, as to orient the reader as to which portion of the board and Compute Core is being referred to. This specification refers to the Near as where DC-SCM R2.0 Management subsystem resides as a board peripheral. This is also typically referred to Rear IO location for Enterprise products, in which products are designed with IO in the hot aisle of a rack deployment (air exit). This is also typically referred to Front IO location for Hyperscale products, in which products are designed with IO in the cold aisle of a rack deployment (air inlet).

Figure 1. Full Width HPM Layout Diagram
8.1. Two Socket (CPU) Assumptions
The OCP NIC R3.0 subsystem is positioned on the left based on two assumptions:

- In a 2S (CPU) system, the First/Boot CPU in a two CPU motherboard is positioned on left.
- OCP NIC R3.0 is directly routed through the motherboard to the first/boot CPU.

The OCP NIC R3.0 is intended to be closer to this boot CPU to best enable the high-speed IO routing. The OCP NIC R3.0 will usually require higher bandwidth routing, and thus should be optimized for material selection and cost impacts. The routing from first/boot CPU to management subsystem (DC-SCM R2.0) has lower bandwidth requirements, and thus should not be the determining factor in board material selections and routing strategy. See Figure 2.

Figure 2. First CPU position relative to OCP NIC R3.0 and DC SCM R2.0

In this specification the CPU and Memory locations are intentionally not specified. This is for future flexibility in CPU/Memory quantities, locations, sizes, etc. The board area between DC-SCM R2.0 and OCP NIC R3.0 is designated as a “Platform Custom Zone”, as shown in Figure 1. Full Width HPM Layout Diagram. The goal is to provide board area and system volume for individual platforms to provide system specific features.

8.2. One Socket Assumptions
In theory, for a one socket (CPU) platform, the OCP NIC R3.0 location does not have a strong affinity to either side. **The OCP NIC R3.0 shall remain in the specified HPM location for chassis compatibility for all Full Width HPM products.**
9. Mechanical Requirements

9.1. HPM Outline

The Full Width HPM (FLW) Outline is defined as the required HPM size, outline and peripheral locations to fit compute core and IO elements in an FLW compliant chassis. This is intended to fit a wide variety of Platform and Chassis applications.

The Full Width HPM Common Area Outline is defined in Figure 3 Full Width HPM Outline below. Units are Inches [mm]. The intent is to show overall dimensions of board outline. No tolerances are to be implied. DFX/CAD files will be in 13.7 CAD files, and subsequent package releases.

Figure 3. Full Width HPM Outline
9.2. Board Datum and Mounting holes

A set of six required board mounting holes specified shall be implemented around the board perimeter. These six board mounting holes interface to the Chassis-to-Board Bracket (Board Pan). Other optional board holes are allowed as needed, to ensure appropriate mechanical support of the Compute Core (not shown). These additional board holes are expected to interface to the board-chassis bracketry and should be designed in consideration of the bracket to chassis interface features, as defined in Section 9.4.

A design should follow good engineering practices and in consideration of Platform Shock and Vibration requirements. Shock and Vibration requirements are not in scope of this specification.

Figure 4. Board Mounting Holes
9.3. HPM Board and Assembly Thickness

The maximum board thickness allowed shall be 3.18mm nominal, assuming +10% max tolerance. HPM Thickness choices may have impacts on chassis stackup. HPM thickness must consider the backing plate thickness of a required Core Compute. **HPM designers shall consider that a recommended maximum allowable HPM thickness + backing plate stackup is 5.86mm.** Backing plates are assumed to be allowed to protrude thru cuts in the Chassis-to-Board bracketry.

**Figure 5** and **Table 1** below demonstrate example scenarios HPM designers should consider when choosing HPM thickness.

**Table 1. Board and Chassis Stackup Scenarios**

<table>
<thead>
<tr>
<th>(Dimensions in mm)</th>
<th>1 HPM Height</th>
<th>2 HPM Thickness</th>
<th>3 Backplate</th>
<th>5 Gap Backplate to Base Chassis</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical Nominal Range</td>
<td>5.0 - 5.86</td>
<td>1.57 - 3.18</td>
<td>2.0 – 2.6</td>
<td></td>
</tr>
<tr>
<td>Scenario 1 Nominal</td>
<td>5.2</td>
<td>2.6</td>
<td>2.2</td>
<td>0.4mm</td>
</tr>
<tr>
<td>Scenario 2 Nominal</td>
<td>5.86</td>
<td>3.18</td>
<td>2.6</td>
<td>0.08mm</td>
</tr>
<tr>
<td>Worst case Gap 5 scenario</td>
<td>5.5</td>
<td>3.5</td>
<td>~2.0mm</td>
<td>0</td>
</tr>
</tbody>
</table>

Gap 4 not shown as it depends on customer chassis geometry
Implementors Note:

Designers should consider that variations in HPM thickness can result in variation of the offset locations of OCP NIC R3.0 and DC SCM R2.0 peripherals (relative to fixed chassis openings).

There are some common connectors (some offset) in the industry that should be taken into consideration when designing an HPM, Chassis and associated heights of HPM and peripherals.

Designers may consult with vendors of SFF-TA-1002 4c+ to determine best options for their chassis application.

See Figure 6. HPM thickness and Straddle Mount Peripheral Offsets

---

**Figure 6. HPM thickness and Straddle Mount Peripheral Offsets**

**4C+ Straddle Mount Connector Offset Examples**

<table>
<thead>
<tr>
<th>HPM Thickness – t (mm [in])</th>
<th>Peripheral Midplane Offset Required for Z = 0.49 (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.57mm [.062&quot;]</td>
<td>-.49mm</td>
</tr>
<tr>
<td>1.93mm [.076&quot;]</td>
<td>-.31mm</td>
</tr>
<tr>
<td>2.36mm [.093&quot;]</td>
<td>-.055mm</td>
</tr>
<tr>
<td>2.55mm [.100&quot;]</td>
<td>0mm</td>
</tr>
<tr>
<td>2.67mm [.105&quot;]</td>
<td>+.08mm</td>
</tr>
<tr>
<td>2.79mm [.110&quot;]</td>
<td>+.12mm</td>
</tr>
</tbody>
</table>
9.4. HPM to Chassis Retention

The HPM and Chassis-to-Board Bracket assembly requires retention to the chassis base. **There shall be a hole required in board to be used for motherboard retention to the chassis.** The hole is sized for common retention methods such as plungers, thumbscrews, etc, as shown in **Figure 7** below.

**Figure 7. HPM Assembly to Chassis Retention Enablement**

9.4.1. Keep out zone for Retention Hardware

A keepout zone shall be implemented on both topside and bottom side around the Retention Hardware hole.

The Primary (or Topside) KOZ is defined in **Figure 19. Zones for Primary Side Component Height Restrictions**.

For Secondary side KOZ, refer to **Figure 21. Motherboard Secondary Side HPM Zero-Height Keep Out Zones for Chassis to Board Bracketry**
9.5. HPM Handling

The FLW HPM shall require a hole interface to a mechanical handle. This handle solution may be implemented with but not limited to a plastic handle. An example is shown in Figure 8.

Figure 8. HPM Handling Feature
A board hole example is shown in Figure 9. The hole location for this handle shall be provided near the Far side edge of the Compute Core in the HPM. The handle may utilize an existing Far side hole, except for the corners. The location of the hole on the Far side is not specified but should be placed considering Compute Core details, such as Far High-Speed IO cabling, and Thermal solution keep outs. To balance handling of board with Chassis Retention feature (near DC SCM R2.0), it is preferred to place the handle feature to left half of the HPM.

Figure 9. HPM Handling Feature Location

A board hole shall be provided near the Far Edge to enable a mechanical handle feature to be installed. The location is not required. Left of Center location is preferred.
9.6. Common Peripheral Location Requirements
There are key peripheral subsystems that connect directly to the Full Width HPM.

- OCP NIC R3.0 (Near)
- DC-SCM R2.0 (Near)
- Control Panel connections (Far)

9.6.1. Near Edge Peripheral Locations
The centerline location of each of the connector subsystems is defined in Figure 10. For further details of how the connector centerlines are defined, refer to SFF-TA-1002 specification.

Figure 10. Centerline Locations of OCP NIC R3.0 and DC-SCM R2.0
9.6.2. Far EdgePeripheral Connections

The HPM shall implement 2 instances of the M-PIC defined Control Panel connections as shown in Figure 11. Control Panel Connection Locations. See Section 11.5 for connector details.

Figure 11. Control Panel Connection Locations
9.7. Internal USB Connection

The HPM shall implement an internal USB3 connector. The connector must be placed in the HPM within the zone defined by Figure 12. The USB Connector details are further defined in Section 11.2 and the M-PIC specification.

Figure 12. USB Connection Placement Zone
9.8. Intrusion Switch Connection

The HPM shall implement a connector for a Chassis Intrusion Switch. The Intrusion connector must be placed in the HPM within the zone defined in Figure 13. The Intrusion Switch Connector details are further defined in Section 11.3 and the M-PIC specification.

Figure 13. Placement Zone for Intrusion Switch Connector
9.9. Boot Storage Peripheral Connection

The HPM is recommended to implement a Boot Storage Peripheral connector. The connector must be placed in the HPM within the zone defined by Figure 14. The Boot Storage Peripheral Connector details are further defined in Section 11.4 and the M-PIC specification.

Figure 14. Placement Zone for Boot Peripheral Connector
9.10. Near IO Riser-Cable Connector Placement

The HPM shall implement High Speed XIO connectors that are intended to be used for IO Riser subsystems or Cabled High speed IO. The recommended connectors have power integrated with High-speed IO (for use with risers). The following set of requirements and recommendations shall be followed by the HPM design. These requirements enable:

- Blind mating and docking of riser cards
- Enable Chassis, Riser, or Other IO Mechanical subsystem Reuse between generations of HPMs.
- Future Higher Power Compute Cores
- Ability to cable High Speed IO from these connectors, as an alternative to mechanical subsystems.

9.10.1. Near IO Riser Cable Connector Requirements

1. An HPM shall implement the Near IO Riser-Cable connectors within the Near IO Keep In Zone, defined in Figure 15.

2. The X Dimensions in Figure 15 shall be followed for Spec Compliance.
   - This methodology ensures compatibility with PCIe Add In Card configurations, as well as future Compute Core fit within the FLW outline.
   - These connectors are fixed horizontally (X – direction) because they are set to accept fixed PCIe Riser configurations.
   - Typical Configuration assumptions and background information on these location choice requirements are detailed in Section 13.3

3. The X-direction dimensions indicate riser centerlines. If a chosen connector centerline is offset from the riser card centerline, the designer must adjust connector location to accomplish the Riser centerlines.
   - Offset connectors may exceed the X-direction width of the recommended Keep In Zone, as long as Riser Centerlines are maintained per Figure 15.

4. Mechanical Retention holes associated with each IO connector position are detailed in Section 9.12 Mounting Hole Requirements for IO Module Retention
9.10.2. Near IO Riser Cable Connector Recommendations and Guidance

1) If a HPM contains more Near IO ports than the 6x required connectors, additional connectors may be placed in the Near area at discretion of the designer. Considerations should be made to ensure additional connectors can be accessed and cabled to the Far direction.

2) Connector Choice and Y-dimension attributes are left flexible in the spec to enable future technology advances in IO (speed, bandwidth) to be supported with connector technology improvements and offerings.

3) HPM shall follow a Required Keep In Zone as defined in Figure 15, especially to provide Y-dimension guidance. Following the Y-dimension limits of the Keep In Zone will enable future compatibility to 1U PCIe Add-in Cards, and allow HPM layout room for Future Compute Cores.
A summary of the Fixed vs Flexible choices in Near IO is summarized in Table 2.

<table>
<thead>
<tr>
<th>Item</th>
<th>Fixed</th>
<th>Flexible Choice</th>
</tr>
</thead>
<tbody>
<tr>
<td>Connector Choice</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>.................................</td>
<td></td>
<td>Recommended Connectors are Defined in Section 11.1, and defined in the M-XIO specification</td>
</tr>
<tr>
<td>X-dimension location</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Y-dimension location</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>.................................</td>
<td></td>
<td>(Recommend to place within Near IO Keep In Zone)</td>
</tr>
<tr>
<td>Retention hole X-Y location</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Additional IO connector locations, beyond those specified</td>
<td></td>
<td>X</td>
</tr>
</tbody>
</table>

BOM Population Note:

Custom BOM Population choices are made at the discretion of a customer and are not covered by this specification. (This includes any depopulation choices for cost savings.)
4) A recommended connector choice is the Amphenol G03V213X2HR (or equiv) with a recommended placement shown in Figure 16

Figure 16. Reference Locations of Recommended Near IOs for Amphenol G03V213X2HR

- This diagram is a REFERENCE to follow when implementations are using the Recommended Near IO connector.
- All measurements are with respect to datum mounting hole
- All measurements are to riser PCB centerline
- High Speed Connector recommendations are detailed further in Section 11.1
9.11. Far Side IO Connector Placement
The Far Side IO connector locations referenced in Figure 1. Full Width HPM Layout Diagram are not specified because they are all assumed to be cable-only connections and will not have major dependencies to chassis or subsystem reuse compatibility.

9.12. Mounting Hole Requirements for IO Module Retention
The HPM shall implement mounting holes associated with each Near IO module location.

Hole Implementation Note:
An M-FLW compliant HPM must implement both 1U and 2U IO Module Retention holes.

These are intended to be used for mechanical module retention (such as PCIe Risers, or other modules that require mechanical retention in the HPM area). There is a total of 7x holes associated with the 6x IO connectors. These mounting holes are associated with both 1U (Figure 17) and 2U (Figure 18) PCIe Riser configurations. The motherboard requires a 3.68mm diameter hole. Chassis designers may choose the hardware and utilization method for riser retention.

For further explanation on which mounting holes are associated with its Near IO connectors, see Figure 39. Riser Retention Holes and Associated Near XIO Locations in the Supplemental Information section.
Figure 17. 1U IO Module Retention Enablement Holes

Figure 18. 2U IO Module Retention Enablement Holes
9.13. Primary Side Component Height Restriction Zones

**A Component Height Restriction Zone shall be required.** The purposes are to enable:

1. Thermal solutions to interface to Compute Core items such as CPU and DIMMs (not shown). Thermal solutions in scope include extended air heatsinks and liquid cooling solutions.
2. Cable routing channels along HPM edges
3. PCIe CEM cards on 1U risers

For thermal solutions, one must consider the allowable variance in numbers, types, and location of Compute Core items. Thus, a fixed 12mm for Component Height Restriction in the Central Core area is intended to allow air cooling heatsinks, or liquid cooling hardware of any variance. DIMM sockets are exempt from the 12mm Component Height Restriction. All other soldered board components must comply.

If a cable connection (power, High speed IO, etc) is placed in the Component Height Restriction Zone, the max height restriction shall apply to the mated height of the plug and cable assembly.

Figure 19. Zones for Primary Side Component Height Restrictions

9.14.1. Overall Secondary side Keep In Zone Requirements

The Back side or Secondary side of the HPM shall have a universal Keep In Zone Height Restriction of 1.6 mm, unless otherwise specified in the areas of 0 height zones. This is to ensure clearance to chassis componentry. This is especially important with a max allowable board thickness defined in Section 9.3.

9.14.2. Chassis-to-Board Bracket (Board Pan) Requirements, and KOZs.

The Full Width HPM shall be designed to fit a Chassis-to-Board Bracket (Board Pan), that enables different board layouts and mounting hole locations between different Compute Core designs, while still maintaining compatibility to a common chassis design. See Figure 20

On the HPM, there will be required locations for chassis hook features that interface between chassis base and the Chassis-to-Board Bracket. These hook locations require HPM secondary side (bottom side) zero-height keep out zones, as specified in Figure 21. Motherboard Secondary Side HPM Zero-Height Keep Out Zones for Chassis to Board Bracketry

![Figure 20. Example of Chassis-to-Board Bracket (Board Pan)](image)
The Keep Out Zones defined in Detail E of Figure 21 are to allow Chassis Base hook geometry to interface the cutouts on the Chassis to Board Bracket. See example in Figure 41. Chassis Base Geometry to Interface Chassis-to-Board Bracketry. The geometry of the Board Bracket is not specified and is a design choice for chassis designer.


In some instances, an HPM designer or System designer, may desire tall secondary side components (such as special capacitors) that exceed the Secondary Side height restriction. Although this should be avoided, a designer may implement local exceptions if the following conditions can be met:

1) Exceptions are contained to small areas of the Secondary side, not to exceed 400mm² area per instance.

2) No two instances of exception are closer than 10mm, as to not drive excess cutouts in Chassis-to-Board bracketry.

3) The Chassis-to-board bracketry can be cutout to accommodate these exceptions.

4) **The HPM thickness + backside component shall not exceed 5.86mm**
9.15. Liquid Cooling Bracketry Keep Out Zones

There shall be keepouts around the Far side board mounting holes to enable bracket mounting to the HPM. These brackets may be needed for systems that wish to mount liquid cooling components, such as DIMM liquid manifolds, or large radiator assemblies.

These keepouts shall be complied with, regardless of a specific board or platforms cooling designs or plans. The details are in Figure 22. Liquid Cooling Bracket Keep Outs.

Figure 22. Liquid Cooling Bracket Keep Outs
9.16. Cabling Enablement Keep Out Zones

There shall be a keep out zone to left and right of outermost DIMM sockets with a minimum dimension to motherboard edge of 8.6mm. This keep out is to enable HSIO cabling, Power cabling and other Platform infrastructure cabling to traverse from Near to Far zones, as needed by Platform designs. (Due to differences in DIMM socket widths from various vendors, DIMM placement restriction may also be considered as a minimum distance of 12.1mm to the centerline of the DIMM socket.

This Keep Out Zone is shown in Figure 19. Zones for Primary Side Component Height Restrictions

**Implementation Note:**

In some cases, a Compute Core design may only be able to deliver a desired capability by violating the cable keep out zone. By doing so, an HPM will cause issue with a Platforms ability to cable High Speed IO and Power delivery. In this case, a designer should make efforts to collaborate with Platform Designers on:

1. Increasing Near to Far Power delivery and Power Egress capability, to mitigate loss of power cabling
2. Identify available cabling space for High-speed IO to meet a given Platform configuration
10. Power Delivery

The Full Width HPM is powered from a 12V DC source. This specification does not cover alternate PSU voltage sources (e.g., 48V DC implementations).

10.1. HPM Power Zones

The HPM supports multiple power zones where significant power delivery and connectivity is expected. Figure 23 illustrates locations of power zones on the HPM. Details of each zone are described below, some are ingress, some are egress from the HPM.

Figure 23. HPM Power Zone locations
Table 3. Power Delivery Zones

<table>
<thead>
<tr>
<th>Zone</th>
<th>Feature</th>
<th>Typical Usage</th>
<th>Connector Power Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zone A</td>
<td>M-CRPS Connector</td>
<td>Ingress</td>
<td>3200W</td>
</tr>
<tr>
<td>Zone B</td>
<td>2x6+12s PICPWR</td>
<td>Egress</td>
<td>864W</td>
</tr>
<tr>
<td>Zone C</td>
<td>Near Side Riser PICPWR</td>
<td>Egress</td>
<td>180W</td>
</tr>
<tr>
<td>Zone D</td>
<td>DC-SCM R2.0</td>
<td>Egress</td>
<td>50W</td>
</tr>
<tr>
<td>Zone E</td>
<td>OCP NIC R3.0 + Platform Custom Zone</td>
<td>Egress</td>
<td>150W</td>
</tr>
</tbody>
</table>

10.1.1. Zone A – M-CRPS Connector

- Power Connector Type: M-CRPS 73.5mm Connector (Figure 24). Manufacturer P/N: Amphenol HPG36P14SRT051T; Bellwether 70278-7015; TE 2407532-2. Refer to M-CRPS specification for additional implementation details.
- Connector Power Rating: 3200W
- Typical usage: Power ingress
- Please refer to connector vendors or [document TBD] for part numbers that best meet the application.
- Refer to M-PIC Specification for additional details.

Locations of M-CRPS connectors shall be placed as defined in Figure 25. M-CRPS Connector Location Requirements

Figure 24. M-CRPS Power Connector
10.1.2. Zone B – 2x6+12s PICPWR

- Power Connector Type: 2x6+6s PICPWR Vertical Header or Right-Angle Header (Figure 26. 2x6+12s PICPWR Power Connectors).
  - Manufacturer P/N:
    - Bellwether Vertical Header 70368-122*
    - Bellwether RA Header 70367-122*
    - Note, these connector part numbers are current as of publication. Please refer to connector vendors or [document TBD] for part numbers that best meet the application.
    - Refer to M-PIC Specification for additional details.
- Connector Power Rating: 864W
- Typical usage: Power egress to peripherals
The HPM shall implement PICPWR connectors at locations defined in Figure 27. Note: HPM shall implement these connector footprints (but can be depopulated in assembly BOM at a Design Spec level guidance.)

Figure 26. 2x6+12s PICPWR Power Connectors

Figure 27 PICPWR connector (2x6+12s) Location Requirement (6 locations)
10.1.3. Zone C – Near Side Riser PICPWR Egress

- Power Connector Type: Amphenol G03V213X2HR
- Connector Power Rating: 180W
- Typical usage: Power egress for up to 2x 75W CEM PCIe devices

Please refer to connector vendors or [document TBD] for part numbers that best meet the application.

Refer to M-PIC Specification for additional details.

Refer to Section 9.10 for additional details on near side connector and location. Refer to Section 11.1 High Speed IO (HSIO) connectors for details of the recommended Near IO connector with Integrated power.

The Egress Near Riser Power Zone provides power to PCIe devices on risers. This specification does not cover direct dock CEM implementation (non-riser approach). The HPM provides 12V_PRIMARY to the Egress Near Riser Power Zone.

75W Slot power, detailed in Table 4, is provided for each PCIe CEM slot on all PCIe risers. The PCIe riser enables a +3.3Vaux and +3.3V (Vcc3_3) power sources derived from the 12V_PRIMARY source from the HPM.

**Table 4. Minimum HPM Power Supply Rail Requirements per PCIe CEM Slot**

<table>
<thead>
<tr>
<th>Power Rail</th>
<th>75 W Slot&lt;sup&gt;2&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>+3.3Vaux</td>
<td>Generated on PCIe riser. Derived from 12V_PRIMARY</td>
</tr>
<tr>
<td>+3.3V (Vcc3_3)</td>
<td>Generated on PCIe riser. Derived from 12V_PRIMARY</td>
</tr>
<tr>
<td>12V_PRIMARY</td>
<td>Generated on PCIe riser. Derived from 12V_PRIMARY</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>12V nominal</td>
<td>7.25A total:</td>
</tr>
<tr>
<td></td>
<td>5.5 A (CEM 5.0) +</td>
</tr>
<tr>
<td></td>
<td>~1.0A (VR conversion to Vcc3_3) +</td>
</tr>
<tr>
<td></td>
<td>~0.35A (VR conversion to +3.3Vaux) +</td>
</tr>
<tr>
<td></td>
<td>~0.40A (misc.)</td>
</tr>
</tbody>
</table>

Note 1: see M-PIC specification for definition of 12V_PRIMARY

Note 2: Additional power is provided to each CEM slot beyond PCIe CEM 5.0 specification to budget for miscellaneous logic on risers and VR conversion losses. Effective total power is 87W per slot.

10.1.4. Zone D – DC-SCM R2.0

- Connector Type: See OCP DC-SCM R2.0 specification
- Connector Power Rating: 50W
- Typical usage: See OCP DC-SCM R2.0 specification

10.1.5. Zone E – OCP NIC R3.0 and Platform Custom Zone

- Power Connector Type: See OCP NIC R3.0 spec
- Connector Power Rating: 150W
- Typical usage: Power egress for OCP and any subsystem inside the Platform Custom Zone
10.2. HPM Power Planes

The HPM power planes (and supplementary power delivery mechanisms like cables) have the following features:

- At maximum load, the HPM power shapes temperatures have a maximum of 30°C T-rise and do not exceed 100°C absolute.
- At maximum load, the maximum HPM voltage drop (IR loss) between power sources and associated loads or connectors is less than or equal to 1%.
- Any load (operating up to its maximum power rating) in the platform can be powered with a single operational power source (e.g. PSU), where the total of all loads does not exceed the capacity of the power planes as defined in Table 5.
- The HPM should implement fusing to prevent damage to connector and traces.

Three checkpoint areas have been defined on the HPM (see Figure 28 Power Plane (and supplementary power delivery mechanisms) Checkpoint Areas):

1) NORTH-SOUTH power delivery checkpoint
2) EAST-WEST NEAR SIDE power delivery checkpoint
3) EAST-WEST FAR SIDE power delivery checkpoint

The sum of all 12V_PRIMARY power planes (and supplementary power delivery mechanisms) INSIDE the cross-sectional areas of the HPM defined by the power delivery checkpoints must meet the minimum power delivery capacity requirements defined in Table 5.

Note 1: see M-PIC specification for definition of 12V_PRIMARY

<table>
<thead>
<tr>
<th>Power Plane Checkpoint</th>
<th>Minimum Power Delivery Capacity</th>
</tr>
</thead>
<tbody>
<tr>
<td>NORTH-SOUTH</td>
<td>2800W</td>
</tr>
<tr>
<td>EAST-WEST NEAR SIDE</td>
<td>2400W</td>
</tr>
<tr>
<td>EAST-WEST FAR SIDE</td>
<td>864W</td>
</tr>
</tbody>
</table>
Figure 28 Power Plane (and supplementary power delivery mechanisms) Checkpoint Areas
11. I/O System (Electrical Interfaces)

The HPM shall implement electrical interfaces in compliance with the DC-MHS family of specifications. Refer to Section 5 for additional details. This section provides additional guidance for specific connectors on the Full Width HPM.

11.1. High Speed IO (HSIO) connectors

HSIO connector selections are strongly recommended, but not required for compliance. Use of the recommended HSIO connectors will ensure broader compatibility with chassis, risers and cable interfaces in the future. The selection is intentionally not stated as “required” so the specification allows for future selection of new connector technologies, as may be required by IO speeds and bandwidth changes in future generations of HPM.

Requirement: Connector Choices must be compliant XIO specification.

<table>
<thead>
<tr>
<th>Near HSIO</th>
<th>Amphenol G03V213X2HR</th>
<th>Appropriate for both cable and riser usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Far HSIO</td>
<td>SFF-TA-1026</td>
<td>Appropriate due to low profile and ability to fit under thermal solutions</td>
</tr>
</tbody>
</table>

The Near HSIO location and flexibility is further described in Section 9.10.

11.2. Internal USB

- M-PIC Section Reference: “Internal USB3 Connector”
- Connector Requirement: The HPM shall implement an internal USB connector.
- Connector Placement: See Section 9.7

11.3. MHS Intrusion Switch

- M-PIC Section Reference: “Intrusion Switch”
- Connector Requirement: The HPM shall implement a connector for a Chassis Intrusion Switch.
- Connector Placement: See Section 9.8

11.4. MHS Boot Storage Peripheral Connection

- M-PIC Section Reference: “Boot Storage Peripheral”
- Connector Requirement: The HPM is recommended to implement a Boot Storage Peripheral connector.
- Connector Placement: See Section 9.9

11.5. MHS Control Panel Connectors

The FLW HPM shall implement the “HPM to Control Panel” connections defined in the M-PIC specification. The connections shall be implemented in locations defined by Figure 11. Control Panel Connection Locations.
12. Adapted FLW HPMs

The goal of the FLW specification is for a single HPM form factor to be used in many industry chassis solutions and support many Compute Cores. However, there may exist instances where adaptation of HPM's for unique chassis and system capabilities is desired.

This section shall define Open and Standardized Adaptations of the FLW HPM specification.

An Adapted HPM shall have the following requirements:

a) The Compute Core area of the FLW layout shall not be changed in a way that drives Core Computes to be different between Standard FLW and Adapted FLW.

b) Augmentation in overall size should be considered to enable unique system interfaces
   a. Helps not impact Compute Cores

 c) Adapted HPM’s should not grow beyond 385mm (this is still TBD) in total length
    (measured from the from Near Edge OCP NIC R3.0 edge to Far Edge).

An Adapted HPM may have the following attributes:

d) Modifications may transcend FLW base spec, to enable new applications (beyond FLW assumed environments).

e) May have unique Peripheral requirements.

Future Adapted HPMs will be documented in this section if productized and accepted in future FLW Revisions.

12.1. UBB / Blade FLW Adapted HPM Requirements

UBB Blade FLW Adapted HPM architecture leverages the base HPM specifications. Modifications for the UBB Blade Adaptation are focused at the Far side area to optimize Power Delivery and IO connections meant for UBB Blade implementation.

In Blade implementation, blind-mate panel mountable connectors and their specific locations are required. These details are included in this Section.

12.1.1. UBB Blade FLW HPM Outline

UBB Blade FLW HPM Outline is an extension of the base outline listed in Section 9 Mechanical Requirements. The Far edge dimension of the base outline is extended by 38.11mm [1.5"] to accommodate blind mate IO connectors, Power connector and Blind-mate guide pins to achieve reliable docking with panel-mount connections. This is shown in Figure 29. Full Width HPM Outline for UBB and Blade.
12.1.2. Blade High Speed IO connector

High Speed IO connector outline shown in Figure 29 is based on Amphenol Examax family or equivalent. There are seven 4x8 Examax shown from left to right and the one in far right is shown as 6x8 Examax to include extra clock and signals.

The connectors pin-out would be included in M-XIO specification

The specification defines the position of the Examax connector to allow flexibility for implementors to select board or cable connector version to be chosen.

Date: 04/22/2022
Table 6 Blade Far/South High Speed IO recommended connectors

<table>
<thead>
<tr>
<th>Connector family</th>
<th>Company</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Examax / Examax 2</td>
<td>Amphenol or Equivalent</td>
<td>4 pairs X 8 columns</td>
</tr>
<tr>
<td>Examax / Examax 2</td>
<td>Amphenol or Equivalent</td>
<td>6 pairs X 8 columns</td>
</tr>
</tbody>
</table>

Figure 30 Examax 4x8 connector

Figure 31 Examax 6x8 connector
12.1.3. Ingress Power Connector

Far power connector shown in Figure 32 is based on Amphenol Power Blade Plus or equivalent. The configuration is 3 high-power contacts on each side with 12 signal contacts in the middle.

The connector is capable of up to 2000W with 12V input voltage. The connector pin-out would be included in M-PIC specification and leverage PICPWR connector pin definition.

Table 7 Blade Far/South Ingress Power recommended connector

<table>
<thead>
<tr>
<th>Connector family</th>
<th>Company</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Blade Plus</td>
<td>Amphenol 10106263-6003003LF or Equivalent</td>
<td>3 High Power + 12 Signals + 3 High Power</td>
</tr>
</tbody>
</table>

Figure 32 Power Blade Plus Ingress Power Connector

12.1.4. Blade Minimum Power Plane Capacity Requirements

Blade Far side power delivery ingress is intended to heavily leverage existing power delivery capacity in base HPM definition. As such, the bulk of power delivery capacity requirements
shall follow requirements currently defined in Far-side PICPWR connector (see 10.1.2 Zone B – 2x6+12s PICPWR). The PICPWR connectors at the far side will be de-populated.

To ensure the UBB Blade Adaptation has sufficient power delivery capacity at the Far area, Blade left and right, the Power Delivery Checkpoint area and its minimum capacity requirements are defined in Figure 33 and Table 8

Table 8 Blade Minimum Power Plane Capacity Requirements

<table>
<thead>
<tr>
<th>Power Plane Checkpoint</th>
<th>Minimum Power Delivery Capacity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Blade West</td>
<td>1100W</td>
</tr>
<tr>
<td>Blade East</td>
<td>1100W</td>
</tr>
</tbody>
</table>

Figure 33 Blade Power Plane Checkpoint Areas

12.1.5. Blade Mechanical Guide Pin

The outline shown in Figure 29 also includes a position identified for a mechanical guide pin for blind mate alignment. The HPM shall implement this feature for safe blind mate implementation.
13. Supplemental Information

13.1. Alternate HPM Outlines for OCP NIC R3.0
Alternate HPM outlines may be utilized by customers for unique requirements. These alternatives may not be compatible with chassis designed to the Base FLW outline. These alternatives are intended to improve compatibility for chassis and HPMs that can align to these options.

<table>
<thead>
<tr>
<th>Alt Outline Name</th>
<th>Key Difference from Base</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Near Edge Cabled NIC outline</td>
<td>HPM outline modification to detach OCP NIC R3.0</td>
<td>Figure 34</td>
</tr>
<tr>
<td>Near Edge OCP NIC LFF support</td>
<td>HPM Outline modification to enable 2x of the OCP NIC R3.0 connectors for full support of LFF form factor (SFF-TA-1002, 4C+ connectors)</td>
<td>Figure 35</td>
</tr>
</tbody>
</table>

A Platform may wish to NOT have OCP NIC R3.0 direct dock to the HPM. For Chassis compatibility, it is assumed the Platform’s OCP NIC R3.0 is to be cabled in the same mechanical location of a chassis that is compliant to this specification. In Figure 34, Outline Cutout modification to Enable Cabled OCP NIC R3.0 in Base Outline the outline cutout change (material removal) is prescribed to enable an OCP NIC R3.0 card.

The cable assembly (including PCB with OCP NIC R3.0 connector) is assumed to be placed and fixed in the same location Platform/chassis as the direct dock OCP NIC R3.0 placement required in Figure 10. Centerline Locations of OCP NIC R3.0 and DC-SCM R2.0.
Figure 34. Outline Cutout modification to Enable Cabled OCP NIC R3.0 in Base Outline

Figure 35. Alternate Outline to Enable OCP NIC R3.0 LFF
13.2. Rack and Chassis Depth Stackup Assumptions

The HPM spec is constructed under the considerations that the installation environment has a Power Distribution Unit approximately 780mm from the front EIA flange. Although platforms may vary in depth, the board size constraint is chosen to enable typical chassis storage systems using this HPM spec to fit with a Cable Management arm, in less than the 780mm PDU constraint.

Figure 36. Rack Depth Constraints

- Rear Management Compute and IO (motherboard)
- Storage and Fans ~220mm
- Motherboard 480mm
- Rear Door
- Front Door
- Typical PDU locations in 1070, 1100, 1200mm racks
- CMA and cabling space ~80mm

Date: 04/22/2022
13.3.  1U and 2U PCIe Slot Typical Configurations

The following images in Figure 37 are of typical Enterprise 1U and 2U PCIe Slot Configurations.

Figure 37. Typical 1U and 2U PCIe Slot Configurations for Rear Management System
The following images in **Figure 38** are of typical Hyperscale 1U and 2U PCIe Slot Configurations. Note, these are 19" FrontIO chassis like OCP Mt. Olympus. Also, the front can be shuffled around using an extra "adapter board" like **Figure 40** not covered by the HPM spec.

**Figure 38. Typical 1U and 2U PCIe Slot Configurations for Front Management System**
13.4. Additional Information on Near IO Riser Retention Holes

In a system configuration that uses riser cards in the Near IO, mechanical retention is enabled by holes in the HPM, near each Near IO location. The following Figure 39 demonstrates the riser retention holes and which Near IO position each hole is associated with.

Figure 39. Riser Retention Holes and Associated Near XIO Locations
13.5. Reference System Architecture in 21” Chassis

Figure 40 shows how the Base Outline HPM can be utilized in a 21” chassis architecture, including if Power Supply Infrastructure is on the Far Side with cables to the near side power Ingress.

Figure 40. Base Outline HPM used in 21” Reference Chassis

13.6. Chassis Base Geometry for Chassis-to-Board Bracket interface

Figure 41 demonstrates example geometry required in the chassis base to interface to the Chassis-to-Board bracketry in Figure 20. Example of Chassis-to-Board Bracket (Board Pan). The exact geometry is not specified, but considerations must be made for maximum board thickness (see Section 9.3) and HPM Keepout Zone sizes (See Section 9.4).
13.7. CAD files
This will be filled out at version 1.0.

14. Appendix A - Checklist for IC approval of this specification (to be completed by contributor(s) of this Spec)
Complete all the checklist items in the table with links to the section where it is described in this spec or an external document.
This will be filled out at version 1.0.

15. Appendix B-<supplier name>- OCP Supplier Information and Hardware Product Recognition Checklist
(to be provided by each supplier seeking OCP recognition for a Hardware Product based on this specification)
This will be filled out at version 1.0.