Founded in 1988
by the merger of SDA Systems, Inc. and ECAD, Inc.

Lip-Bu Tan, CEO

Revenue
$2.3B*

Employees
~8,000

Countries
20

Software and Programming

Industry

Exceed customer expectations
Explore what’s possible
Execute with quality
Elevate the team

Culture

Source: Cadence Earnings Press Release, Q4 2019

*Estimated 2019 revenue, actual revenue may differ.
Cadence at a Glance

4,500+
R&D ENGINEERS

1750+
FIELD ENGINEERS

R&D INVESTMENT
$884M

PATENTS WORLDWIDE
1600+

26 GLOBAL DEVELOPMENT CENTERS

All data as of end of Q4 2018
# Cadence Solution Offerings

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<td>Digital Logic Implementation</td>
<td>Processor and Interface IP</td>
<td>SoC Functional Verification</td>
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Cadence *Intelligent System Design Strategy*…

**Thinking Outside The Chip**

- **Pervasive Intelligence**
- **System Innovation**
- **Design Excellence**

- **Front-to-Back PCB Design**
- **Multi-Chip(let) Advanced Packaging**
- **System-Level Electrical/Thermal Modeling & Analysis**
- **Embedded Software and Security**
- **Analog and RF IC**
- **Full-Flow Digital IC**
- **Verification Suite**
- **Interface and Processor IP**
- **Machine Learning**
- **Artificial Intelligence**
- **Fully Automated Place and Route**

**Cloud Enabled — Partnerships with Ecosystem Leaders**
The Beginning of the “More Than Moore” Era

• For the past five decades, the electronic industry has thrived while enjoying the benefits of Moore’s Law. But things are changing…The economics of semiconductor logic scaling are gone.

• Gordon Moore knew this day would come. He also predicted that "It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected”.

• Heterogeneously integrated packaging (SiP) will be leveraged to design the next generation of electronic products:
  • SiP will replace SoC

• The generation of “More Than Moore” is here…
Is Moore’s Law Already Dead?

- It’s more than the limitations of physics…
- Cost per transistor has steadily increased since 2012/3 (28nm)
- Designing chips at the latest nodes is hard and expensive
  - Low-volume businesses can’t justify the NRE costs of designing an SoC at the latest node
  - Requires huge teams of engineering specialists that aren’t always easy to find
  - Systems and software companies now designing chips and challenging the status quo of SoC approach
- Todays SoC’s are reaching reticle limits…but big chips don’t yield anyways
- More Analog/RF content in today’s designs.
  - Analog/RF never have benefited from Moore’s Law
More Than Moore Example…

- Processor to memory latency reduction
  - Stack thinned memory chips with controller
  - Place memory stacks very close to processor on silicon interposer (2.5D IC)
  - Dramatic reduction in size
  - Simplifies board-level design
  - Drastic reduction in latency
  - Reduction in power
  - Thermal needs proper consideration
Transitioning to “More than Moore”…Heterogeneous Integration

• SiP becomes the new SoC?
  – Modular approach vs monolithic approach
    – Not everything needs to be designed in the same process node
  – Leveraging IP in the form of chiplets
    – IP that is physically realized working on a standard communication interface (AIB, PCIe®, HBM, etc.)

The new modularized SoC (long-term vision)
Evolution of Multi-Chip(let) Packaging…

- Multi-Chip Module (MCM) 1970
- System in a Package (SIP) 1998
- RF Module 2005
- Silicon Interposers 2.5D IC 2008
- FOWLP 3DIC 2018
- Heterogeneous Integration Disaggregated SoC Future
The Next Packaging Paradigm Change is Here…

- **Mechanical Design Tools**
  - Leadframe

- **PCB-Like Design Flows**
  - BGA/LGA

- **Hybrid Design Flows**
  - 2.5D-IC/FOWLP/Embedded Bridges

- **IC-Like Design Flows**
  - 3D-IC
What Are We Announcing?

**Cadence® UltraLink™ D2D PHY IP**

- High-performance, low-latency PHY IP for die-to-die connectivity
  - **Fastest** NRZ D2D PHY – 40Gbps
  - Targets cloud **HPC and networking** applications – 1Tbps/mm beachfront bandwidth
  - Supports MCMs on organic substrate. **No silicon interposer required** – 130um bump pitch
  - 7nm process – The preferred node for the HPC market

- IP is proven in 7nm silicon

- Extends Cadence’s existing HPC IP portfolio
Chiplet Value Proposition

- Allow flexibility in choosing process node, core die and SerDes don’t need to be on the same process node
- Achieve better yield by reducing die size
- Shorten IC design cycle and simplify integration complexity by separating high-speed SerDes into chiplet
- Lower manufacturing cost by purchasing known good die
Die-to-Die Interconnect Tradeoffs

Can we avoid using high-cost packaging? (e.g. silicon interposer or InFO)

Is the system proprietary or we need an eco-system?

What are the most critical metrics?

Package Cost & Yield

Beachfront bandwidth

NRZ vs PAM4

Power

Latency

There’s NO one size fits all solution for D2D connectivity
Die-to-Die Interconnect Options

Parallel Interface
- Ex: AIB, HBM, HBI (2-4Gbps NRZ)
- Required by advanced packaging – silicon interposer or InFo
- Pros: Lowest power, low latency, must-have for HBM
- Cons: High wire count, high package cost, low yield, reliability issue

NRZ Serial Interface
- Ex: 20-30Gbps NRZ
- Pros: Support organic substrate, easy routing, low latency
- Cons: Higher power, design complexity

PAM4 Serial Interface
- 112G-PAM4
- Pros: Industry standard (CIE-OIF-XSR112G)
- Cons: Requires FEC for "error-free" links, higher latency, higher power

Fastest, higher bandwidth, low latency
Cadence® UltraLink™ D2D PHY IP
Example: 51.2 Tbps Switch

- Organic substrate (MCM)
- Each chiplet provides 6.4T bandwidth
- Use 8 chiplet to support 51.2T total bandwidth
- D2D interface between I/O chiplets and cores
- D2D interface between two cores
Example: AI/ML Accelerator

- 2.5D interposer for HBM
- 112G SerDes provides chip-to-chip connectivity
- D2D interface between I/O chiplets and the core
Under the Hood: UltraLink™ D2D PHY IP
High-bandwidth, low-power, low-latency die-to-die interconnect

- Flexible line rate of 20-40Gbps NRZ
- ~500Gbps bidirectional bandwidth in 1mm of beachfront (1Tbps/mm aggregate)
- Support 8dB insertion loss (20+mm trace)
- Low power and ultra-low latency
- Forwarded clock
- Raw BER of 1e-15, no FEC
- Sideband for link management
- Targets 130u bump pitch for MCM applications
- Also supports micro bump for silicon interposer
- Integrated Spacial encoding and lane-to-lane de-skew logic
Cadence® UltraLink™ D2D PHY IP Test Board
UltraLink™ D2D PHY IP TX: 40Gb/s
Bump Diagram Example
240 Gbps Full Duplex (480Gb Aggregate) Bandwidth in 0.5 mm of die edge

- TX Group
  - 7 TX, 2 Clk, 2 Sideband,
- RX Group
  - 7 RX, 2 Clk, 2 Sideband,
- Group. [X: 260u, Y: 1300u]

- 1Tx and 1 RX groups shown above
  - Line Rate 20-40Gbps
  - Effective number of Lanes after coding overhead – 6 TX, 6 RX
  - Bandwidth 240G RX + 240G TX Total Power for configuration 360mW @ 40G, 180mW @ 20G
  - Die Edge ➔ 0.5 mm, Die Area ➔ 0.68 mm²
UltraLink 40G RX On Die Eye Plot

Long Channel

Short Channel