Cadence

Rishi Chugh , Product Marketing , IPG
12/18/2019

Cadence Design Systems, Inc

Founded in 1988
by the merger of SDA Systems, Inc. and ECAD, Inc.

Lip-Bu Tan, CEO

S&P 500
Nasdaq 100

Revenue
$2.3B*
• Estimated 2019 revenue actual revenue may differ

Employees
~8,000

Countries
20

Software and Programming
Industry

Exceed customer expectations	Explore what's possible
Execute with quality	Elevate the team

Culture

Source: Cadence Earnings Press Release, Q4 2019
https://www.cadence.com/en_US/home/company/newsroom/press-releases/pr-ir/2019/cadence-reports-third-quarter-2019-financial-results.html

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Cadence at a Glance

4,500+
R&D ENGINEERS

1750+
FIELD ENGINEERS

R&D INVESTMENT
$884M

PATENTS WORLDWIDE
1600+

26 GLOBAL DEVELOPMENT CENTERS

All data as of end of Q4 2018

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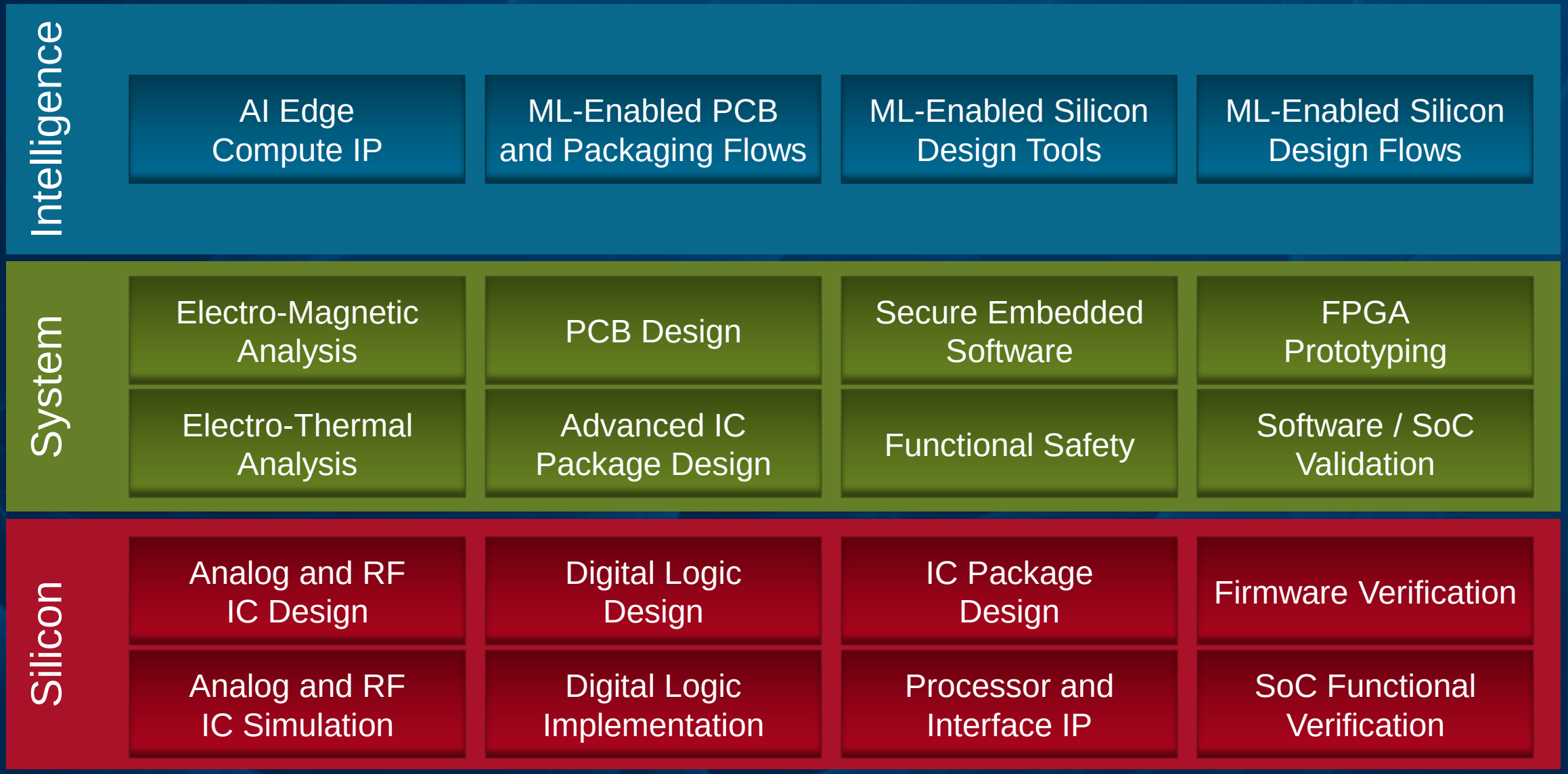
Cadence Solution Offerings



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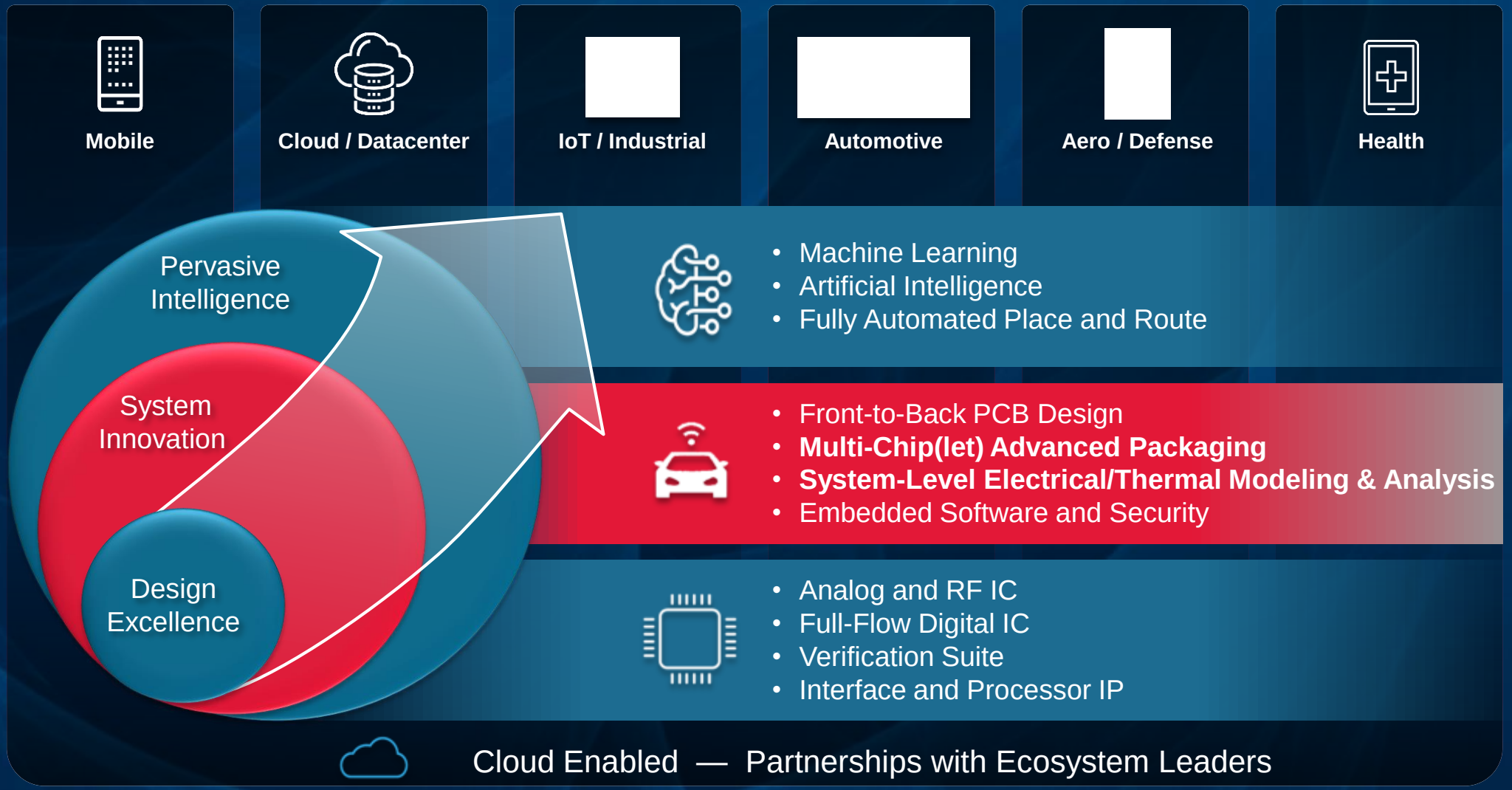
Cadence *Intelligent System Design Strategy*…
Thinking Outside The Chip



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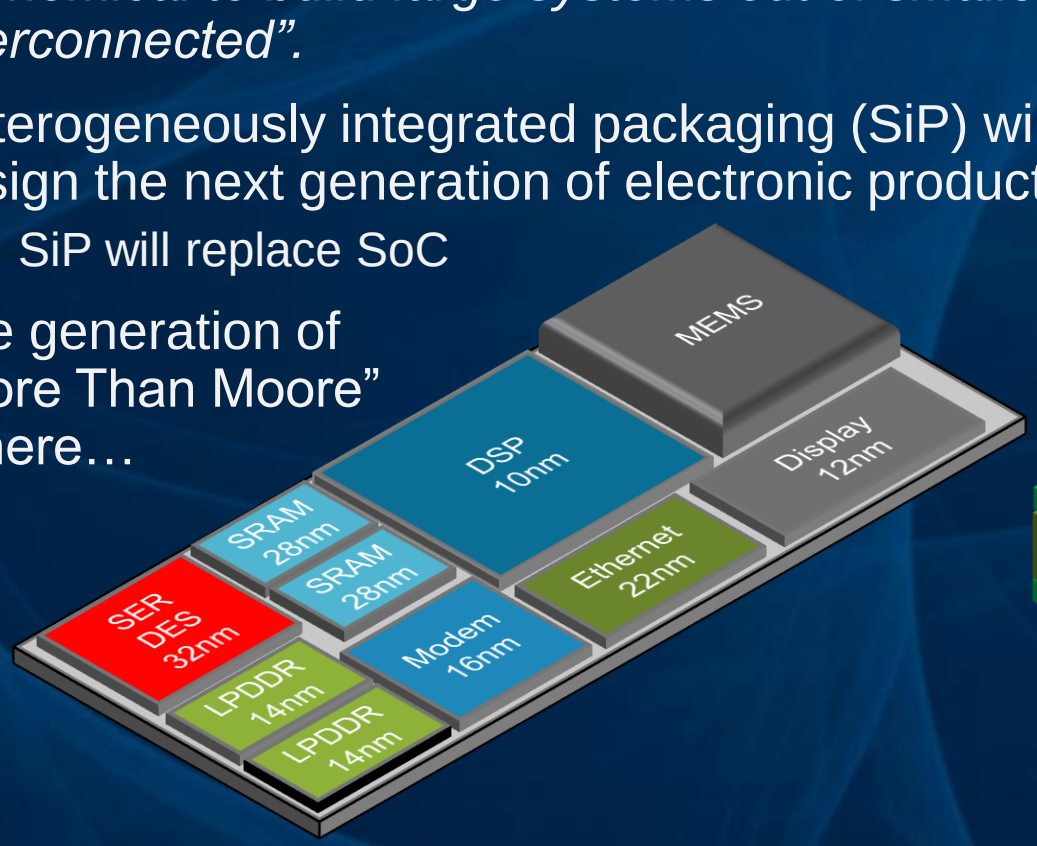
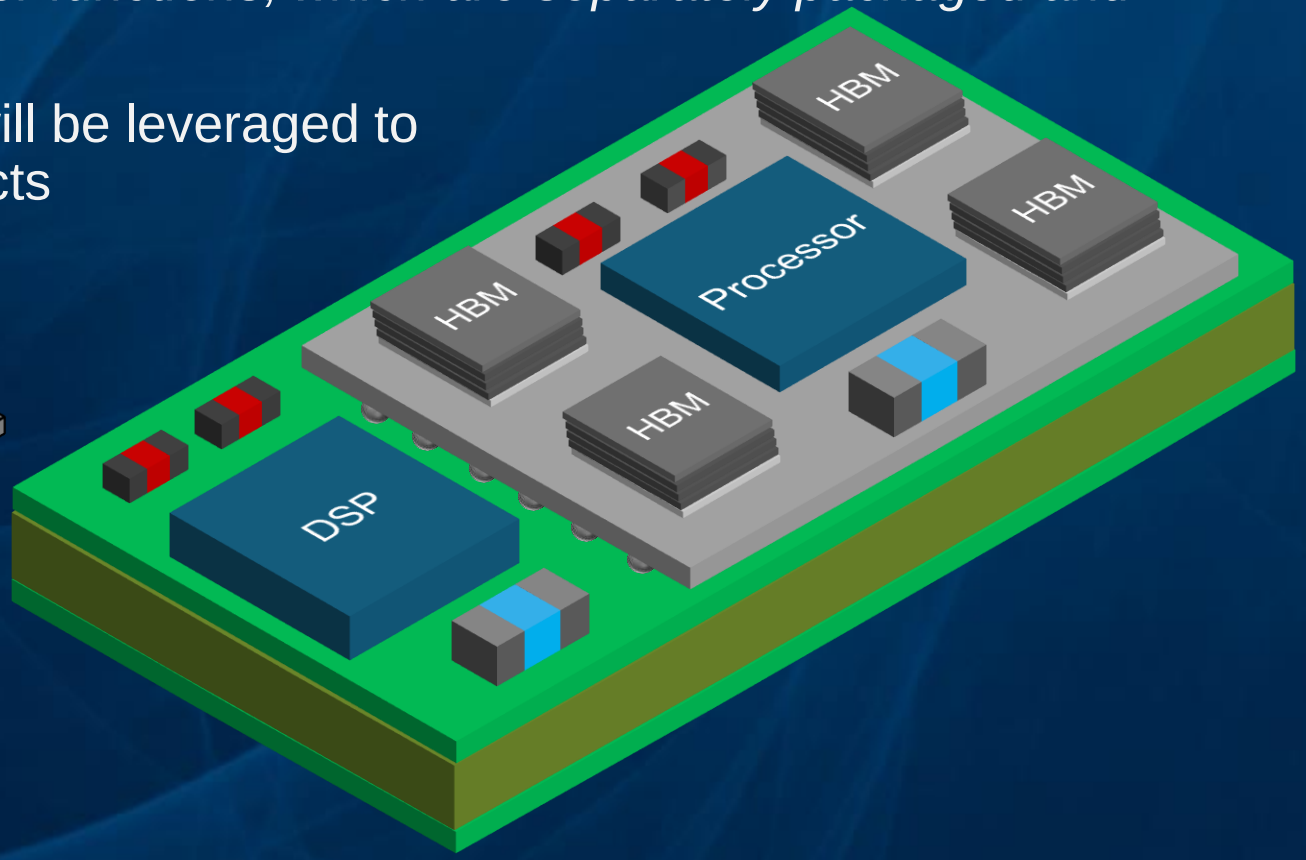
The Beginning of the “More Than Moore” Era

- For the past five decades, the electronic industry has thrived while enjoying the benefits of Moore’s Law. But things are changing…The economics of semiconductor logic scaling are gone
- Gordon Moore knew this day would come. He also predicted that *”It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected”.*
- Heterogeneously integrated packaging (SiP) will be leveraged to design the next generation of electronic products
  - SiP will replace SoC
- The generation of “More Than Moore” is here…





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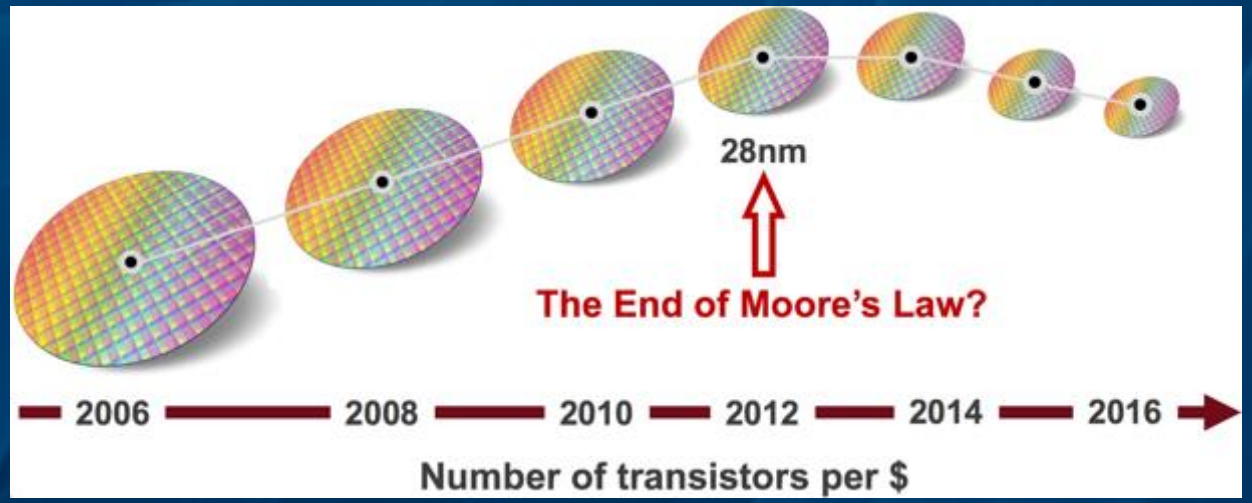
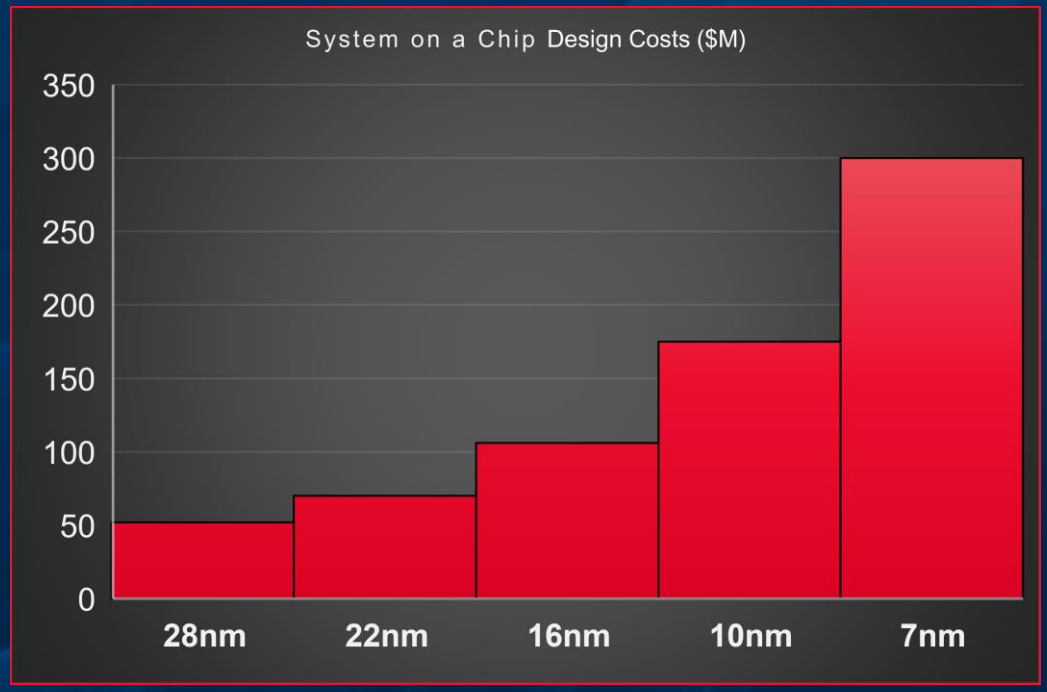
Is Moore's Law Already Dead?

- It's more than the limitations of physics…
- Cost per transistor has steadily increased since 2012/3 (28nm)
- Designing chips at the latest nodes is hard and expensive
  - Low-volume businesses can't justify the NRE costs of designing an SoC at the latest node
  - Requires huge teams of engineering specialists that aren't always easy to find
  - Systems and software companies now designing chips and challenging the status quo of SoC approach
- Todays SoC's are reaching reticle limits…but big chips don't yield anyways
- More Analog/RF content in today's designs.
  - Analog/RF never have benefited from Moore's Law





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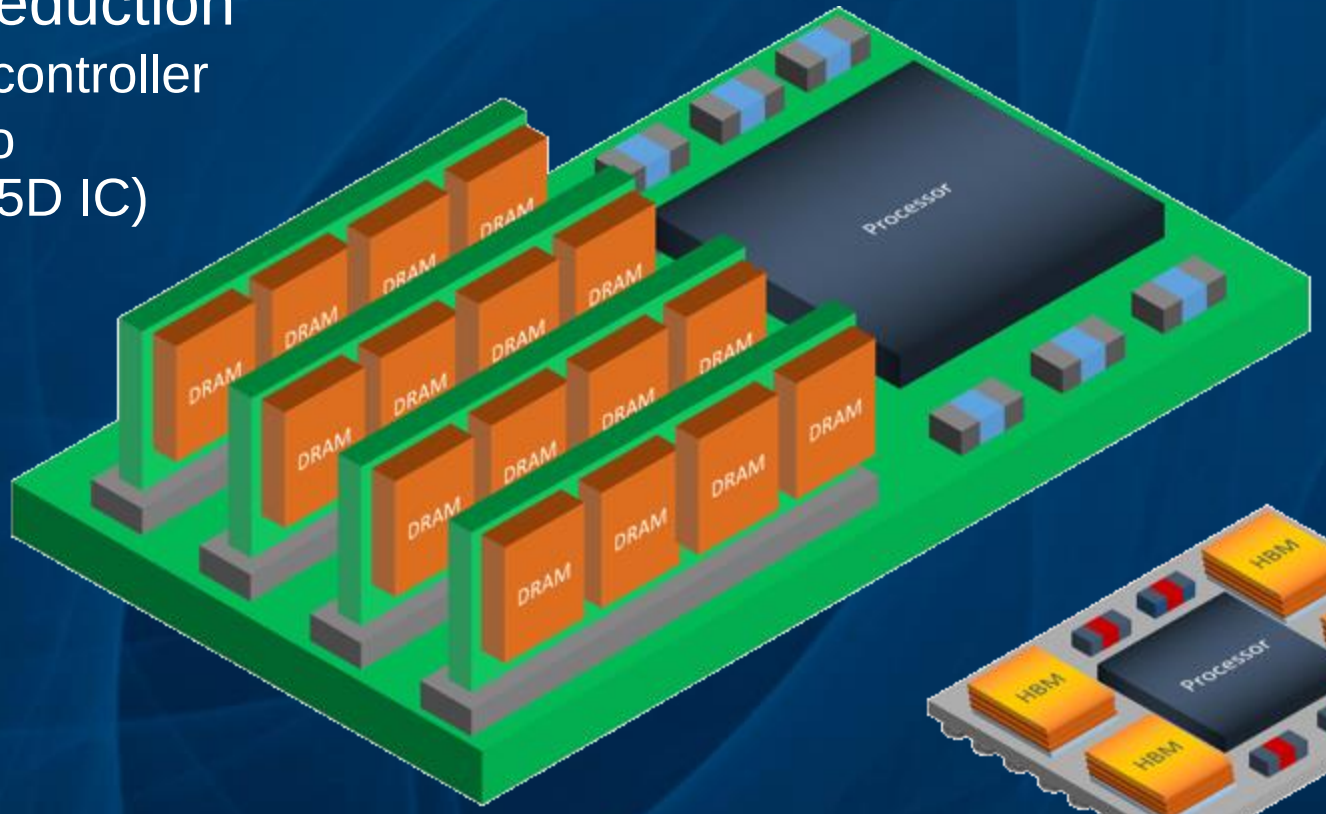
More Than Moore Example…

- Processor to memory latency reduction
  - Stack thinned memory chips with controller
  - Place memory stacks very close to processor on silicon interposer (2.5D IC)
  - Dramatic reduction in size
  - Simplifies board-level design
  - Drastic reduction in latency
  - Reduction in power
  - Thermal needs proper consideration



Board-level implementation

Package-level implementation

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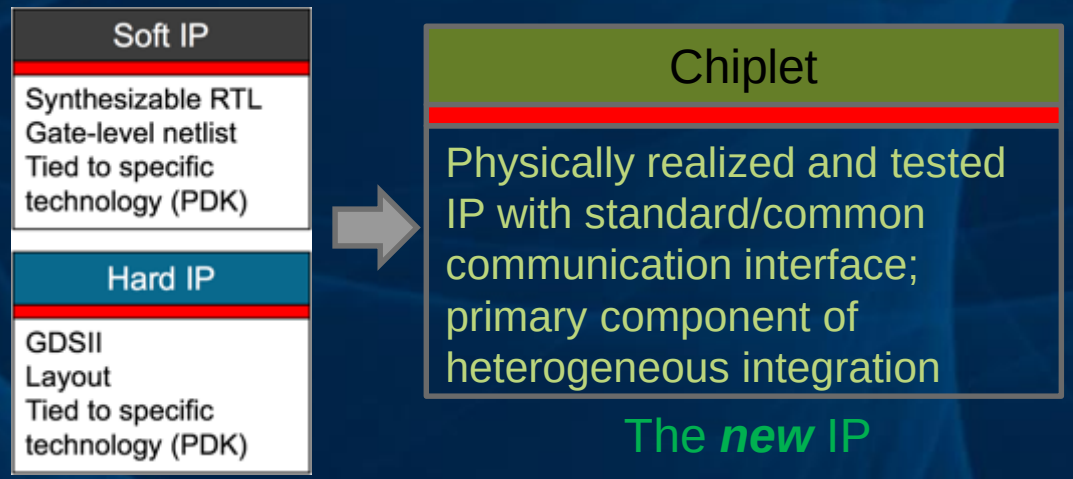
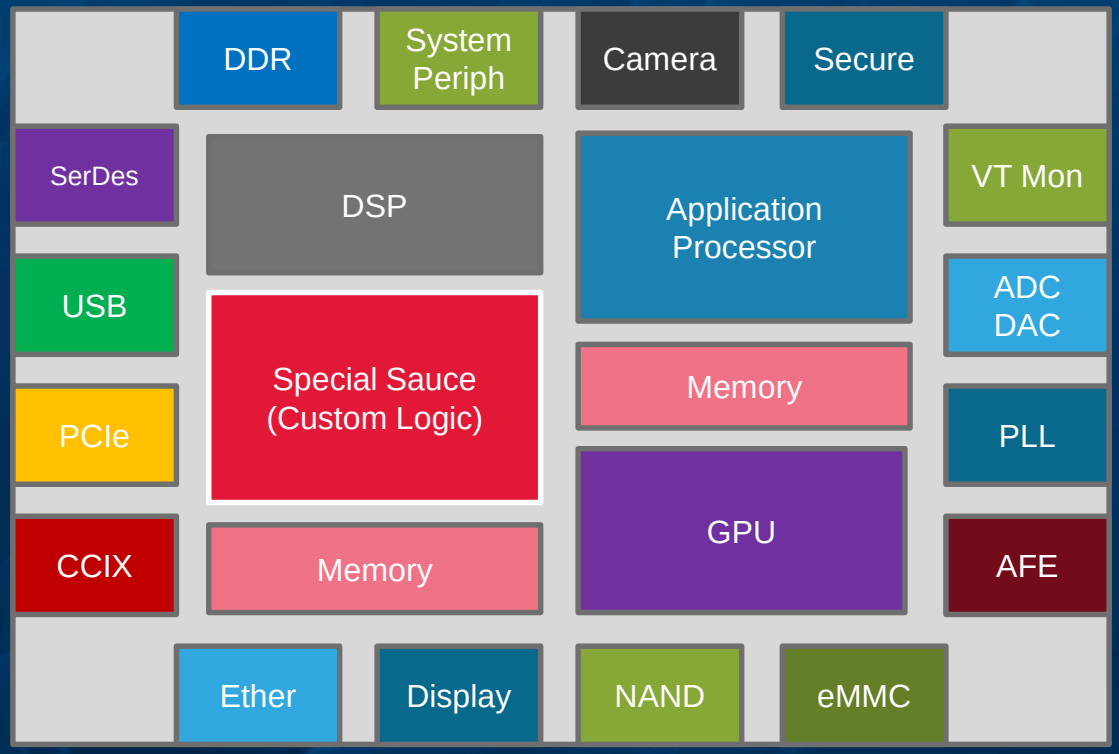
Transitioning to “More than Moore”…Heterogeneous Integration

- SiP becomes the new SoC?
  - Modular approach vs monolithic approach
    - Not everything needs to be designed in the same process node
  - Leveraging IP in the form of chiplets
    - IP that is physically realized working on a standard communication interface (AIB, PCIe®, HBM, etc.)



The ***new*** IP



The ***new*** modularized SoC (long-term vision)

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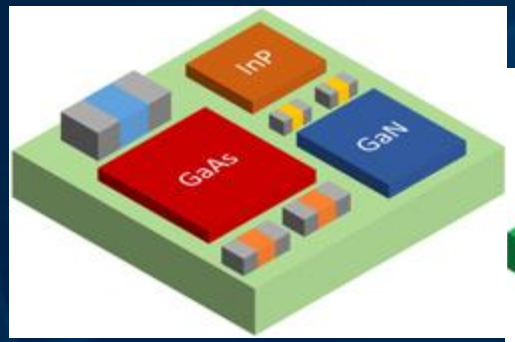
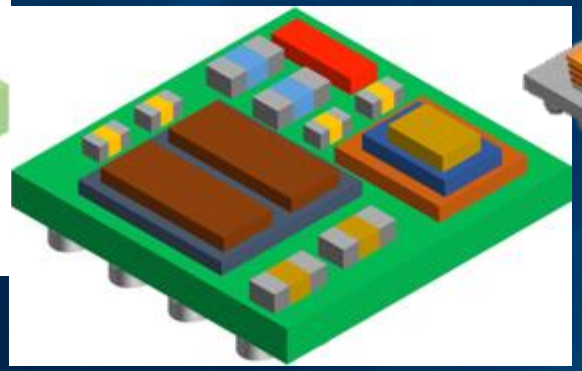
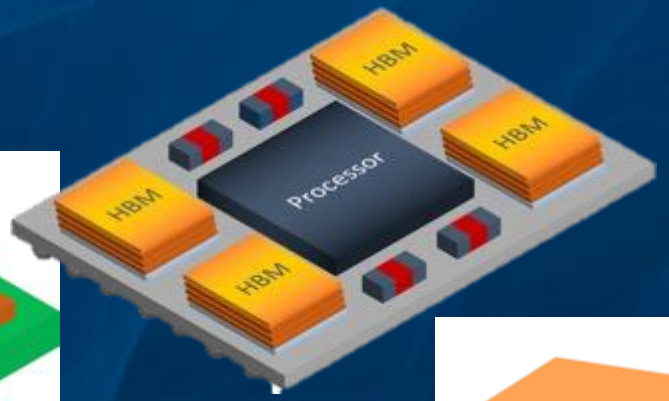
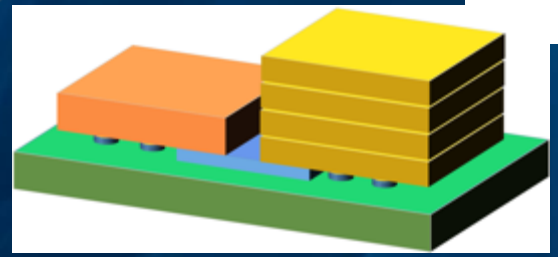
Evolution of Multi-Chip(let) Packaging…









Multi-Chip Module (MCM) — 1970

System in a Package (SiP) — 1998

RF Module — 2005

Silicon Interposers 2.5D IC — 2008

FOWLP 3DIC — 2018

Heterogeneous Integration Disaggregated SoC — Future

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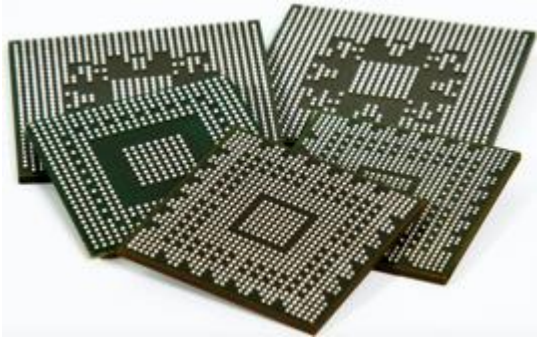
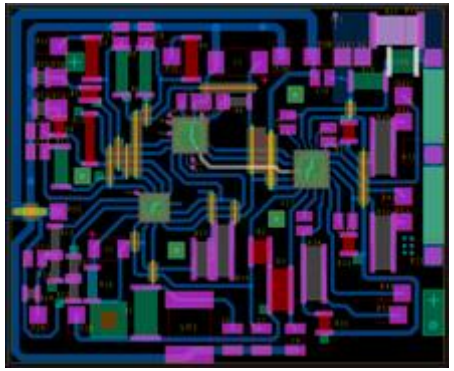
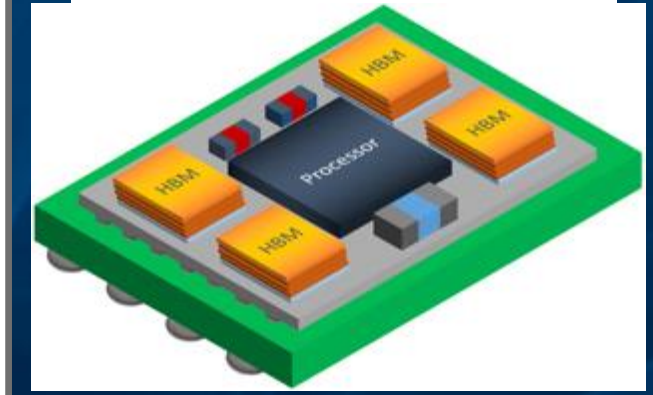
The Next Packaging Paradigm Change is Here…

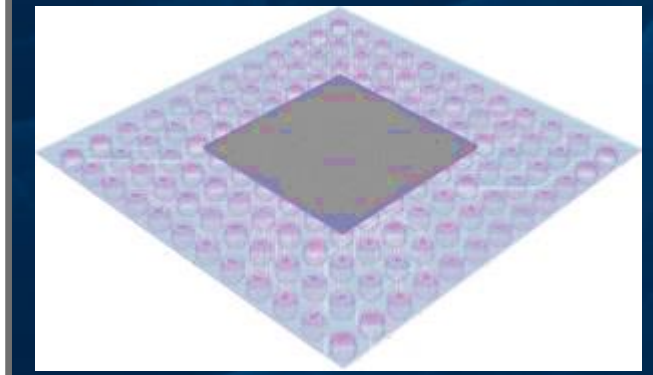
Mechanical Design Tools | PCB-Like Design Flows | Hybrid Design Flows | IC-Like Design Flows

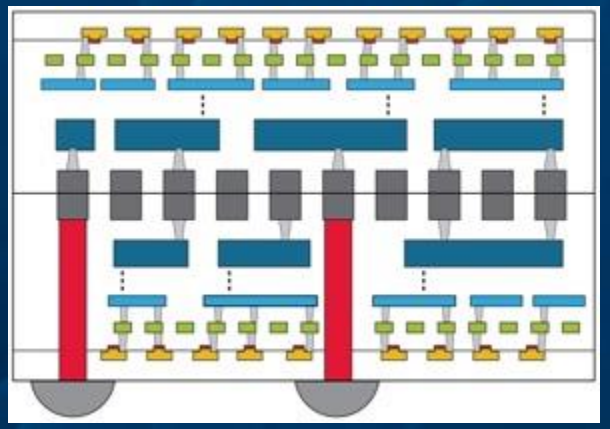
Leadframe	BGA/LGA	2.5D-IC/FOWLP/ Embedded Bridges	3D-IC

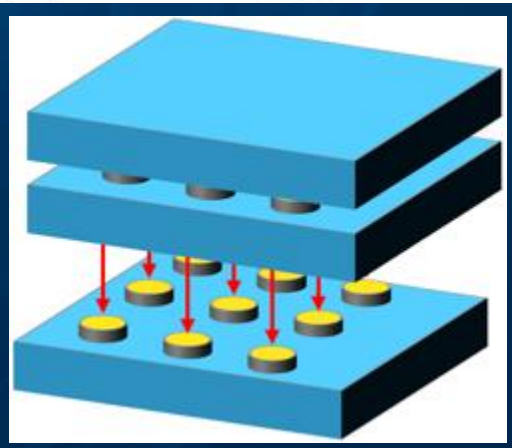












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What Are We Announcing ?

Cadence® UltraLink™ D2D PHY IP

- High-performance, low-latency PHY IP for die-to-die connectivity
  - **Fastest** NRZ D2D PHY – 40Gbps
  - Targets cloud **HPC and networking** applications – 1Tbps/mm beachfront bandwidth
  - Supports MCMs on organic substrate. **No silicon interposer required** – 130um bump pitch
  - 7nm process – The preferred node for the HPC market
- IP is proven in 7nm silicon
- Extends Cadence's existing HPC IP portfolio

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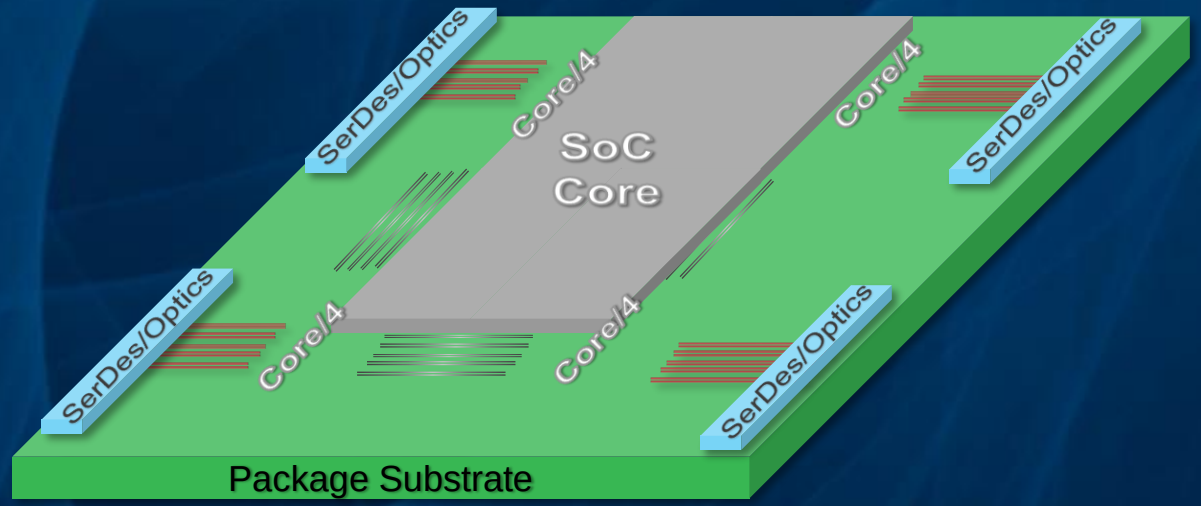
Chiplet Value Proposition

- Allow flexibility in choosing process node, core die and SerDes don’t need to be on the same process node
- Achieve better yield by reducing die size
- Shorten IC design cycle and simplify integration complexity by separating high-speed SerDes into chiplet
- Lower manufacturing cost by purchasing known good die



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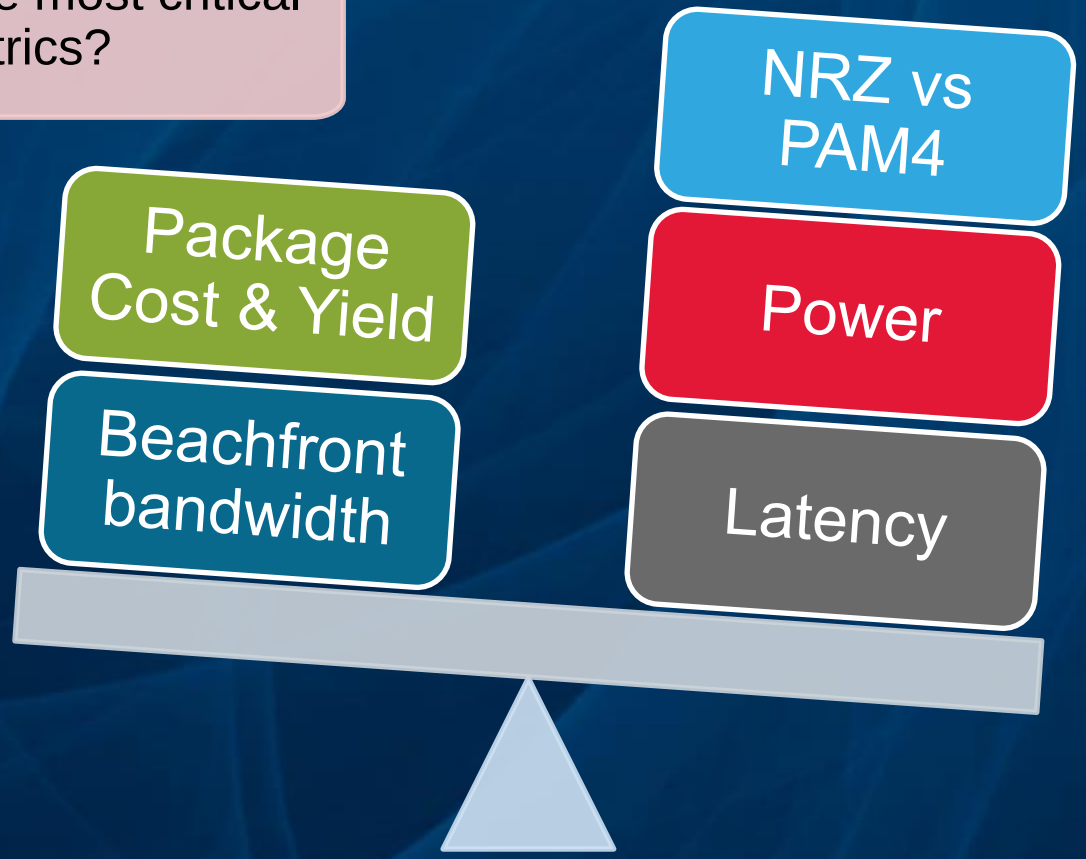
Die-to-Die Interconnect Tradeoffs

What are the most critical metrics?

Can we avoid using high-cost packaging? (e.g.silicon interposer or InFO)

Is the system proprietary or we need an eco-system?



There’s NO one size fits all solution for D2D connectivity

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Die-to-Die Interconnect Options

Parallel Interface

- Ex: AIB, HBM, HBI (2-4Gbps NRZ)
- Required by advanced packaging – silicon interposer or InFo
- Pros: Lowest power, low latency, must-have for HBM
- Cons: High wire count, high package cost, low yield, reliability issue

NRZ Serial Interface

- Ex: 20-30Gbps NRZ
- Pros: Support organic substrate, easy routing, low latency
- Cons: Higher power, design complexity

PAM4 Serial Interface

- 112G-PAM4
- Pros: Industry standard (CIE-OIF-XSR112G)
- Cons: Requires FEC for "error-free" links, higher latency, higher power

Fastest, higher bandwidth, low latency

Cadence® UltraLink™ D2D PHY IP

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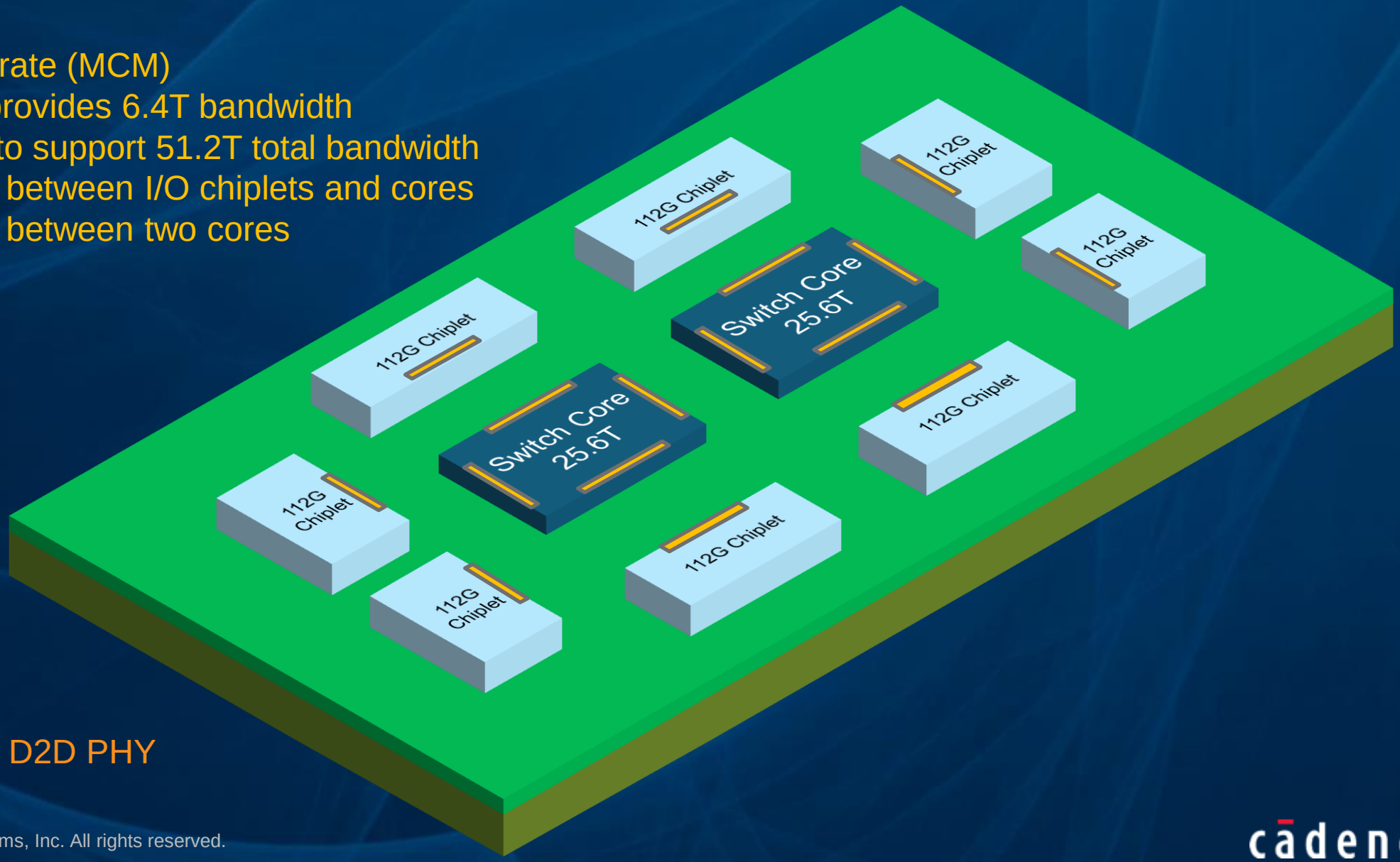
Example: 51.2 Tbps Switch

- Organic substrate (MCM)
- Each chiplet provides 6.4T bandwidth
- Use 8 chiplet to support 51.2T total bandwidth
- D2D interface between I/O chiplets and cores
- D2D interface between two cores



UltraLink D2D PHY

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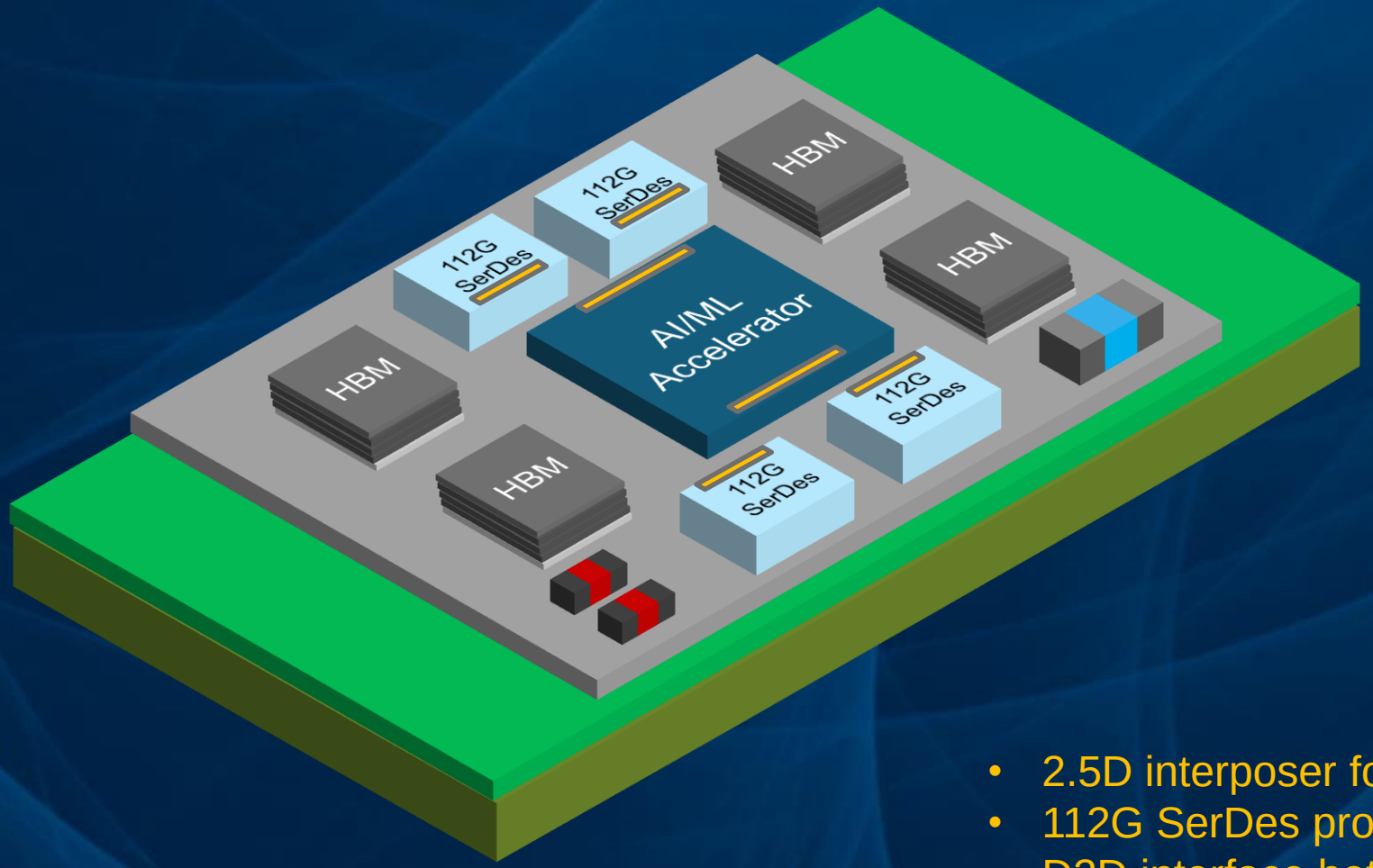
Example: AI/ML Accelerator



UltraLink D2D PHY

- 2.5D interposer for HBM
- 112G SerDes provides chip-to-chip connectivity
- D2D interface between I/O chip-lets and the core

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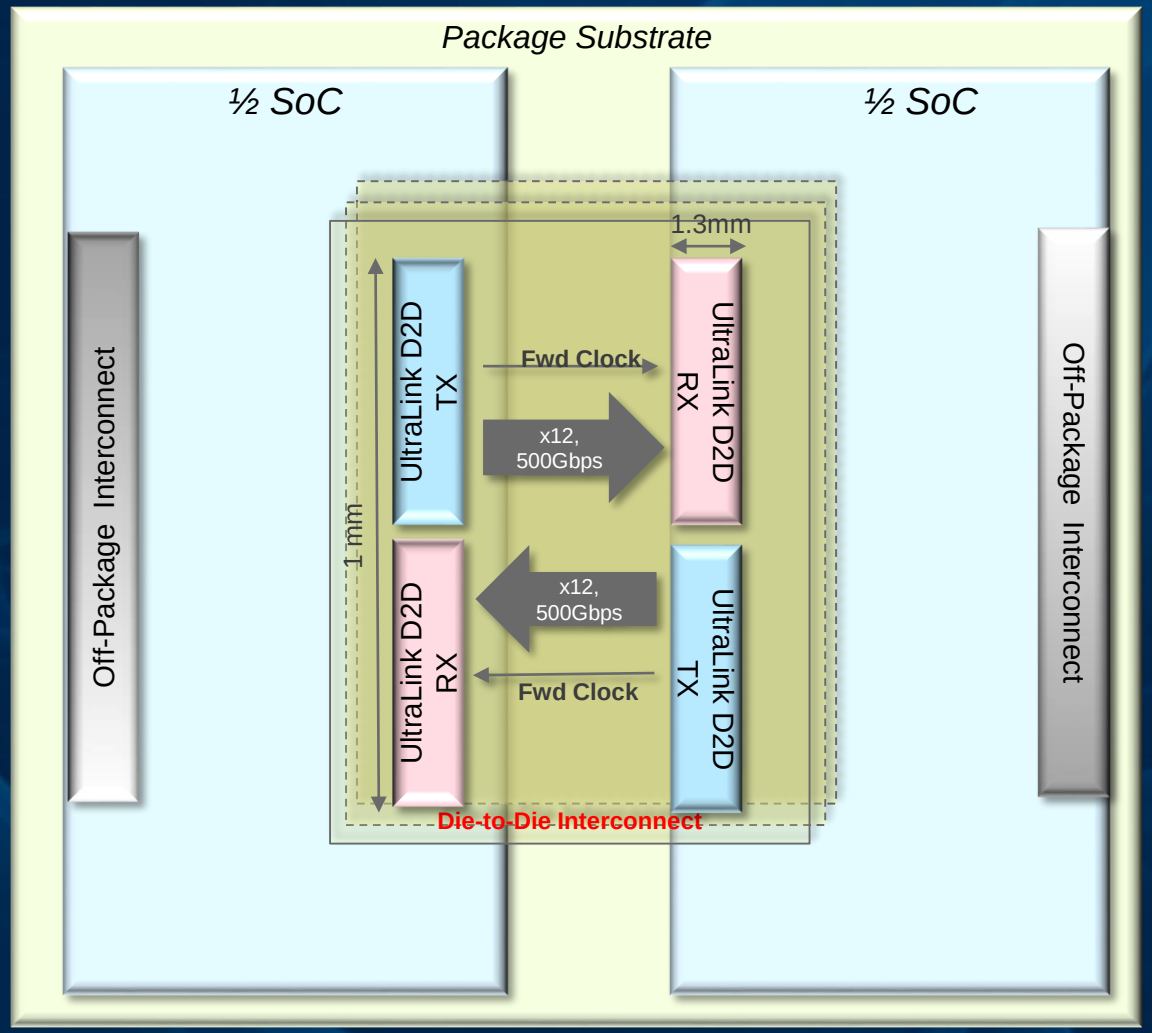
Under the Hood: UltraLink™ D2D PHY IP

High-bandwidth, low-power, low-latency die-to-die interconnect



- Flexible line rate of 20-40Gbps NRZ
- ~500Gbps bidirectional bandwidth in 1mm of beachfront (1Tbps/mm aggregate)
- Support 8dB insertion loss (20+mm trace)
- Low power and ultra-low latency
- Forwarded clock
- Raw BER of 1e-15, no FEC
- Sideband for link management
- Targets 130u bump pitch for MCM applications
- Also supports micro bump for silicon interposer
- Integrated Spacial encoding and lane-to-lane de-skew logic

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Cadence® UltraLink™ D2D PHY IP Test Board

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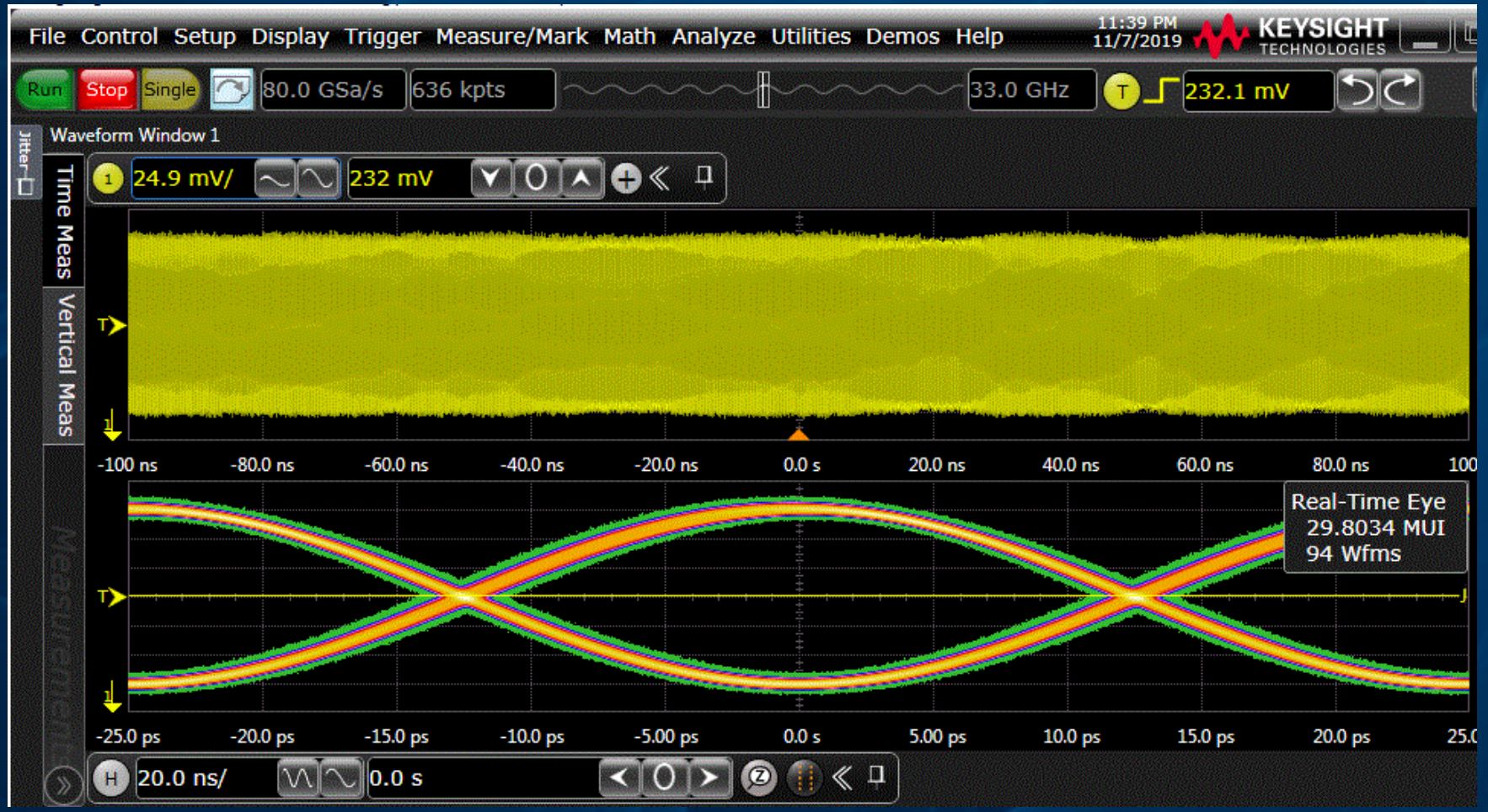
UltraLink™ D2D PHY IP TX: 40Gb/s



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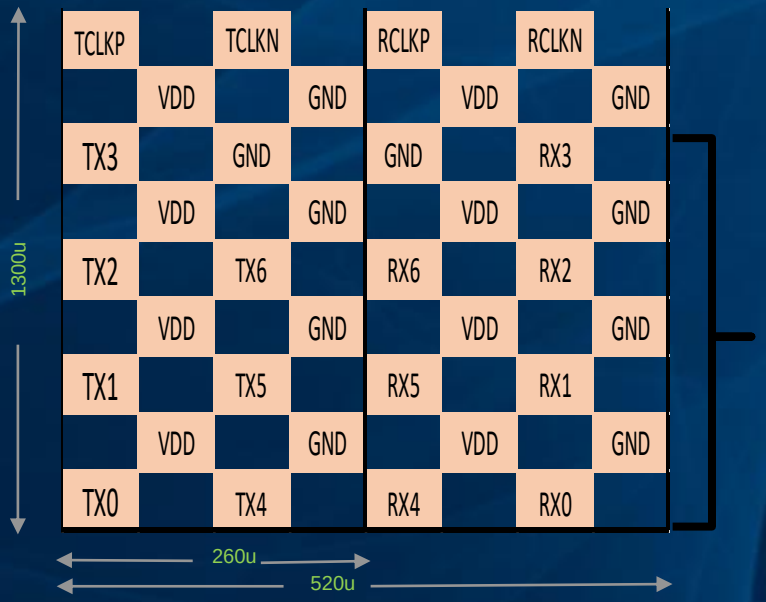
Bump Diagram Example

240 Gbps Full Duplex (480Gb Aggregate) Bandwidth in 0.5 mm of die edge



High Speed Signals in 1st 4 rows

- TX Group
  7 TX, 2 Clk, 2 Sideband,
- RX Group
  7 RX, 2 Clk, 2 Sideband,
- Group. [X: 260u, Y: 1300u]

- 1Tx and 1 RX groups shown above
  - Line Rate 20-40Gbps
  - Effective number of Lanes after coding overhead – 6 TX, 6 RX
  - Bandwidth 240G RX + 240G TX Total Power for configuration 360mW @ 40G, 180mW @ 20G
  - Die Edge ➔ 0.5 mm , Die Area ➔ 0.68 mm^2

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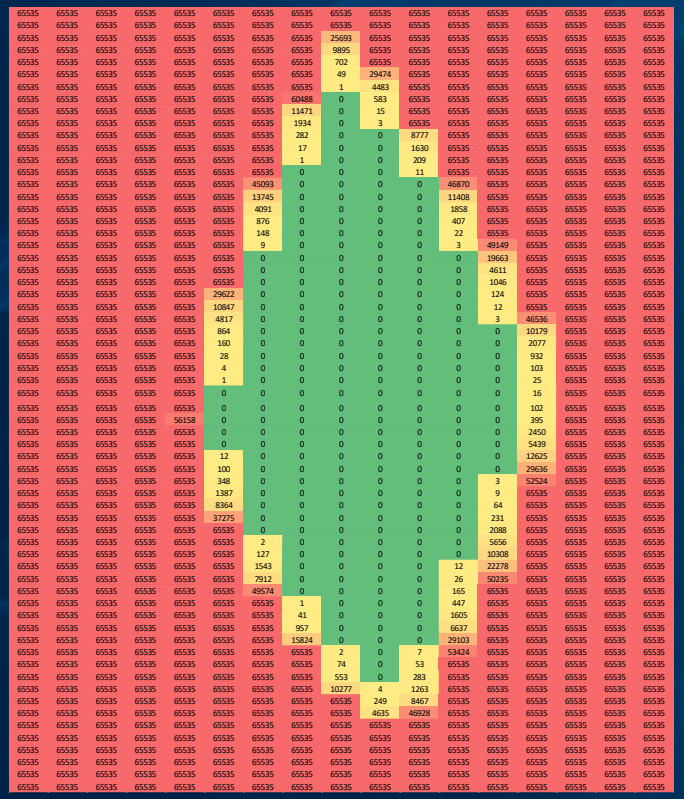
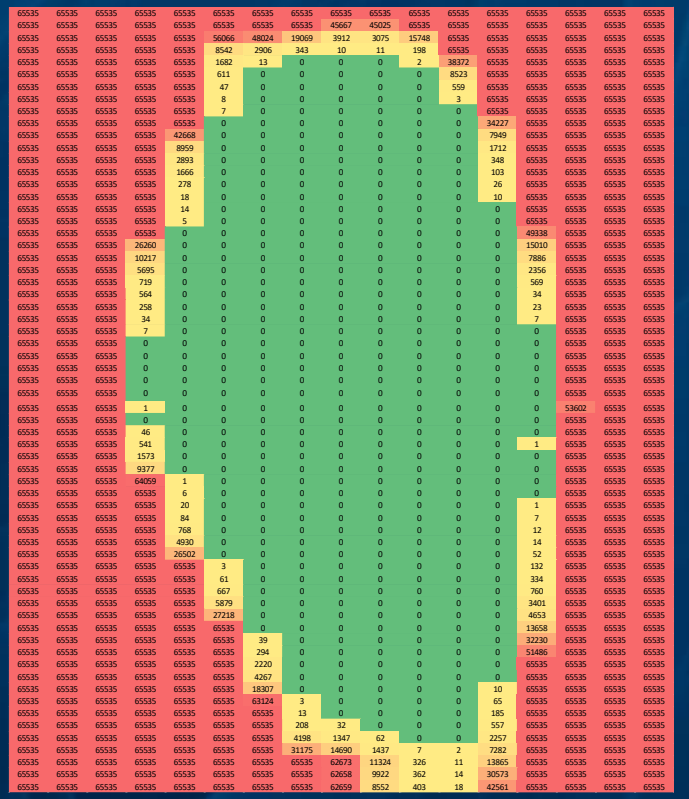
UltraLink 40G RX On Die Eye Plot

Long Channel



Short Channel



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