OCP – ODSA Project

Commercialization Use Case

BoW D2D Interface for Multi-Chiplet AI System

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d-Matrix Participation

- d-Matrix has been actively participating in ODSA since year 2020
- Using ODSA Bunch of Wires (BoW), d-Matrix designs die-to-die (D2D) interface for parallel multi-chiplet communication

- BoW design specifications
- Example link channels
- Shared channel simulation

- Design experience
- Implementation feasibility
- Support interoperability
d-Matrix Company Profile

- **Past background**
  - 20+ years of silicon and systems leadership
  - Delivered > 100M chips in the cloud and enterprise
  - Products generated > $1B in revenue

- **Current team**
  - 55 persons, 30% PhDs
  - Silicon Valley / Sydney / Bengaluru

- **Investors:** $44M raised from top tier financial and strategic VCs

More information at https://www.d-matrix.ai
d-Matrix AI Compute Products

- From single AI neural core, d-Matrix designs AI engine and integrates multiple AI engines into chiplet
- Fabric of chiplets delivers modularity and scalability for different applications
- Proof-of-concept Nighthawk AI platform silicon (top-right) announced in 2021
- Next generation Corsair chiplet (bottom-right) incorporates BoW D2D interface to scale the modular chiplet into more powerful Corsair multi-chiplet AI system
d-Matrix Corsair Multi-Chiplet AI System

- 8-chiplet Corsair AI system on a common substrate
- All chiplets are connected through bi-directional 3×512Gbps BoW D2D interface
- Reason for using BoW
  - Low power (pJ/bit), high beachfront BW and support cost-efficient organic substrate
  - Interoperability enables heterogenous integration with chiplets from different parties
d-Matrix BoW D2D Interface

- **Process node:** TSMC 6nm technology
- **Electrical:** One pair of differential clock (forwarded clock), 16-bit single-ended (16Gbps/wire) data bus with AUX and FEC
- **Physical:** estimated area of 0.8mm²
- **Energy efficiency:** < 0.5pJ/bit
- **Beachfront bandwidth:** 0.19Tbps/mm (single-stack design), up to 0.75Tbps/mm (4-stack design)
- **BER:** < 1e-15
- **Deployment timeline:** Q4 2022 (silicon TC)
d-Matrix Roadmap

- Contribute to the future development of multi-chiplet interface
  - Higher beachfront bandwidth > 1Tbps/mm
  - Improved energy efficiency < 0.25pJ/bit
  - Link layer compliance and interoperability
  - Implementation using advanced packaging
Questions