~~Chiplet Architecture for Large Scale System Design~~
Design Space for Chiplet IO

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Agenda

- Chiplet IO types and comparisons
- Cadence UltraLink w/ Spatial Encoding
- Measurement Results
- UCIe at a Glance
- Summary

Chiplet IO Types

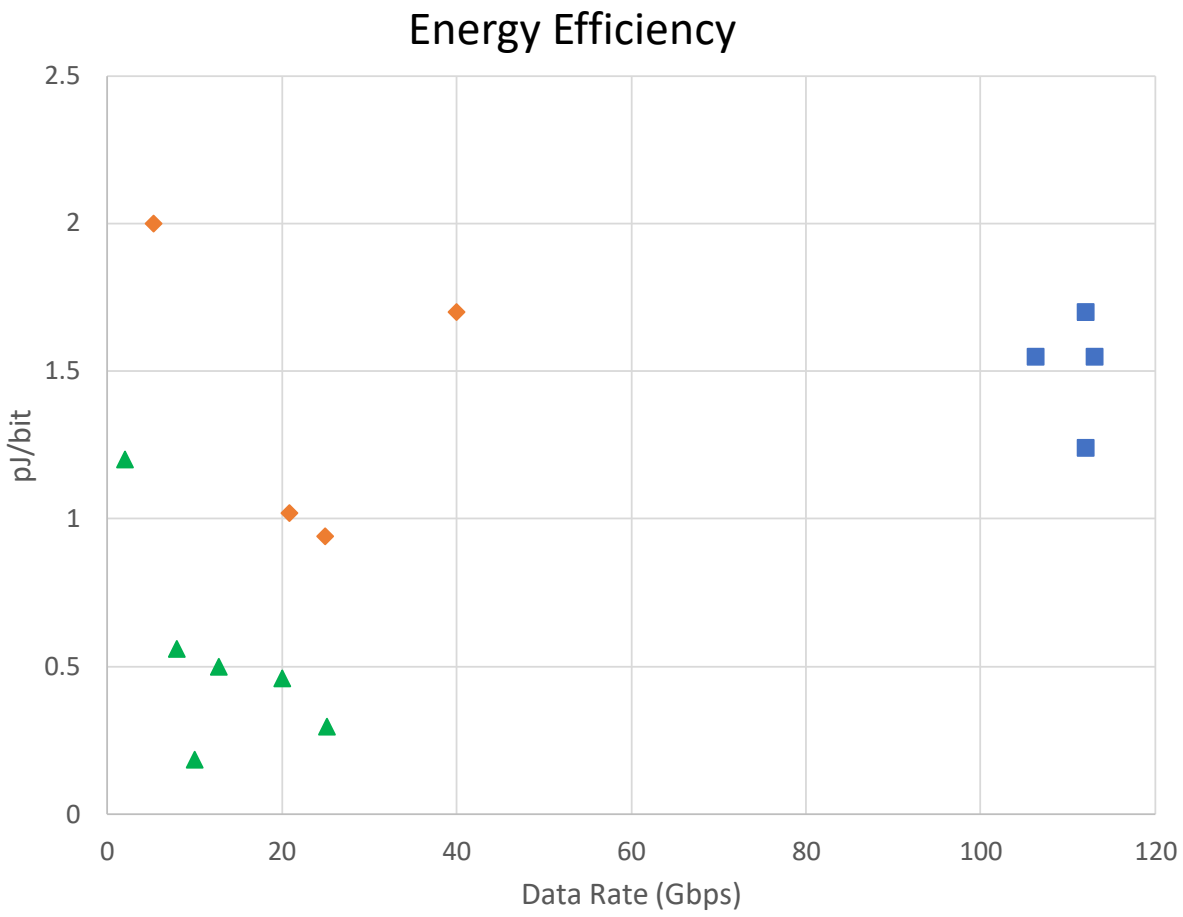
Serial PAM4 Differential	Parallel Advanced Package	Parallel Standard Package
E.g. USR, XSR (112 G - PAM4)	E.g. AIB, HBM, HBI, UCIe (2 - 16 Gbps NRZ)	E.g. BoW, UCIe (16 – 32 Gbps NRZ)
Pro • Industry standard (CIE-OIF-XSR112G) • High throughput	**Pro** • Low power • Low latency • High shoreline density • Low area overhead	**Pro** • Organic substrate • High accessibility • Easy routing
Con • Require FEC for “error-free” links • High latency • High power	**Con** • High package cost • Limited access • Low yield	**Con** • Medium power • Low shoreline density

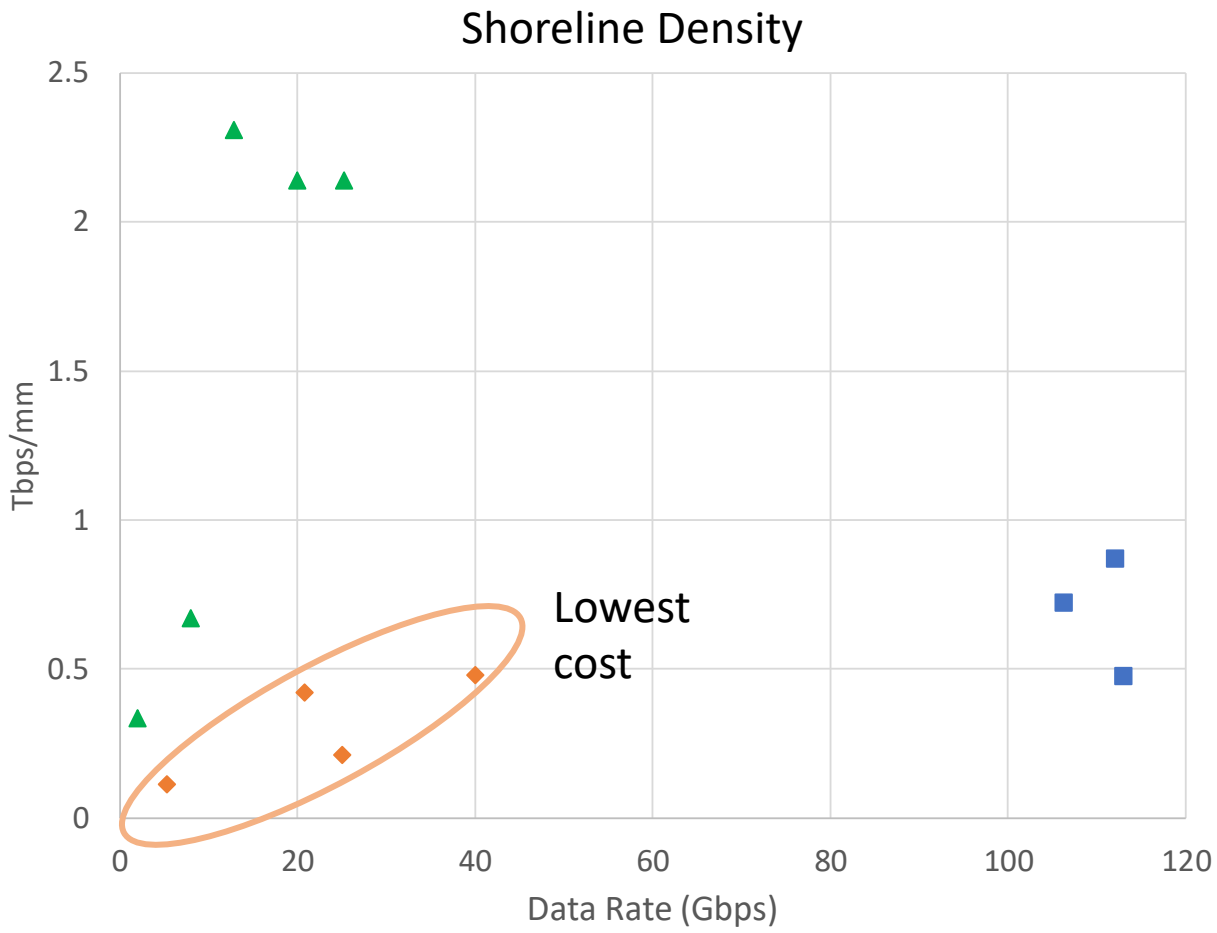
Chiplet IO Comparisons

	Serial—PAM4 Differential	Parallel—Advanced Package	Parallel—Standard Package
Signaling	PAM4, differential	NRZ, single-ended	NRZ, single-ended
Package type	Standard / organic	Interposer / EMIB / InFO	Standard / organic
Data rate	112G, 56G, 28G, etc	2G, 4G, 8G, 16G, 32G, etc	2G, 4G, 8G, 16G, 32G, 40G, etc
Reach	20-80mm [1] [2]	< 5mm	< 20mm
Energy efficiency	~1-2 pJ/bit [1]	<0.5pJ / bit	0.5-2pJ/bit
Shoreline density	~870 Gbps/mm [1]	>2 Tbps/mm @ 16Gbps/lane	240 Gbps/mm [3]
BW / area	750 Gbps/mm^2 [1]	>2 Tbps/mm^2 @ 16Gbps/lane	363 Gbps/mm^2 [3]
BER	1e-9[1]	<1e-27 for <=16Gb/s <1e-15 for > 16Gb/s	< 1e-15 for 40Gbps [3]
FEC	Yes	No	No
Latency	High	Low	Low
Standard	IEEE, OIF	Mixed	Mixed

[1] Poon, VLSI2021, [2] Gangasani, ISSCC 2022, [3] McCollough, ISSCC 2021

pJ/bit, BW/mm from IEEE publications





Serial - PAM4 differential Parallel - standard package Parallel - advanced package

Data from ISSCC, VLSI between 2016-2022, all industry papers

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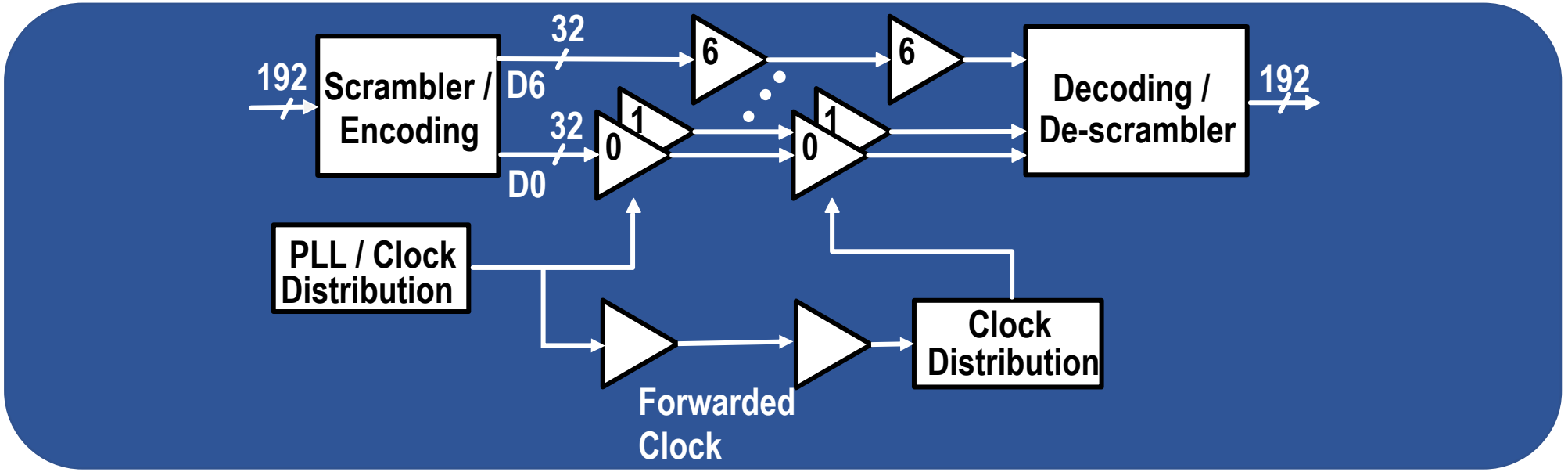
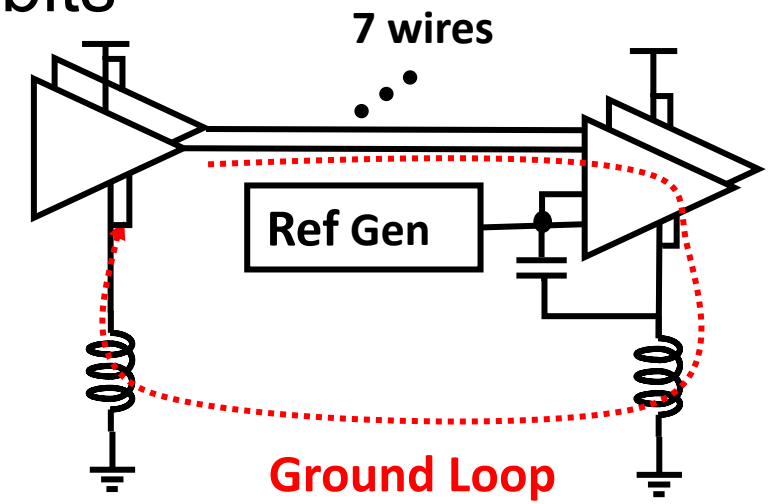
Cadence UltraLink – Spatial Coded D2D Links



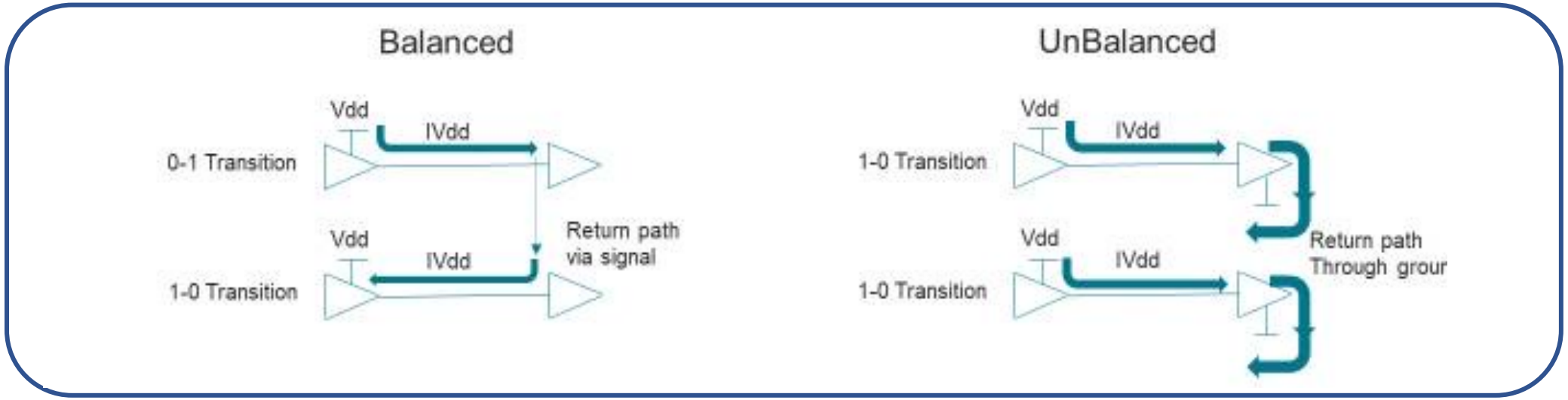
- Standard package, commercially deployed for 5nm and 7nm
- 40Gbps/lane, 1.7/1.5pJ/b for 7/5nm, ~ 8dB channel loss, 80mm
- Scrambling used to minimize long run lengths
- 6/7 encoding used to minimize dynamic power
- Matched forwarded clock used to minimize PLL and clock distribution jitter (Clock and data jitter correlated at RX)

Spatial Encoding

- Performance in single-ended systems is degraded due to ground loops
- Spatial encoding achieves an approximately balanced set of 1's/0's transmitted
- Using a 6/7 code 6 bits are encoded into 7 bits
  - Restriction that 3 or 4 bits are 1
  - Provides $\binom{7}{3}$ + $\binom{7}{4}$ =70 available codes
  - 64 codes for data with 6 additional for control
  - Reduced peak dynamic energy by ~15dB

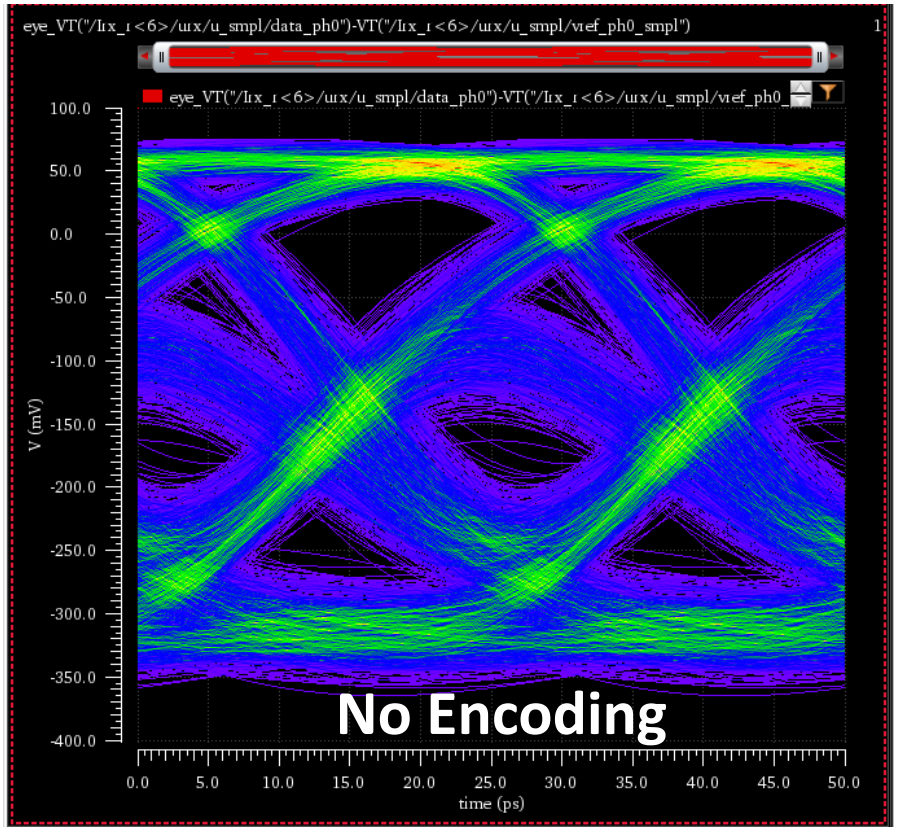


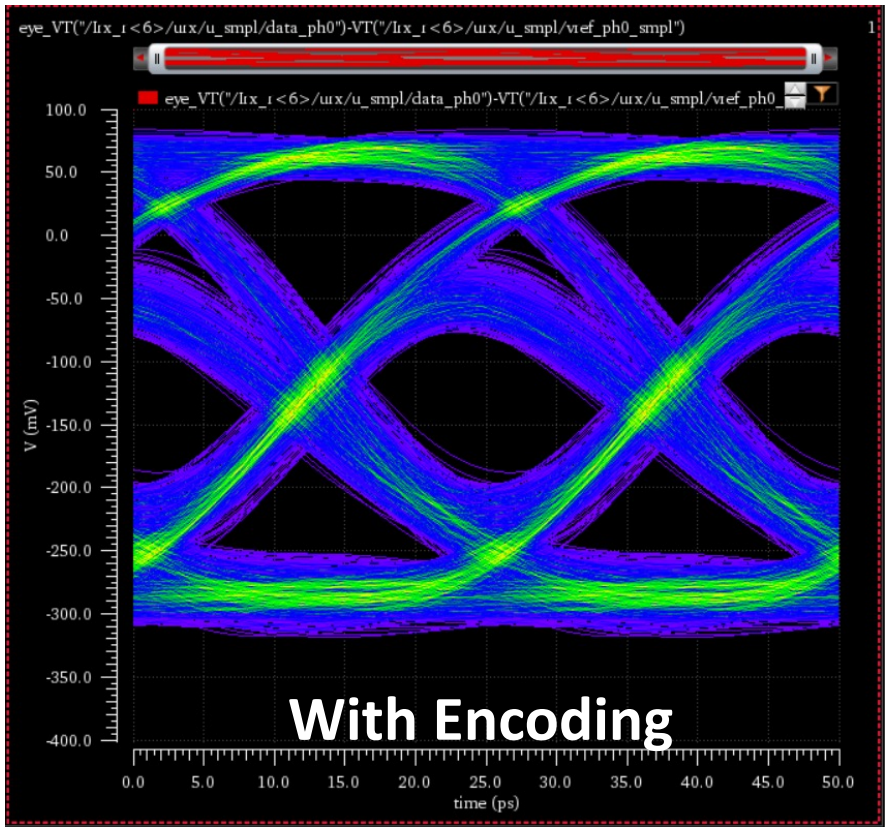
Spatial Encoding



- With spatial encoding there are 3 pairs of outputs that have a 0-1 and a 1-0 transition on all bit boundaries
- For these pairs they look like a differential signal and the return current does not travel through the VDD/GND return
- One of the seven output return currents remains unbalanced

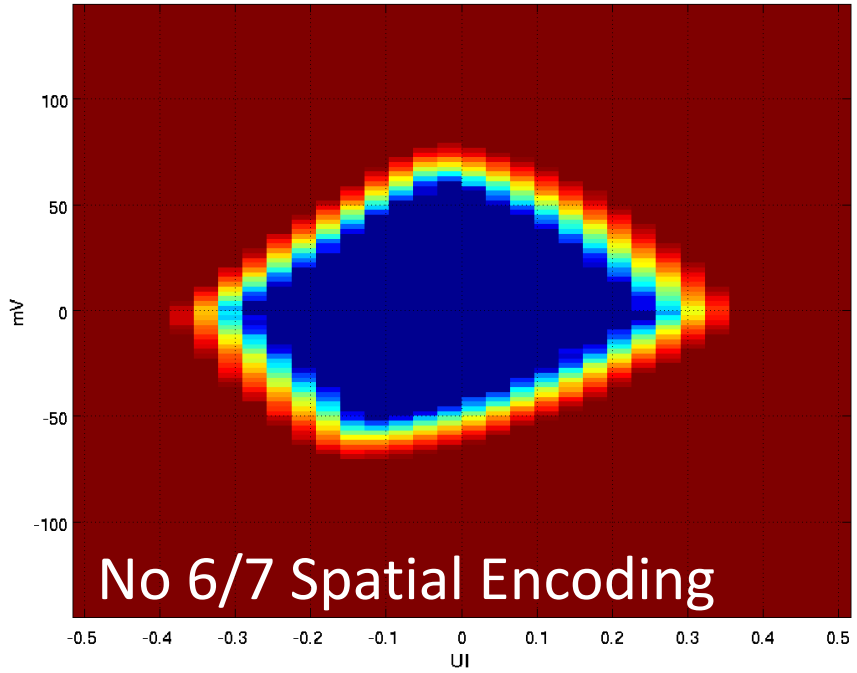
Spatial Encoding

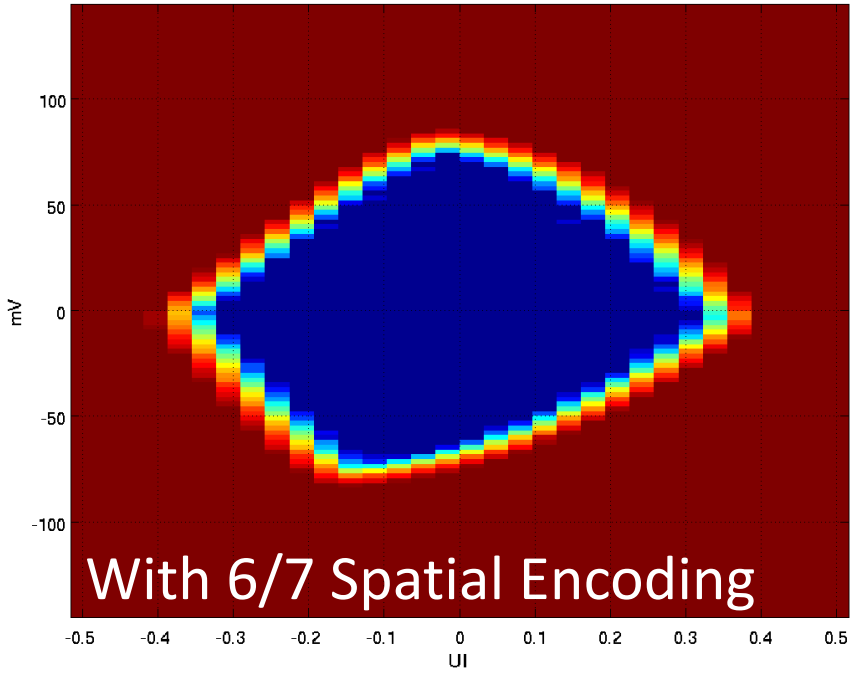




- Simulation with and without spatial encoding (15mm channel with PRBS11)

Spatial Encoding Measurements





- Results of on-board eye plotter with PRBS31, 10mm channel
- Measured with and without the TX/RX clock calibration
  - With encoding: Eye height = 160mvPP Eye width = 0.6UI
  - No encoding: Eye height = 130mvPP Eye width = 0.5UI

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UCIe – Universal Chiplet Interface Express – Emerging Standard

- Specification separated into Standard and Advanced packages
- 16-bit macro for Standard and 64-bit macro for Advanced package
- Transmitter clock adjustment, clock forwarding, per pin skew comp
- 0.3pJ/b for 16GT/s in advanced packages
- > 2Tbps/mm shoreline bandwidth for 16Gb/s in advanced packages
- BER < 1e-27 for < 16GT/s, BER < 1e-15 for >= 16GT/s
- 2ns latency for raw mode
- Only scrambling for coding, relying on path matching to mitigate supply noise induced jitter

Is this the D2D standard of the future?

Summary

- **3 types of Chiplet IO:** Serial - PAM4 differential, Parallel - advanced package, and Parallel - standard package
- **Chiplet IO choice** depends strongly on system requirements and cost: energy efficiency, shoreline density, latency, etc.
- **UltraLink** with 6B/7B spatial code offers low latency, medium energy efficiency, medium shoreline density, and low-cost standard package
- Emerging **UCIe** standard could finally unify the Chiplet IO