Glass Interposer Integration of Logic and Memory Chiplets: PPA and Power/Signal Integrity Benefits

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Agenda

- **Project Goal**

- **Progress: Glass vs. Silicon Interposer**
  - **Chiplet** design PPA comparison
  - **Interposer** design PPA & SI/PI comparison

- **Plans**

Heterogenous Integration Landscape

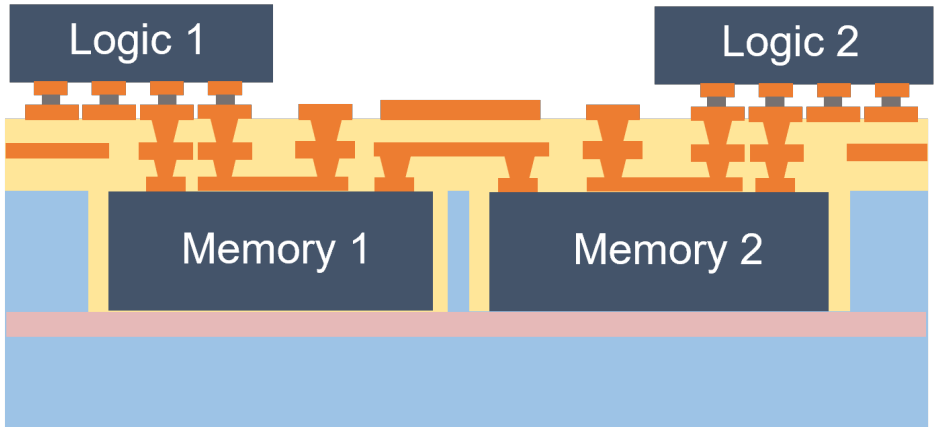
Heterogeneous Architectures

- 2D
  - Silicon
    - 2.5D TSV Interposer
    - Embedded Silicon Bridge
  - Organic
    - 2.5D Organic Interposer
    - 2.1D Organic Interposer
    - Wafer/Panel Fanout
  - Glass
    - 2.5D Glass Interposer (Chip Last)
    - 2.5D Glass Embedded (Chip First)
  - Others
    - LTCC
    - Si Micromachining
- 3D
  - TSV Based
    - 3D Stacking with Microbumps
    - 3D Stacking with Hybrid Bonding
    - IC Foundry only technologies
    - 2-16 High Stacks
  - Non-TSV Based
    - 3D Glass Embedding
    - Package Foundry
    - F2F through RDL

Our Focus

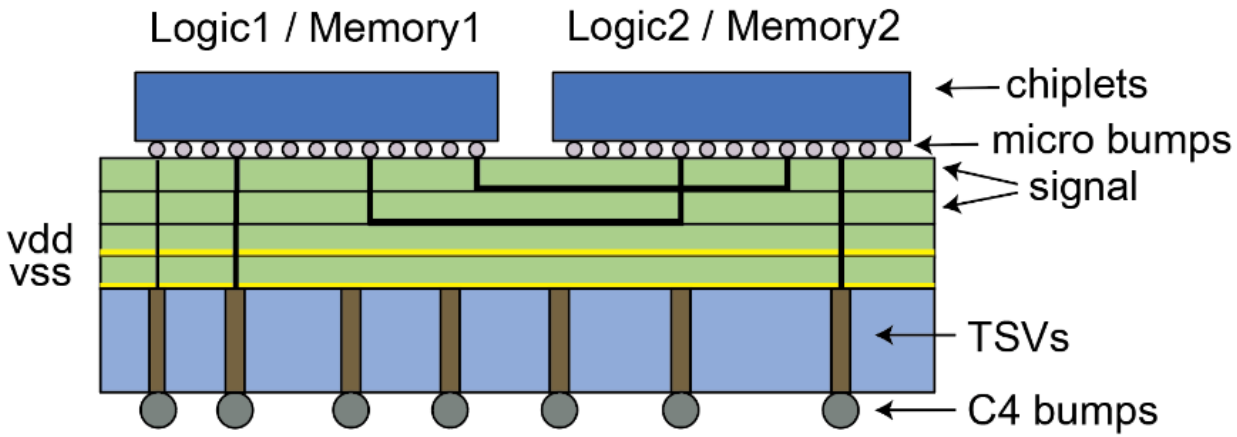
Glass Interposer

- **5.5D IC**
  - 2.5D (interposer) +
  - 3D (flipped chiplets + embedded chiplets stacked)



Glass Interposer (5.5D)

better insulation, better RF, better CTE, larger size, lower cost

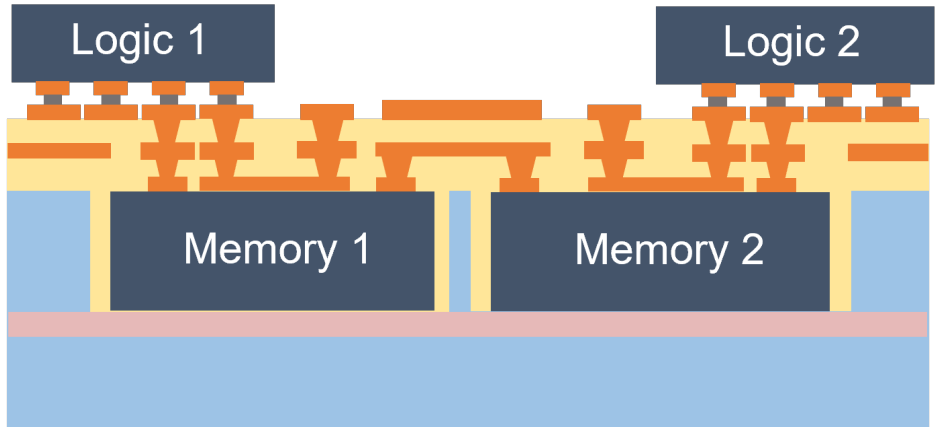


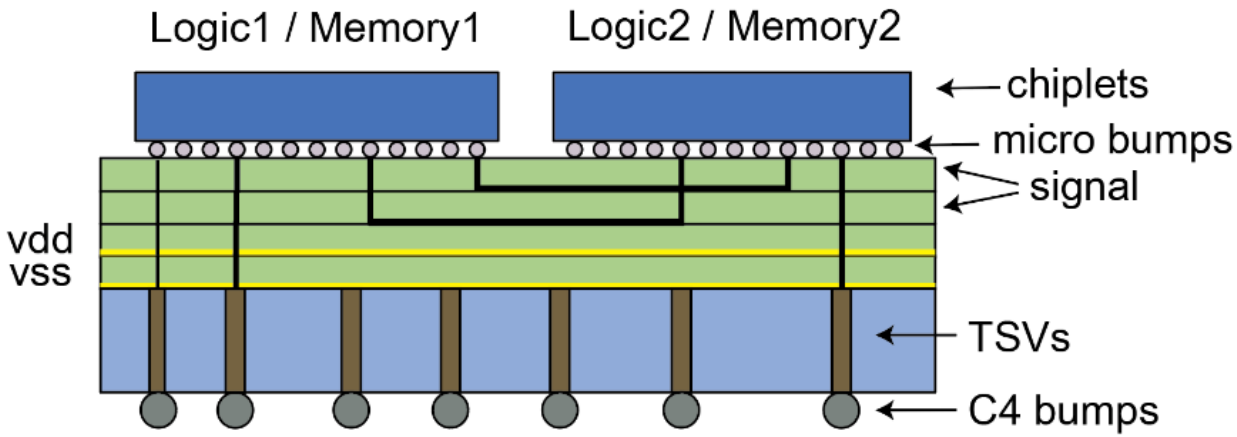
Silicon Interposer (2.5D)

better thermal conductivity

Research Goals

- **Benchmarking: Glass interposer over silicon and 2D SOC**
  - Compare PPA, and Signal/Power Integrity
  - Conduct chiplet/interposer co-design and co-analysis
  - Use GDS layouts and signoff simulations

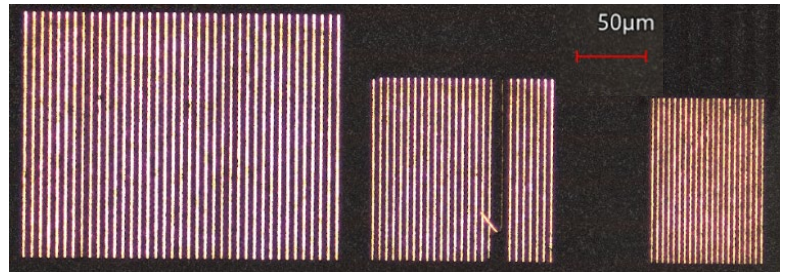


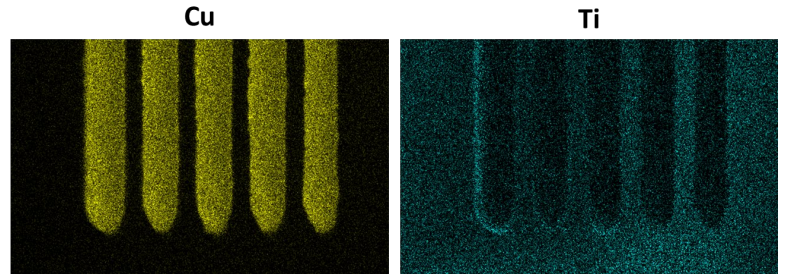


Glass Interposer PDK

- **Calibrated using measurements**

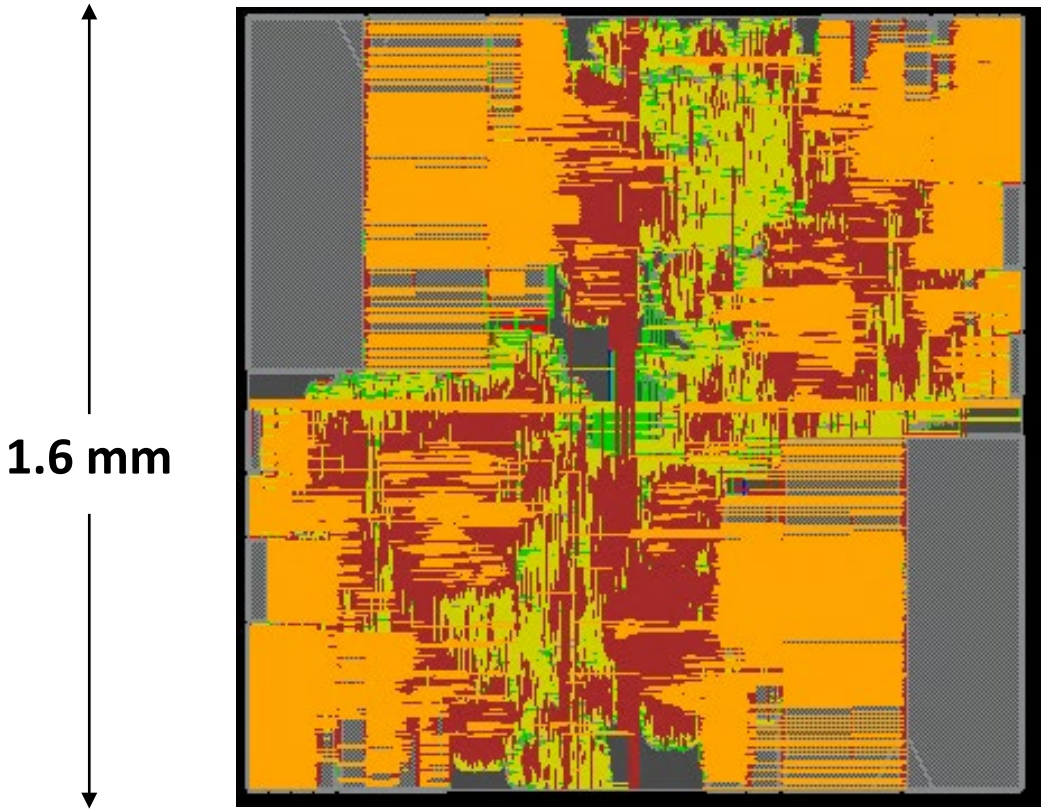
	Glass (GT-PRC)	Silicon (CoWos 65nm)
# Metal Layer	3	4
Metal thickness	4um	1um
Dielectric thickness	15um	1um
Min. Wire width / spacing	2um / 2um	0.4um / 0.4um
Via size	12um	0.4um
Pad size	22um	0.7um
Die-to-Die spacing	100um	100um
Micro-bump pitch	35um	40um
PDN width/spacing	40um / 100um	





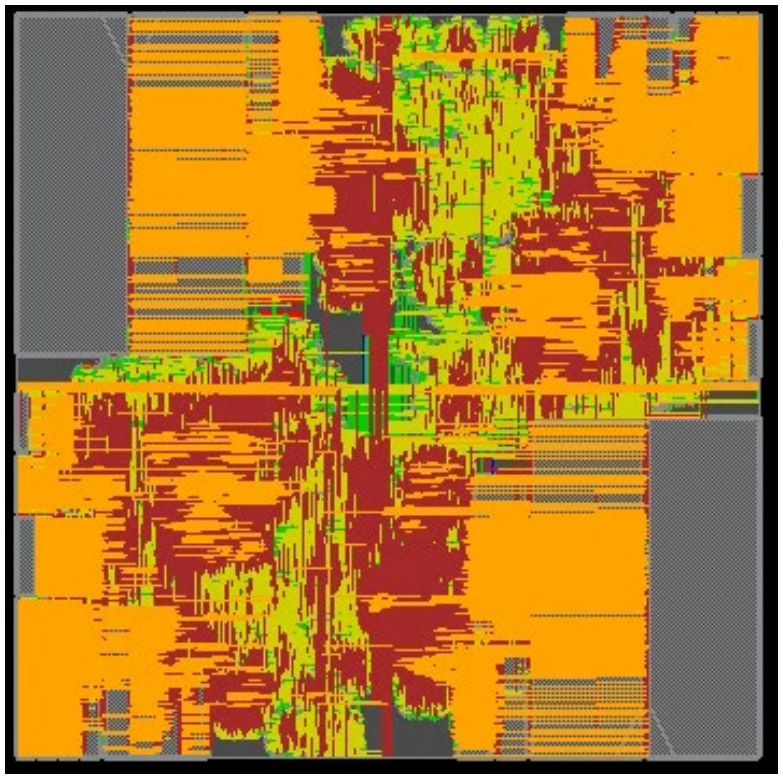
Design Settings

- **Chiplet design**
  - 400K-gate RISC-V
  - Partitioned into **4 chiplets: 2 logic, 2 memory**
  - I/O Driver: Intel AIB
  - 330mW, 645MHz, 1.6x1.6mm @ TSMC 28nm
- **Interposer design**
  - 4 chiplets placed and routed
  - Glass: GT-PRC
  - Silicon: TSMC CoWoS 65nm

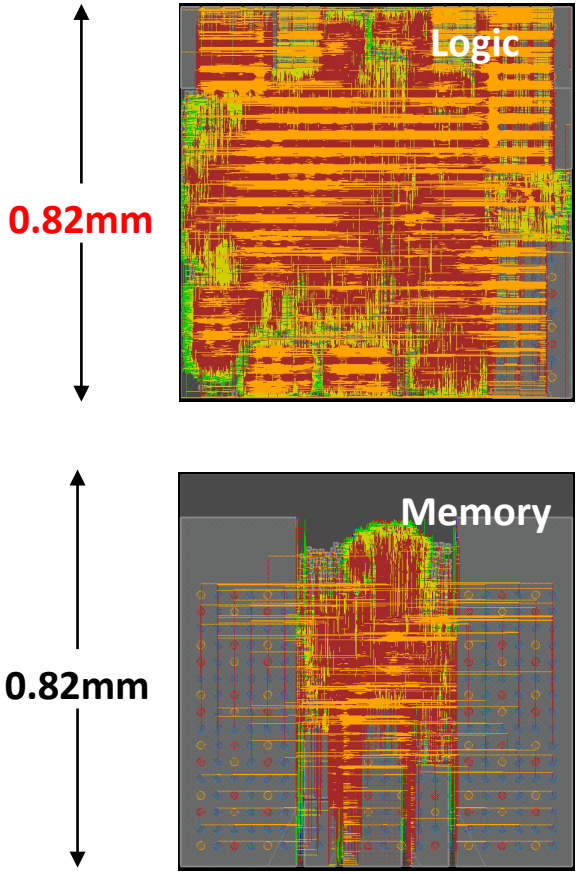


2D monolithic RISC-V
(= single chip)

Chiplet GDS Layouts

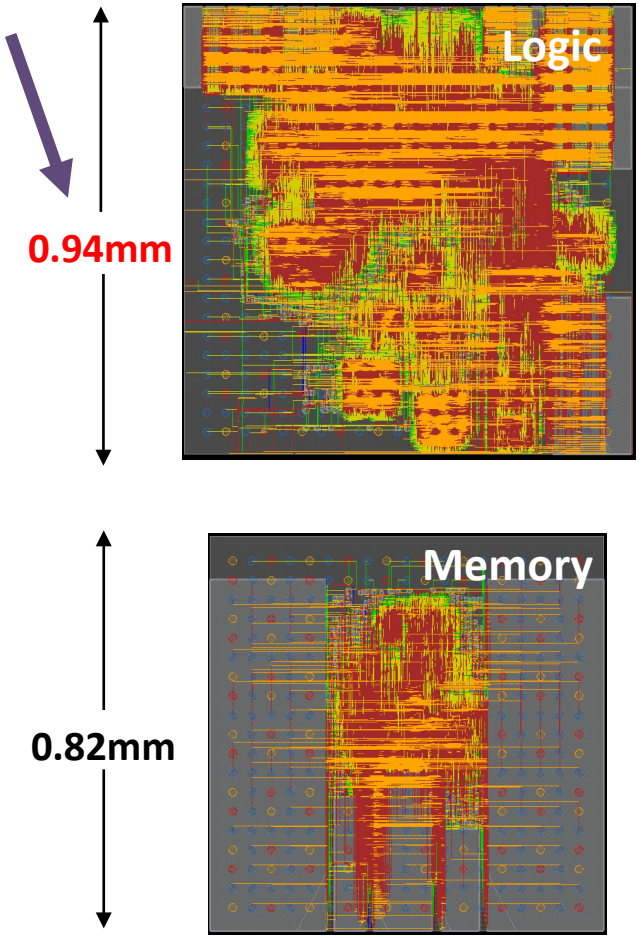


2D Monolithic



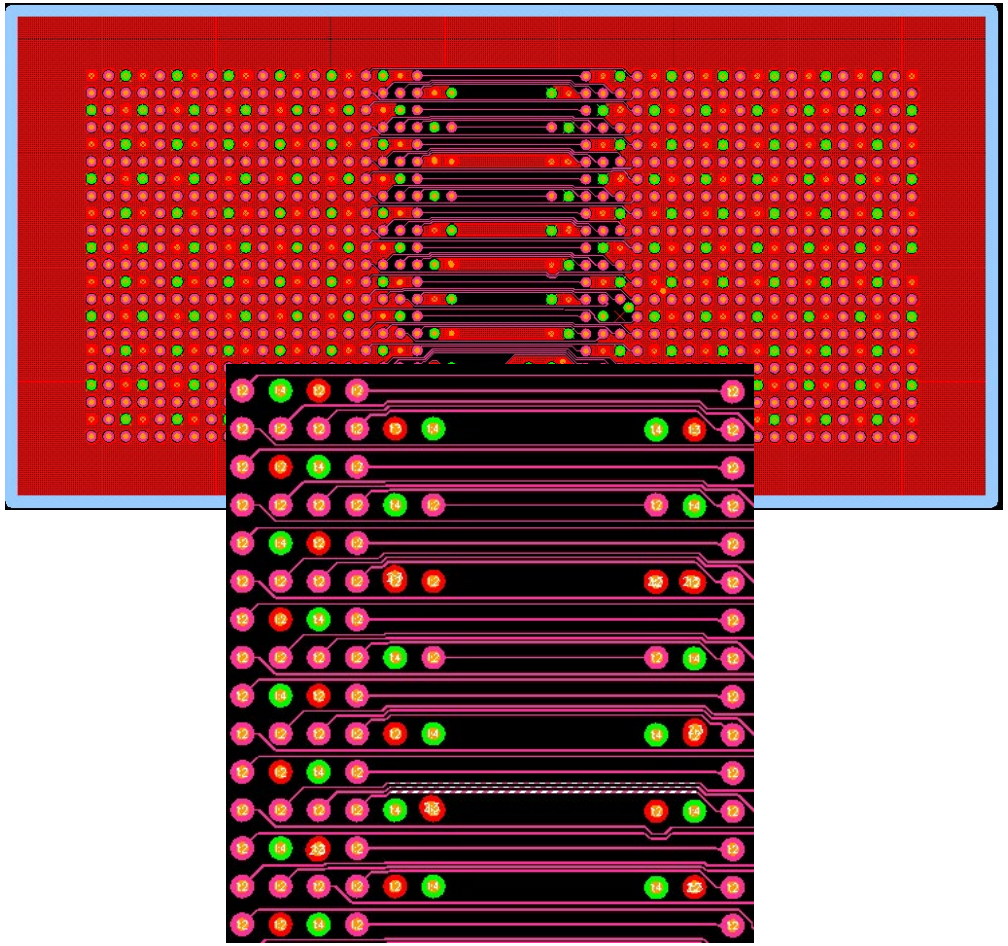
Glass Interposer

Why?

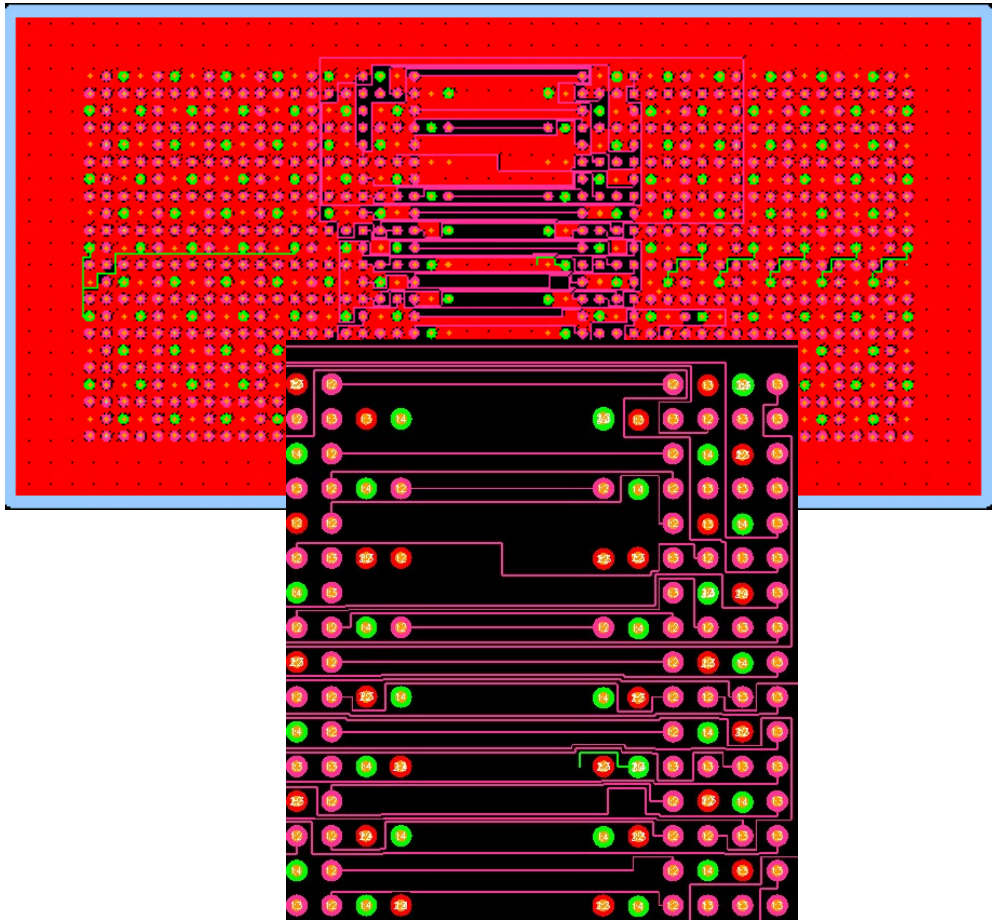


Silicon Interposer

Interposer Signal Routing (both Glass and Silicon)



diagonal (old)



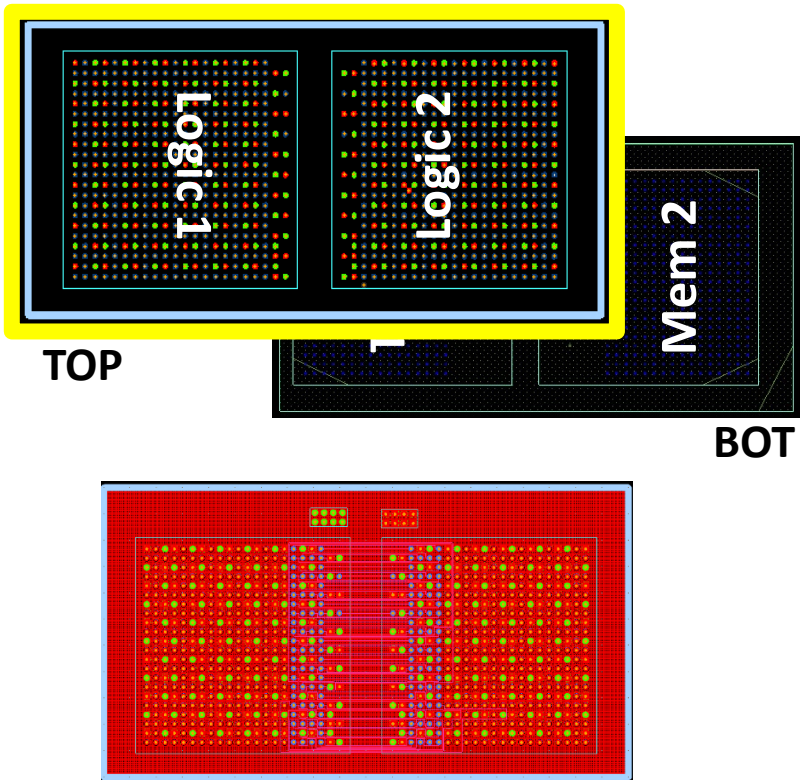
Manhattan (new)

Interposer GDS Layouts

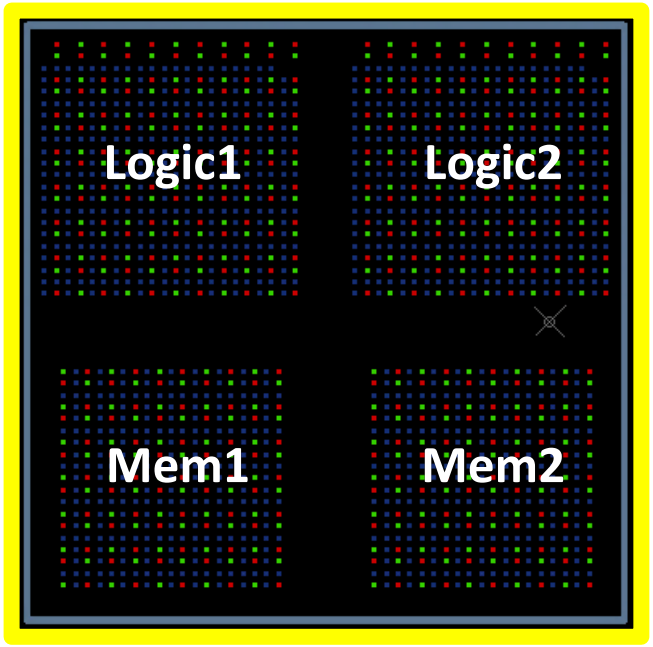
- **Glass interposer footprint is 2x smaller**
  - We embedded memory chiplets into the glass

placement

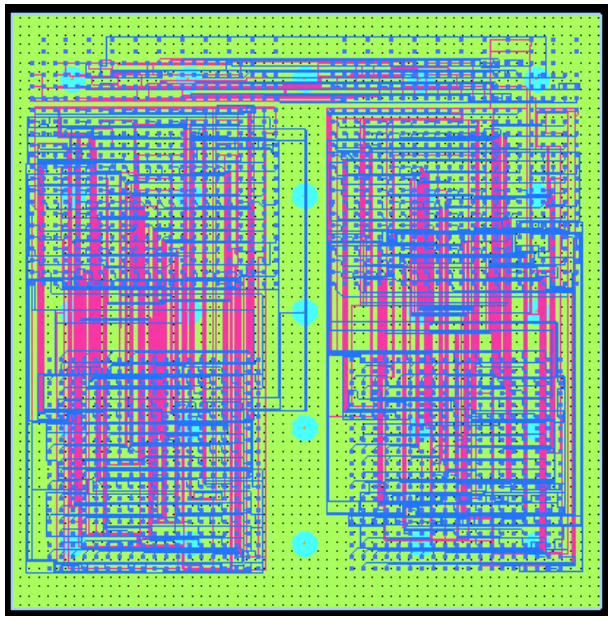
routing



Glass Interposer



placement



routing

Silicon Interposer

Area, Wirelength, Cost Comparisons

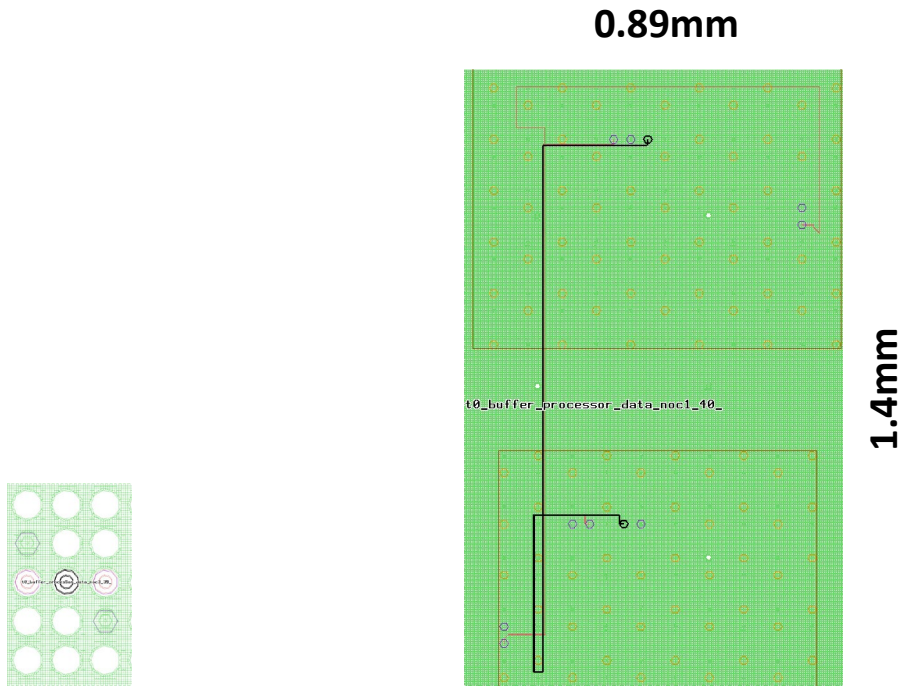
- **Huge saving with glass interposer**
  - Due to smaller footprint made possible with 3D stacking of chiplets

		2D	Glass	Silicon	Glass benefit
Area, WL, Cost	Area (mm^2)	2.56	1.87	4.84	2.6x
	Metal layer used	-	3	4	1.3x
	Total interposer WL (mm)	-	37.9	937	24.7x
	interposer via usage	-	2560	2821	1.1x
PI	PDN DC Impedance (ohm)	-	0.97	7.9	8.1x
SI	Eye width/height (Logic-to-Mem)	-	1.415ns/0.896v	1.381ns/0.817	-
Transient	Settling Time (us)		3.7	4.1	1.1x

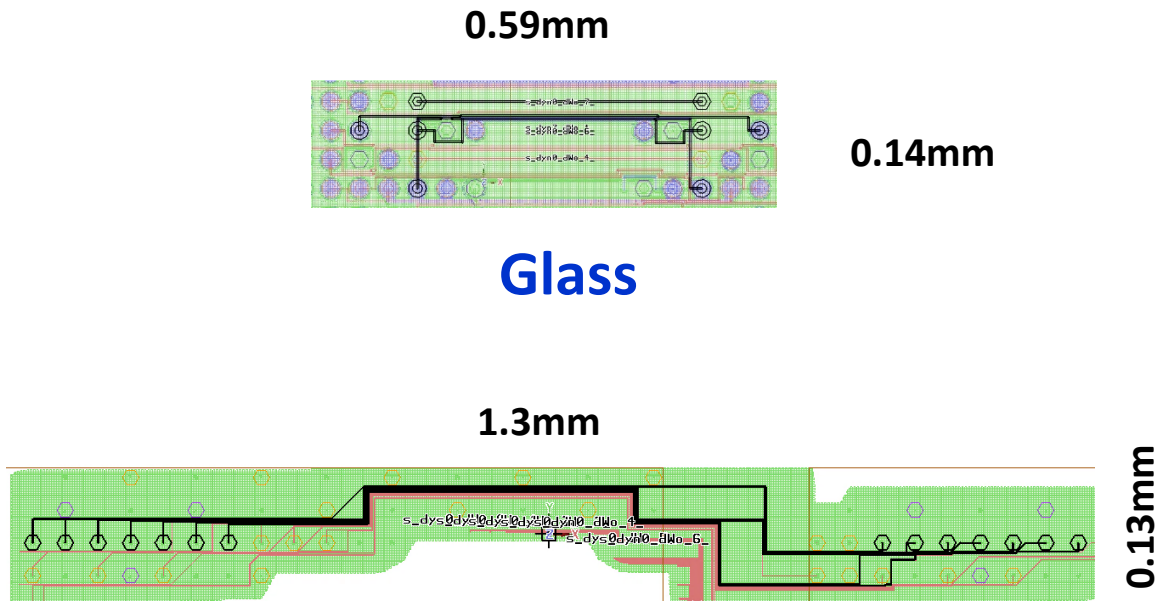
Signal Integrity Comparison

- **Nets used for SI analysis: worst-case victim**

Logic-to-Memory connection

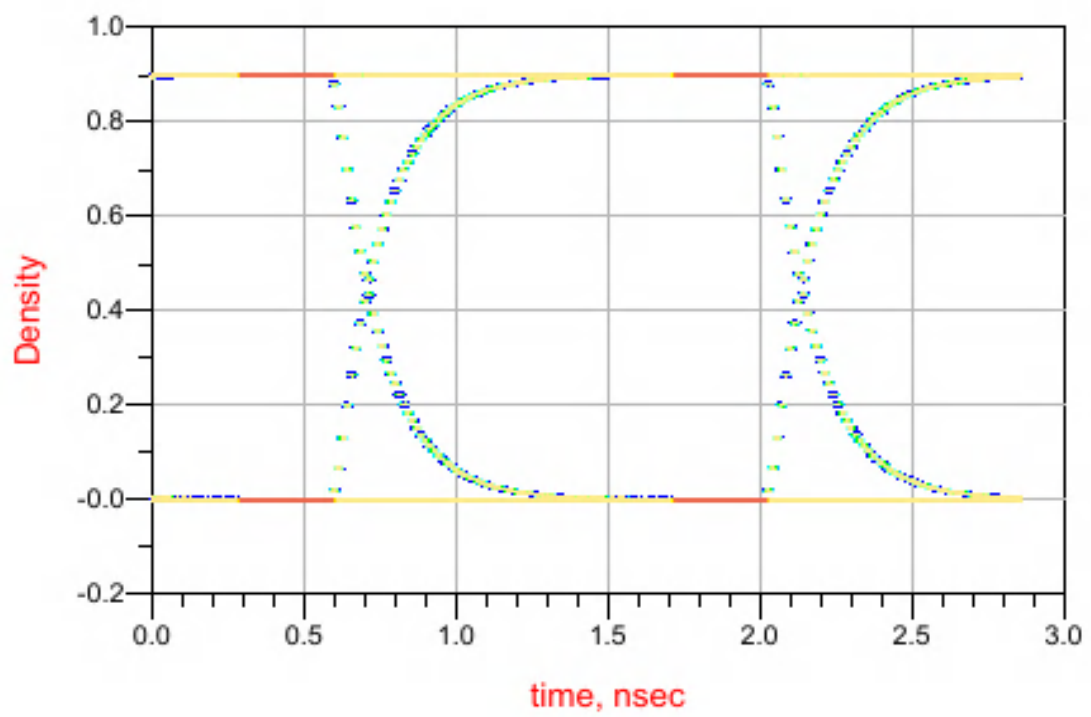


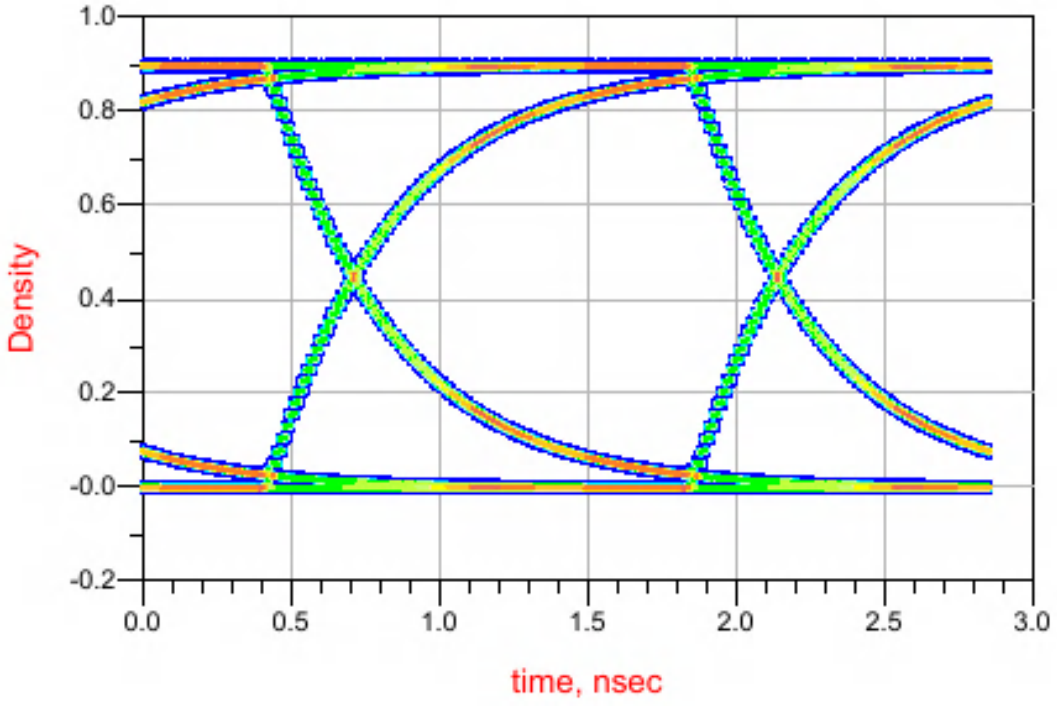
Logic-to-Logic connection



Signal Integrity Comparison (cont)

- **Eye diagram comparison: Logic-to-Memory**
  - Glass has a better eye: **due to a shorter WL**





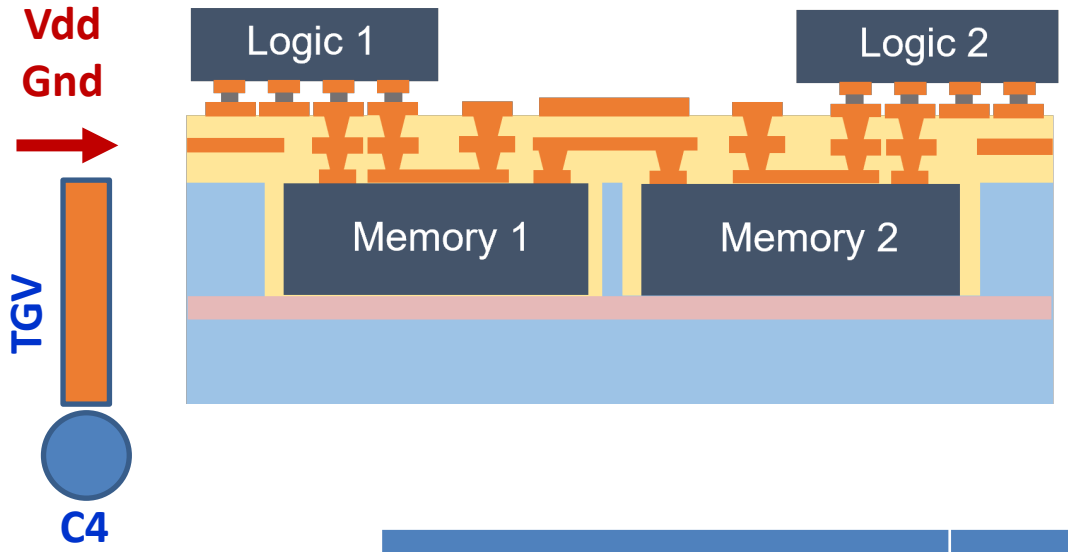
Glass W/H: 1.415ns/0.896V

Silicon W/H: 1.381ns/0.817V

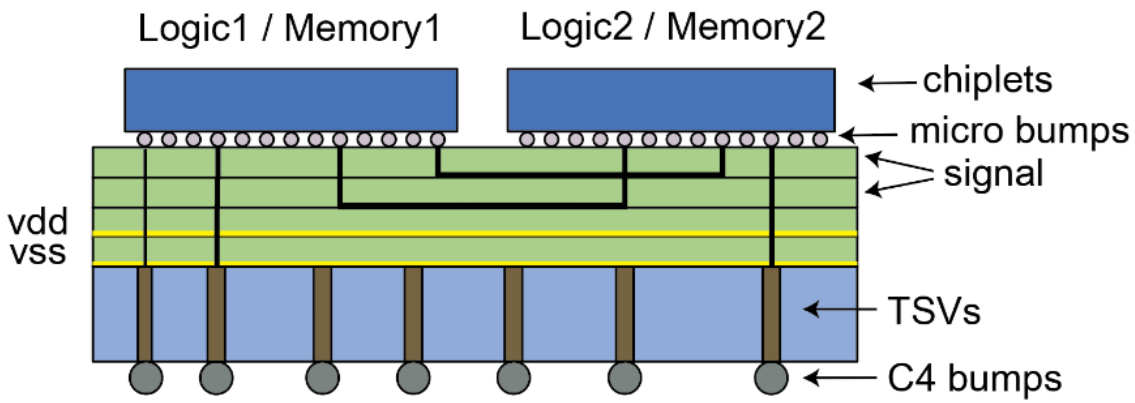
Power Integrity Comparison

- **Based on full-chip power delivery network (PDN)**

Glass



Silicon



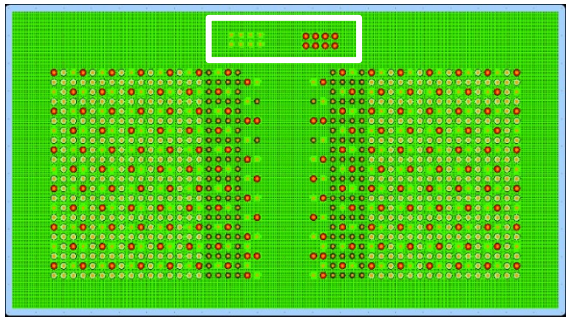
	Glass	Silicon
delivery mechanism	TGVs + wires	TSV + wires
topology	plane	plane or grid

Power Integrity Comparison (cont)

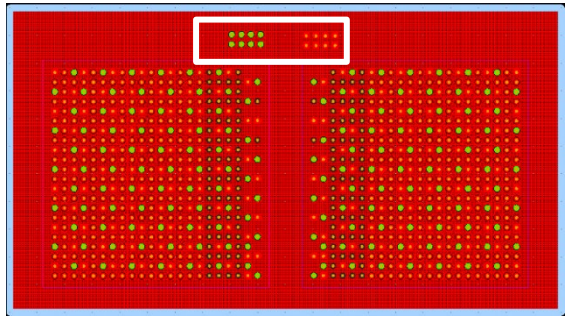
- **PDN routing (plane for glass, grid for silicon)**

TGV (Power port)

M2 (Power)

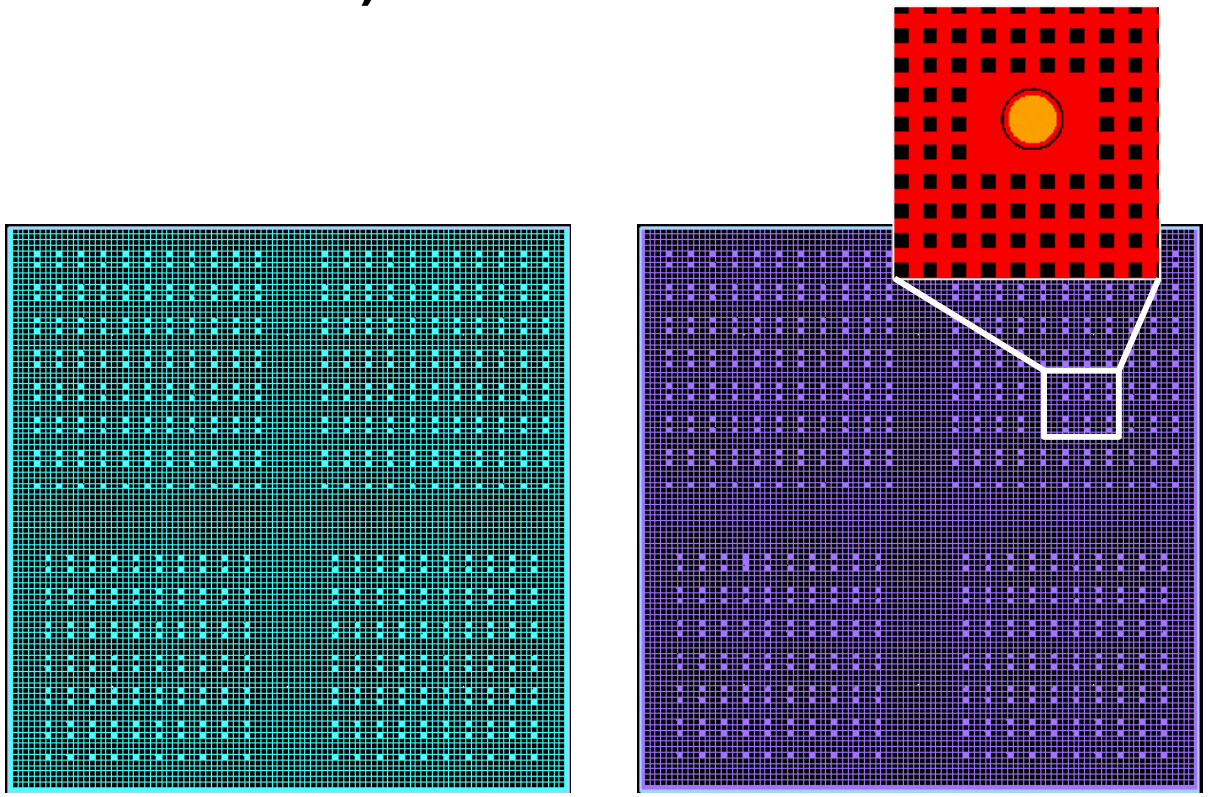


M3 (Ground)



Glass Interposer

TSV (Power port)



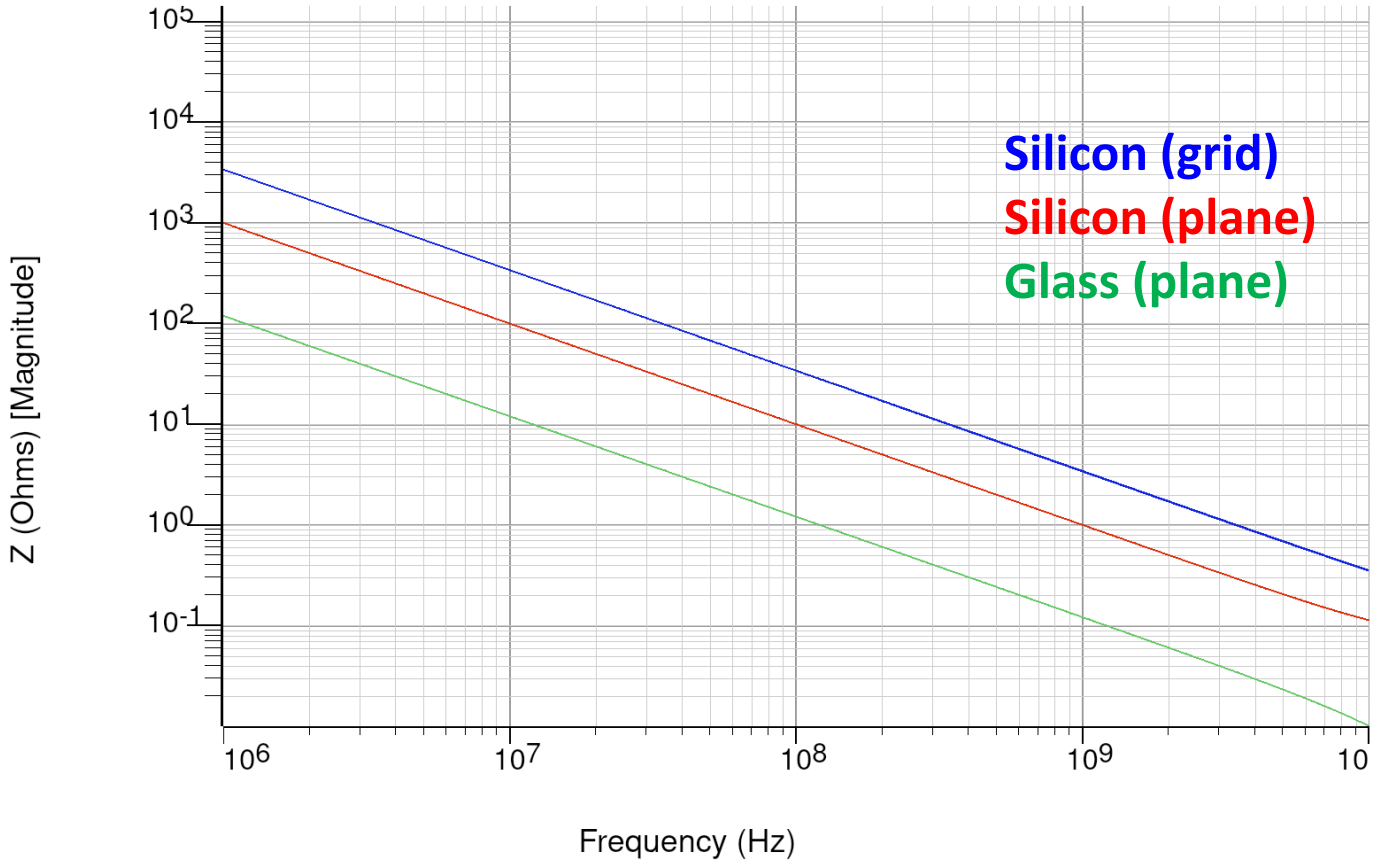
M3 (Power)

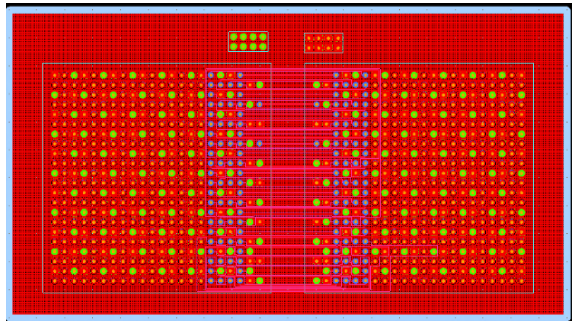
M4 (Ground)

Silicon Interposer (plane)

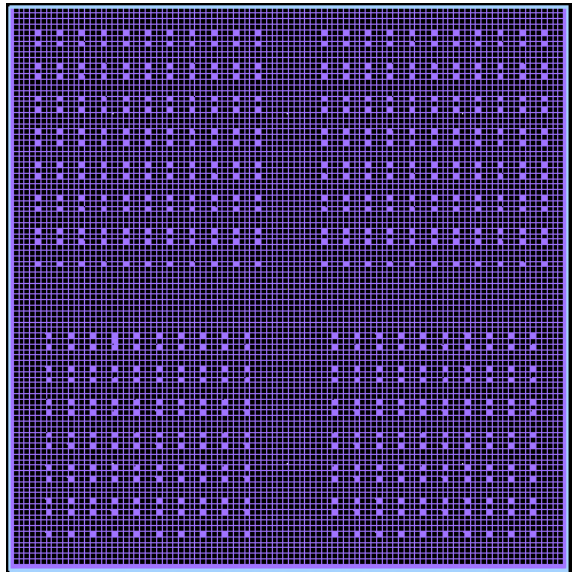
Power Integrity Comparison (cont)

- **PDN impedance comparison**
  - Glass shows the lowest impedance: **due to smaller area**





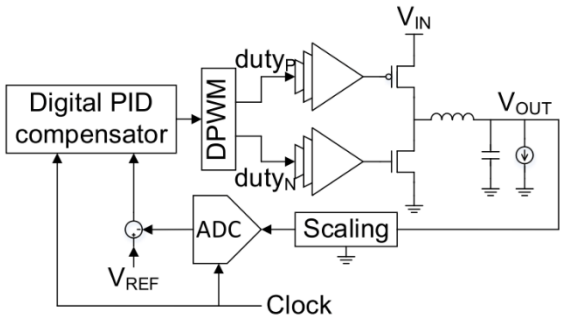
Glass

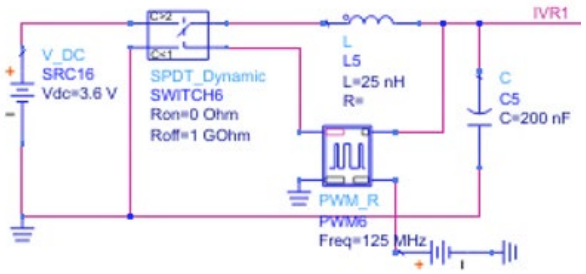


Silicon

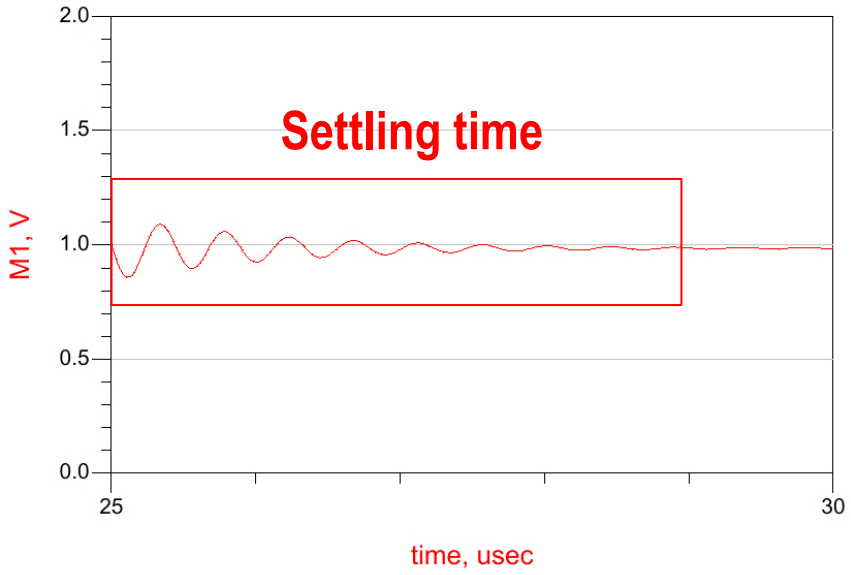
Power Integrity Comparison (cont)

- **Power transient: 125MHz switching input @ memory chiplet**
  - Glass shows better transient: **due to lower PDN impedance + lower power**

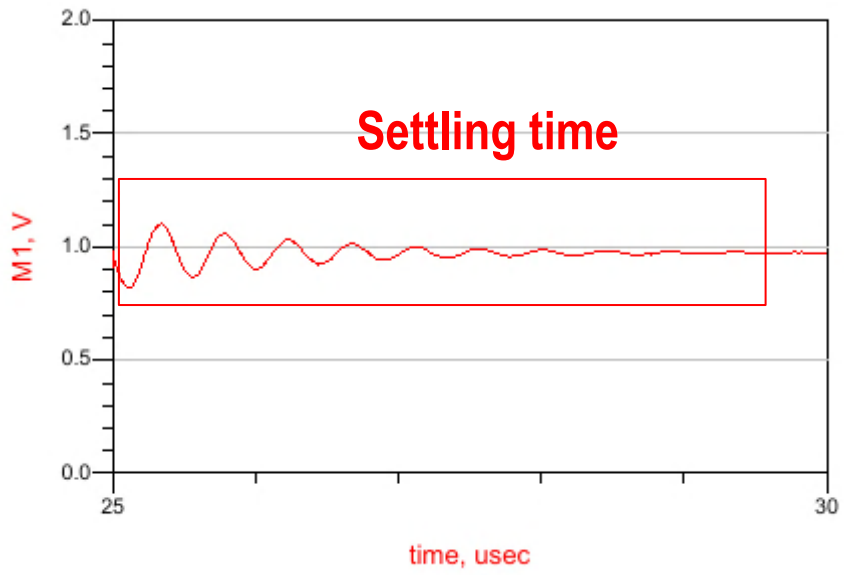




IVR module added



Glass: 3.7us, 0.983V



Silicon: 4.1us, 0.973V

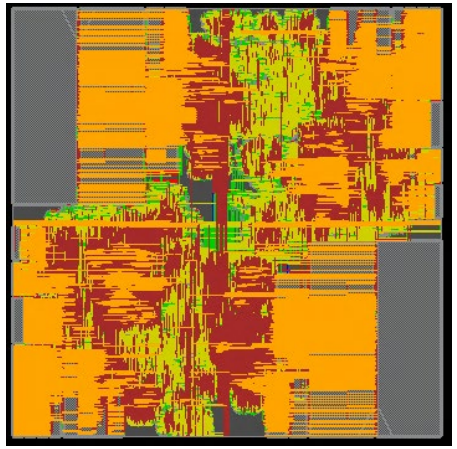
PPA + SI/PI Comparisons

- **Huge saving with glass interposer**
  - Smaller footprint made possible with 3D stacking of chiplets

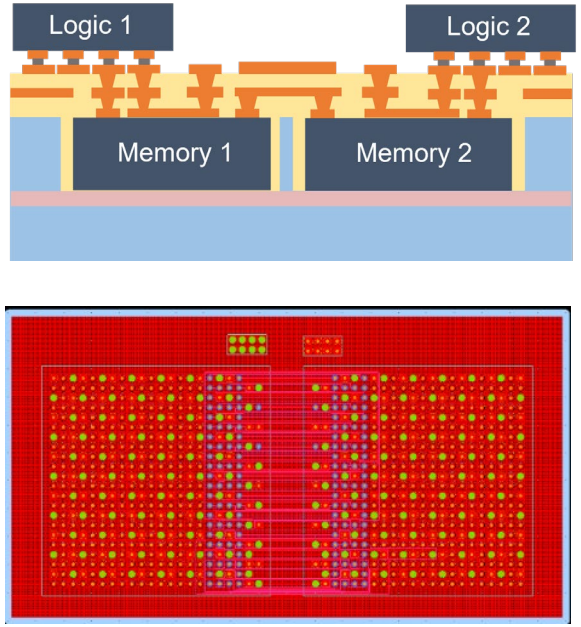
		2D	Glass	Silicon	Glass benefit
Area, WL, Cost	Area (mm^2)	2.56	1.87	4.84	2.6x
	Metal layer used	-	3	4	1.3x
	Total interposer WL (mm)	-	37.9	937	24.7x
	interposer via usage	-	2560	2821	1.1x
PI	PDN DC Impedance (ohm)	-	0.97	7.9	8.1x
SI	Eye width/height (Logic-to-Mem)	-	1.415ns/0.896v	1.381ns/0.817	-
Transient	Settling Time (us)		3.7	4.1	1.1x

Summary

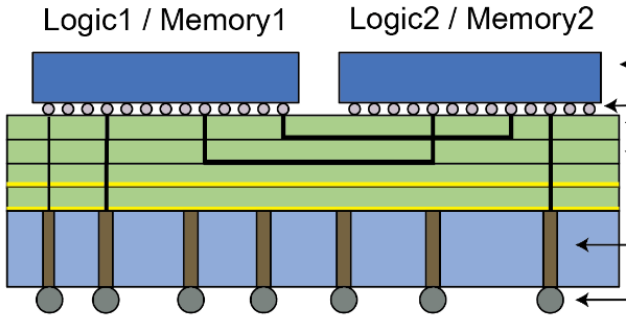
- **Glass vs. silicon interposer comparison**
  - Glass supports cheap solution to 3D chiplet stacking
  - Glass interposer shows better PPA + SI/PI

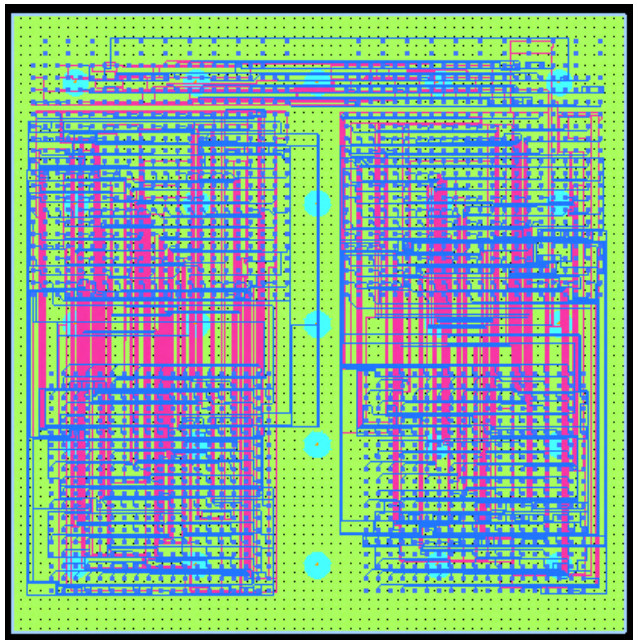


SoC



Glass Interposer





Silicon Interposer

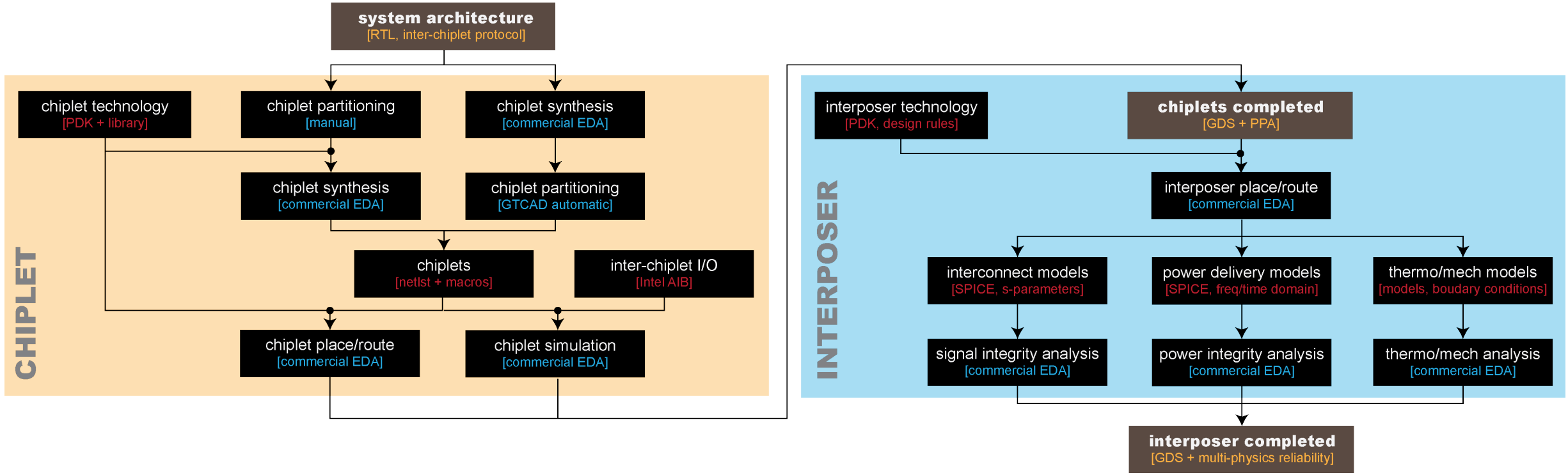
Future Directions

- **Thermal analysis**
  - 2D vs. Glass vs. Silicon
- **Comparison with organic (LCP) interposer**
  - 2D vs. Glass vs. Silicon vs. LCP
- **Explore chiplet partitioning options**
- **Migrate to larger benchmark and reuse chiplets**

SUPPLEMENT

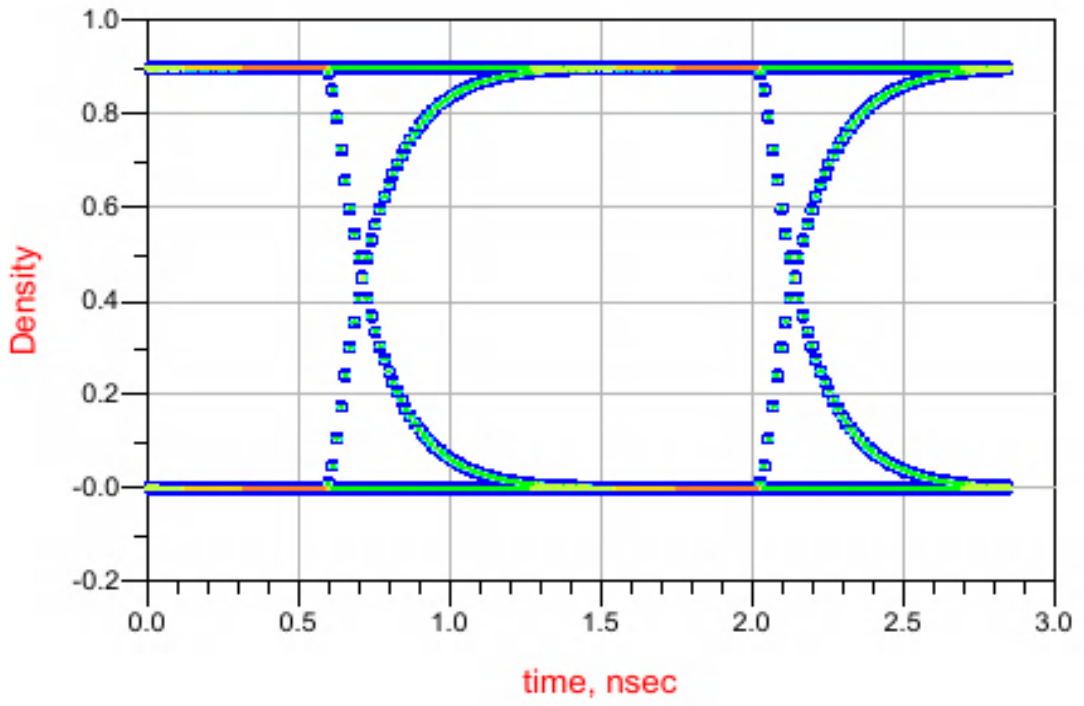
Chiplet/Package Co-Design Tool/Flow

- **Chiplet/package co-design**
  - Chiplet: Cadence and Synopsys IC, Interposer: Siemens
  - Enhanced with our **custom plug-ins (auto-chiplet partitioner, ML-based passive designer)**

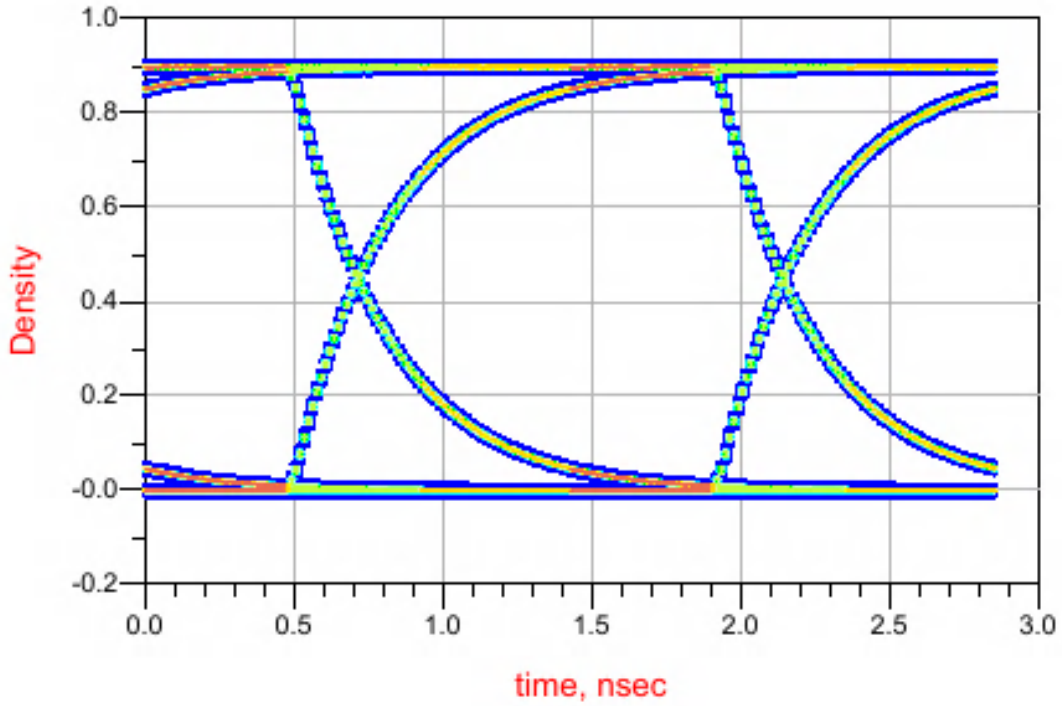


Signal Integrity Comparison (cont)

- **Eye diagram comparison: Logic-to-Logic**
  - Glass has a better eye: **due to a shorter WL**



Glass W/H: 1.401ns/0.88V



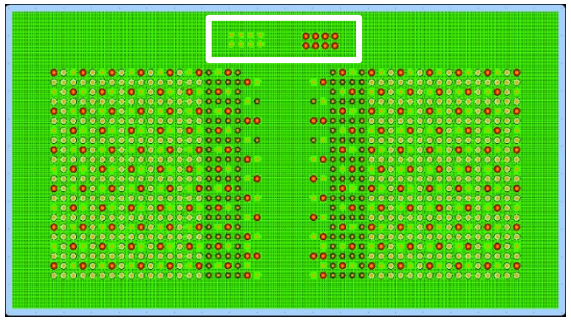
Silicon W/H: 1.387ns/0.851V

Power Integrity Comparison (cont)

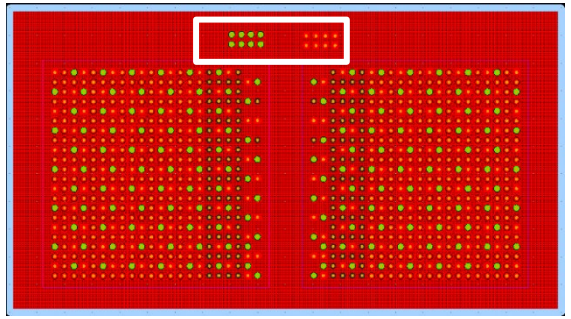
- **PDN routing (plane-style)**

TGV (Power port)

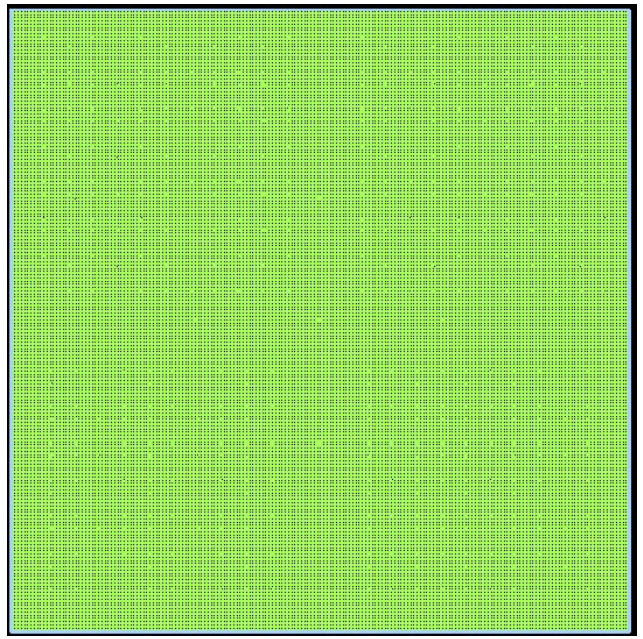
M2 (Power)



M3 (Ground)

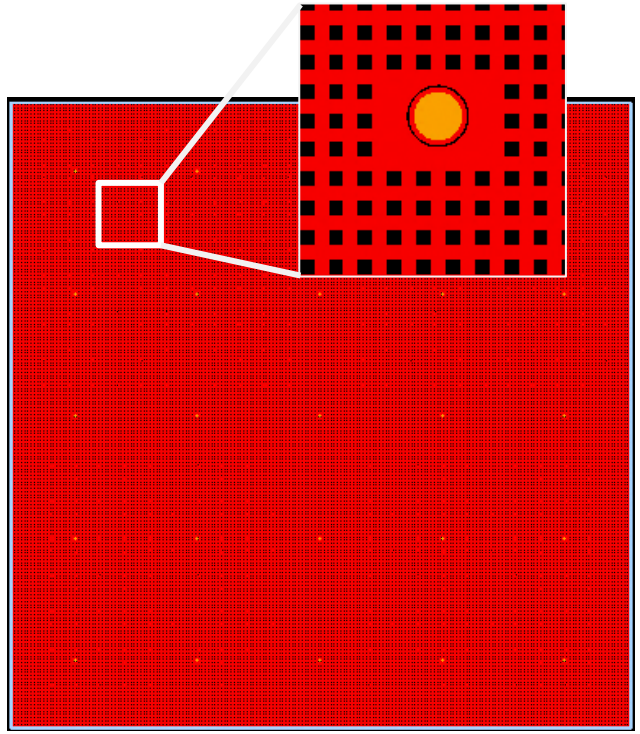


Glass Interposer



M3 (Power)

TSV (Power port)



M4 (Ground)

Silicon Interposer (plane)