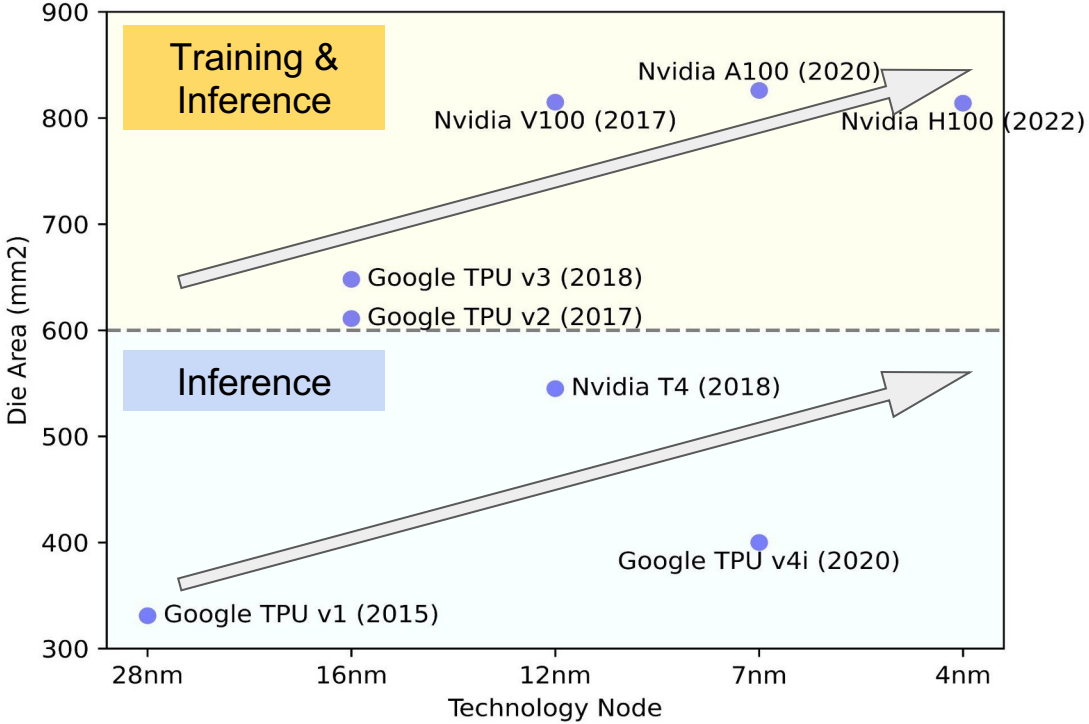
Cost-Aware Exploration for Chiplet-Based Architecture with Advanced Packaging Technologies

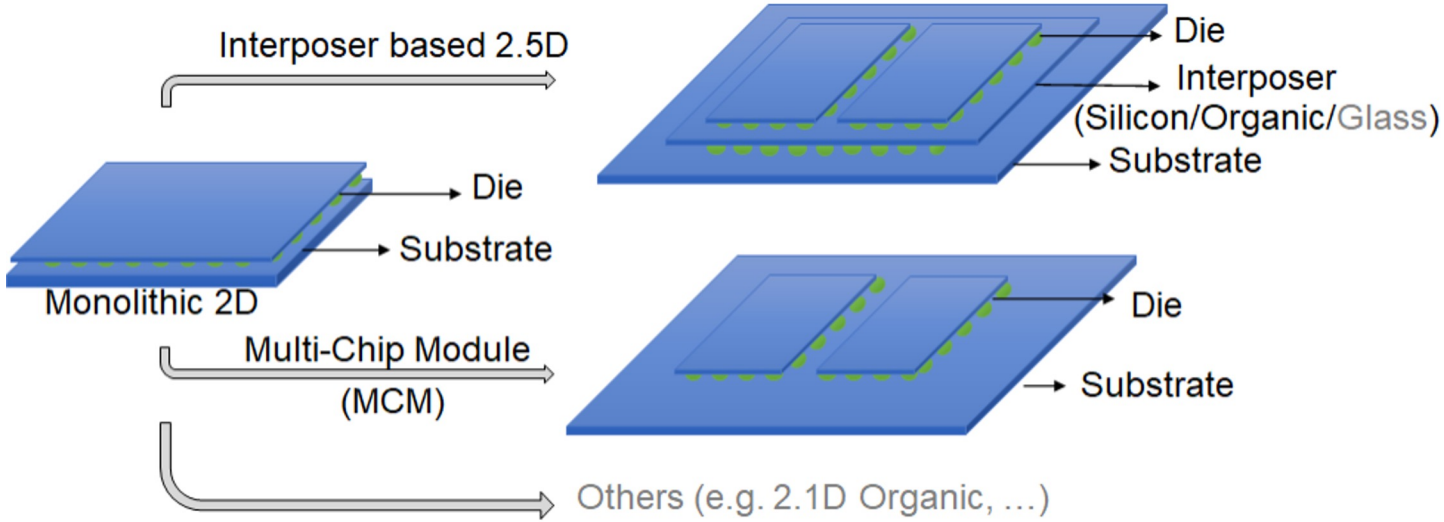
Tianqi Tang, Yuan Xie
tianqi_tang@ucsb.edu, yuanxie@ece.ucsb.edu
University of California, Santa Barbara

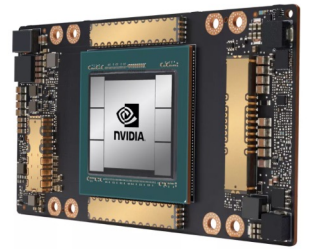
Motivation (1/3): Trends of ML Accelerators in Datacenter



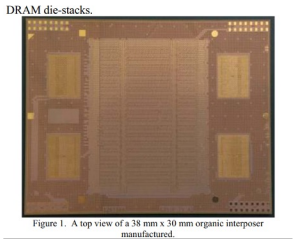
- **Tech Node** scales down while **Silicon Area** gets larger.
- From Cost Perspective, Monolithic vs Chiplet 🤔

Motivation (2/3): The Advanced Package Technologies

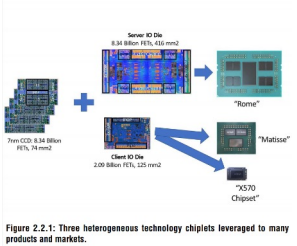




Silicon interposer based 2.5D
Nvidia Ampere

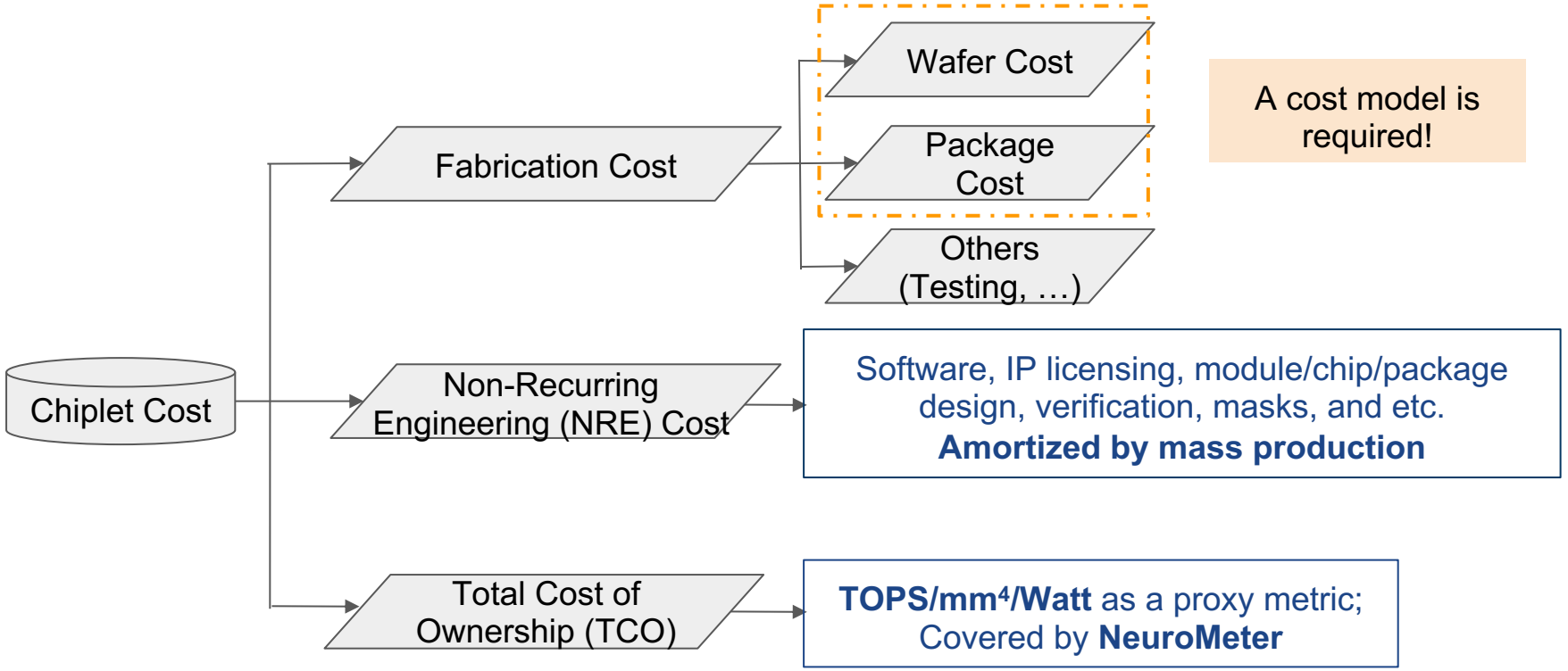


Organic interposer based 2.5D
[TETC'2016]

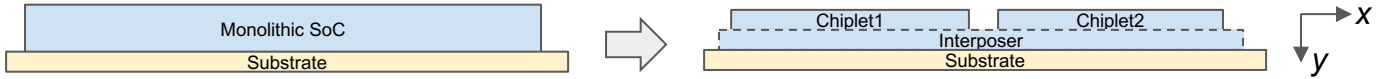


MCM, AMD Mantissa & Rome
[ISSCC'2020]

Motivation(3/3): Cost Model of Chiplet System



Manufacture Cost Modeling for Chiplet-based Architecture



X-axis: Chiplet partition and additional die-die interface, Y-axis: Interconnect offloading

Metal & Build-up Layers

$A_{sub} = A_{int} \cdot f_{int} = \sum A_{die} \cdot f_{die}$

User Input

- Die Area
- Tech Node

Backend Data

IC KNOWLEDGE LLC

- Raw Cost C_{wafer}, C_{panel}
- Defect Rate ϕ_{wafer}

Wafer Cost

Chiplet / Silicon Interposer

$$C_{sil\_int} = \frac{C_{wafer}}{N_{sil\_int}} = \frac{C_{wafer}}{\frac{\pi \times (\Phi_{wafer}/2)^2}{A_{sil\_int}} - \frac{\pi \times \Phi_{wafer}}{\sqrt{2} \times A_{sil\_int}}}$$

$$Y_{sil\_int} = Y_{wafer} \times (1 + \frac{A_{sil\_int} D_0}{\alpha})^{-\alpha}$$

Organic

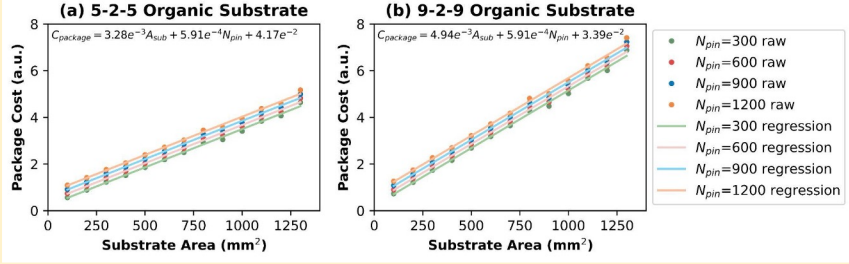
$$C_{org\_int} = \frac{C_{panel}}{N_{org\_int}} = \frac{C_{panel}}{A_{panel}/A_{org\_int}}$$

$$Y_{org\_int} = Y_{panel} \times (1 + \frac{A_{org\_int} D_0}{\alpha})^{-\alpha}$$

Package Cost:Substrate

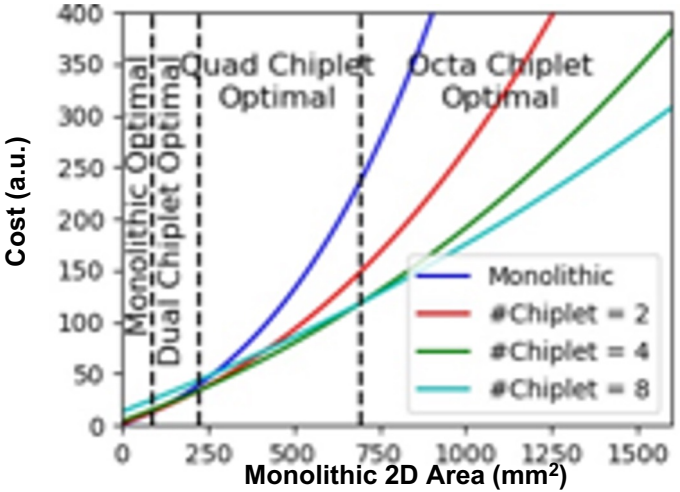
A regression-based analytical package cost model

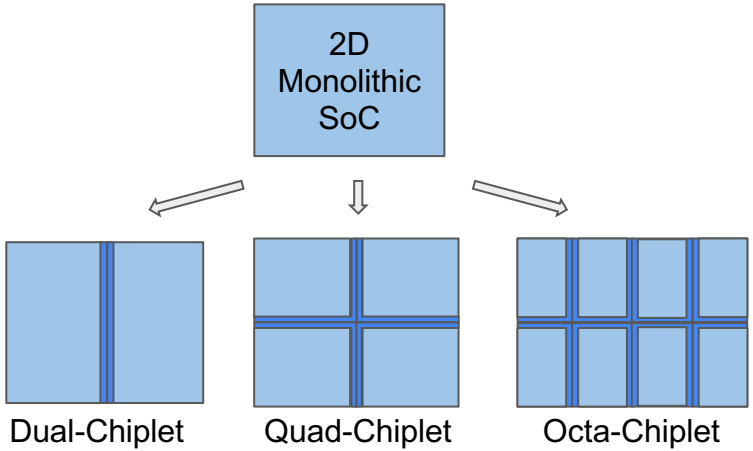
Substrate area (A_{sub}), I/O density (N_{pin}), #(Build-up layers)



Case Study (1/2): Homogeneous Chiplet System

- The optimal partition granularity



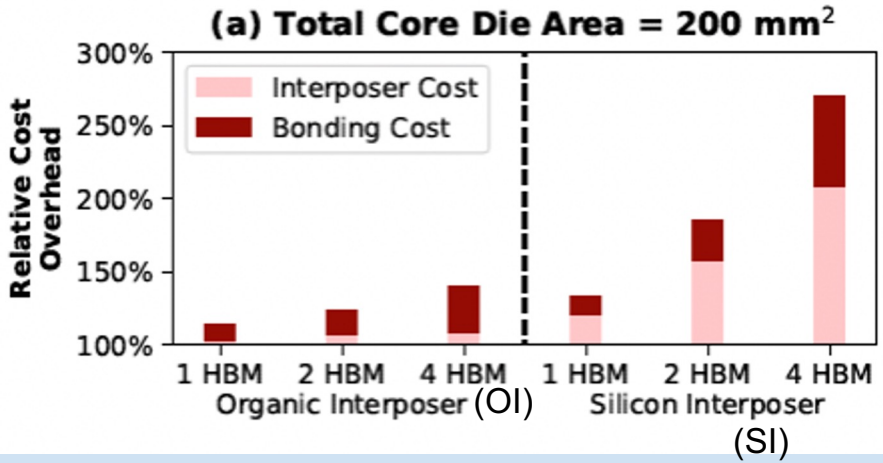


Observation:

- Fine-grained partition (or larger #Chiplet) does not always win in terms of cost.
- Under the optimal granularity, ***Area_per_chiplet*** falls in the range of 100mm^2 to 200mm^2.
- MCM system can also get satisfying cost benefits, but silicon interposer CANNOT.

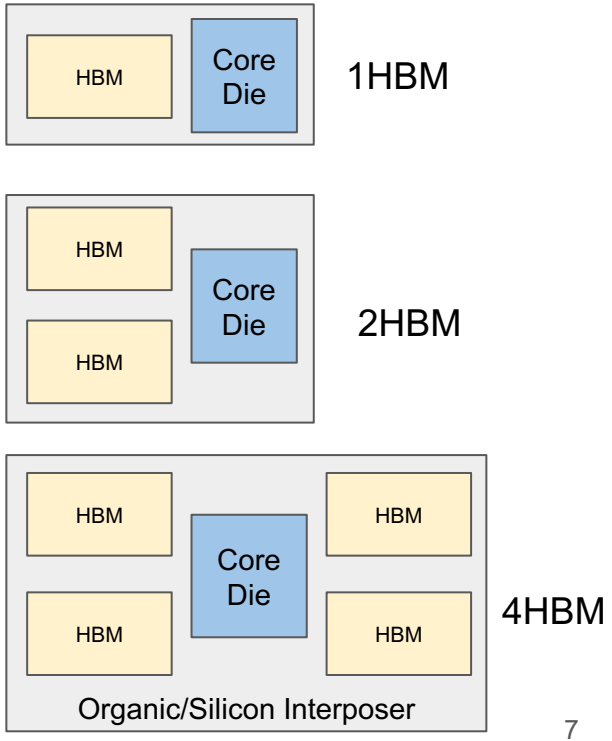
Case Study (2/2): Heterogeneous Chiplet System

- Heterogeneous Chiplet System with HBM Stacks



Observation:

- OI introduces less than 50% overhead for HBM stacks; while SI gets much larger cost overhead;
- The bonding cost takes the majority in OI; while the interposer cost takes the majority in SI.



Summary

- Cost Model for Chiplet System with Advanced Package Technologies:
  - Supporting the cost of silicon/organic interposer based 2.5D and MCM
  - Cost-aware study on the homogeneous/heterogeneous chiplet systems

Thanks for Your Attention!

Q&A