ODSA OpenHBI Workstream proposal

Open High Bandwidth Interconnect for chiplets

ODSA Workshop
Dec 18, 2019

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Outline

- The Proposal – A new ODSA OpenHBI Workstream
- Introduction to OpenHBI
- Scope of OpenHBI spec work
- Target Milestones and Roadmap
- Call for Interest
Problem Statements and Goals for OpenHBI Proposal

> A wide range of I/O types and electricals can be used for chiplets and die-to-die interconnects, BUT………

> It takes a lot of efforts and time to:
  – Standardize the I/O type, electrical and channels
  – Interoperability and Compliance at co-packaging level
  – Design IPs, Verification IPs, Test ecosystems build up
  – Manufacturability between heterogenous chiplets from different vendors

> OpenHBI proposal leverages JEDEC HBM specifications which is:
  – Proven and matured standards
  – Highest volume standard-based chiplet application
    - Broad deployment in GPU, FPGA, Networking, AI, 5G and many more
  – High performance and energy efficiency with advanced roadmap
The Proposal

> Start a new ODSA “OpenHBI Workstream” dedicated to create a high-performance die-2-die interconnect over Si Interposer, FO or fine-pitch organic substrate that meets next gen requirements:

  >> High performance  > 500Gbps/mm
  >> Energy efficient  ~1pJ/bit or better
  >> Low latency      < 5ns
  >> Reliable BER    < 1e-15
  >> Scalable and Extensible
  >> Manufacturable (with Lane Repair capability)

> OpenHBI PHY (L0) and Link (L1) definition

  >> Plan to support ODSA TPA proposal (Transport and Protocol Agnostic interface)
OpenHBI : Key Features

> Leverage JEDEC HBM IO types, electricals and signal designations

> Supports Silicon interposer or similar technologies
  >> e.g., FO-WLP, fine pitch organic substrate

> Multi-Terabits/sec BW per full OpenHBI PHY unit
  >> Symmetric, dual-simplex, multi-channel chip-to-chip interface
  >> Scalable to well beyond 10Tbps with multiple OpenHBI PHY units
  >> Flexible orientation; supports same-orientation and 180° rotated die use cases.
  >> Yield enhancement with “Lane repair” feature in either orientations

> Optimized for shorter reach and scalable number of channels for target use cases.

> A device conformed to OpenHBI can be designed to support both OpenHBI and JEDEC HBM memory devices
OpenHBI DWORD (L0 unit) and Channel

- OpenHBI consists of eight 128-bit Channels; each consists of four 32-bit sub-channel called “DWORD” or L0 unit
  - Each L0 unit consists of 32 DQs, PAR, 4 DM (additional 12.5% to DQ bandwidth), 4 DBI and RD0/1 (lane repair)

OpenHBI Channel:

- Dual simplex link with 2 x L0 Tx + 2 x L0 Rx ➔ total 128 DQs + 4 PAR + 16 DM
- Bits carried over “DM” can be mapped to protocol-specific framing, flow control and vendor-defined info etc.
- DBI pins are used to minimize signal toggling to maximize energy efficiency

<table>
<thead>
<tr>
<th>Mechanical Bumps</th>
<th>Direct Access Test Port</th>
<th>Power Supply Region</th>
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| Depolyed microcarrier area
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JEDEC HBM2

Bump organizations

(available for public download)

OpenHBI Channel

Dual simplex, 2 L0 Tx, 2 L0 Rx

- OHBI DWORD = L0 Unit

OpenHBI Use Cases

HBM Use Cases

- HBM DWORD

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OpenHBI Scalability

> **OpenHBI**
  >> 4 group sizes to optimize for various use cases
  > 1, 2, 4 and 8 Channels (1/8th, 1/4th, 1/2 and Full OpenHBI PHY unit)
  > E.g., 400G, 800G, 1.6T and 3.2Tbps @3.2Gbps/pin **true data bandwidth**, (protocol and flow control overhead mapped to carry over repurposed DM signals)
  >> Scalable with multiple full OpenHBI PHY units

> **Bifurcation**
  >> All OpenHBI channels are symmetric and identical
  >> A multi-channel OpenHBI can be designed to support bifurcation to connect with multiple chiplets
  > E.g., 8-Ch can bifurcate to 2x 4-Ch OpenHBI interfaces

> **Optional JEDEC HBM backward compatibility**
  >> A device conformed to OpenHBI can be designed to support both OpenHBI and JEDEC HBM memory devices
Orientation-Independent Routing and Lane Repair

- OpenHBI PHY supports same orientation or 180° rotated orientation routing
  - Include routing techniques to support both orientations
  - Support JEDEC RD0/RD1 redundant wiring to enhance packaging yield in both orientations
# Figure of Merits – OpenHBI

<table>
<thead>
<tr>
<th>Metrics</th>
<th>OpenHBI-2 (based on HBM2/2e-PHY)</th>
<th>OpenHBI-3 (based on HBM3-PHY*)</th>
<th>Next Gen**</th>
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<tbody>
<tr>
<td><strong>OpenHBI</strong></td>
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<tr>
<td>Link Rate (Gbps)</td>
<td>2.4G – 3.2G</td>
<td>4G – 6.4G</td>
<td>&gt;&gt; 8G **</td>
</tr>
<tr>
<td>Reach (mm)</td>
<td>3mm</td>
<td>3mm</td>
<td></td>
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<tr>
<td>IO Power (pJ/bit)</td>
<td>IO: 0.9pJ/bit @1.2V (3mm channel, with DBI)</td>
<td>IO: 0.5pJ/bit, @0.4V (3mm Channel, with DBI)</td>
<td></td>
</tr>
<tr>
<td>Gbps/mm</td>
<td>730</td>
<td>1150*</td>
<td></td>
</tr>
<tr>
<td>Gbps/mm / pJ/bit</td>
<td>811</td>
<td>2300*</td>
<td></td>
</tr>
<tr>
<td>Gbps/mm2</td>
<td>403</td>
<td>600</td>
<td></td>
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<tr>
<td><strong>Common characteristics</strong></td>
<td></td>
<td></td>
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<tr>
<td>Clocking</td>
<td>Shared clock (Mesochronous)</td>
<td>Shared clock (Mesochronous)</td>
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<tr>
<td>Protection</td>
<td>Parity (per DWORD)</td>
<td>Parity (per DWORD)</td>
<td></td>
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<tr>
<td>Latency (ns) (TX to RX PHY)</td>
<td>4.2 ns</td>
<td>&lt; 4ns</td>
<td></td>
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<tr>
<td>Beach front pitch (um)</td>
<td>55um</td>
<td>TBD*</td>
<td></td>
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<tr>
<td>Connectivity Media / layers</td>
<td>Si Interposer / Fine pitch organic substrate</td>
<td>Si Interposer / Fine pitch organic substrate</td>
<td></td>
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<tr>
<td>PWR/GND bumps</td>
<td>Included</td>
<td>included</td>
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* Based on true data bandwidth and conservative bump pitch. Can be enhanced.
To compare apple-to-apple to other raw BW numbers, adds 12.5% (x 1.125)
** OpenHBI Workstream work item

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Proposed Scope of OpenHBI specification works

> **Layer 0 – Physical Layer**
  >> PHY layer details
  >> Physical connectivity and routing
  >> Flexible Orientation considerations
  >> Redundant wiring for yield management

> **Layer 1 – Link Layer**
  >> Link Layer services
  >> Lane Aggregation
  >> Framing and Alignments
  >> Integrity and Reliability
  >> Bits reordering
  >> Power Management
  >> Support for ODSA TPA I/F

> **Configuration bus – SPI**
  >> Reset, Initialization, Configuration, Link training and activation
ODSA Protocol Stack

Use Cases
- Package Aggregation – Inter package protocols
- Die Disaggregation (Intra-die protocols)
- PHY-Optimized
- Transport Optimized

Txn Layer / Port
- PCIe Txn
- CCI X Txn
- CXL Txn
- PCIe Port
- CCIX Port
- CXL Port
- Custom Protocol (including FIFO) Port
- AXI / ACE-Lite Port (DiPort)
- CHI Port (CCIX)
- Tile Link Port

Link Layer
- PCIe Link Layer
- CXL Link Layer

PIPE I/F
- PIPE Adapter
- Phy Layer
- Substrate
- SerDes (XSR, USR)
- BoW (Phy)
- OpenHBI (Phy)

Legend
- ODSA Standardized Interfaces (no logic)
- ODSA Spec Scope

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Scope of OpenHBI Specifications

Demux version of Link interface definition
Target Milestones & Roadmap

- **Kickoff**: 1Q’2020

- **OpenHBI-2**
  - Frameworks and Requirements draft: 2Q’2020
  - Design-ready draft: 4Q’2020

- **OpenHBI-3**
  - Kickoff 2H’2020
Summary of OpenHBI Proposal and Advantages

> Leverage Proven and Matured standards → much faster Time-to-Deployment
  >> Faster Standardization, Interoperability, Manufacturability, IP and Test ecosystems

> State-of-the-Art Performance and Energy efficiency Roadmap:
  >> Scalable from 100s Gbps to 10s Tbps of true data bandwidth
  >> < 1pJ/bit and roadmap towards ~0.5pJ/bit

> Orientation-Independent
  >> Same and 180° rotated orientation

> Plan to support TPA and mappable to multiple Inter-package or On-die protocols

> Optional Bifurcation support

> Optional backward compatible to support JEDEC HBM on OpenHBI
Call for Interest to OpenHBI Workstream

> Proposed to kickoff OpenHBI Workstream to be a new ODSA Workstream
  >> Xilinx can contribute Layer 0 and 1 OpenHBI proposal as baseline for OHBI development

> “Call for Interest” invitation email to all ODSA members

> If you are interested to contribute or participate, please make sure you are on the ODSA email reflector and reply with:
  1. “Yes, I like to participate in OpenHBI Workstream”
  2. Name and Email address

> Or can send email to me or Bapi to indicate your interest
  >> Kenneth Ma: kma@xilinx.com
  >> Bapi Vinnakota bapi.vinnakota@ocproject.net

> We intend to kickoff in 1Q’2020

THANK YOU FOR YOUR INTERESTS!
Adaptable.
Intelligent.