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Known-Good-Die is at the Heart of a Sustainable Open Chiplet Business Model

NOVEMBER 9-10, 2021

Known-Good-Die is at the Heart of a Sustainable Open Chiplet Business Model

Roberto Rotili, Sr. Director Marketing & GM, Teradyne

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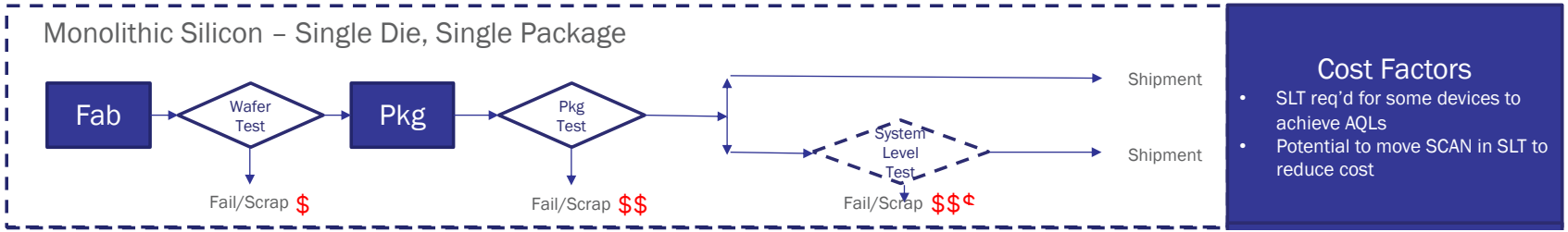
OCP GLOBAL SUMMIT
NOVEMBER 9-10, 2021

Agenda

- Importance of KGD
- Impact of KGD to the business model
- Challenges & Solutions for High & Predictable KGD

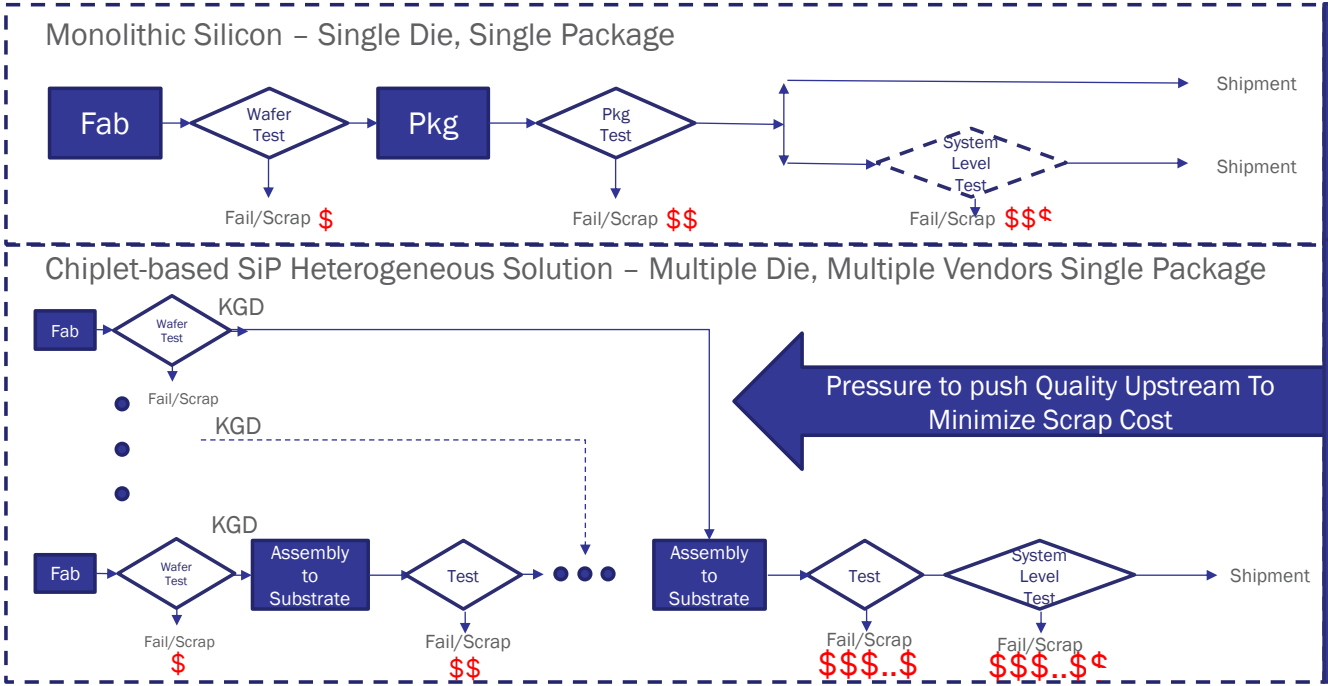
Impact of KGD on Chiplet Work Flow

All About Scrap Cost



Impact of KGD on Chiplet Work Flow

All About Scrap Cost



Cost Factors

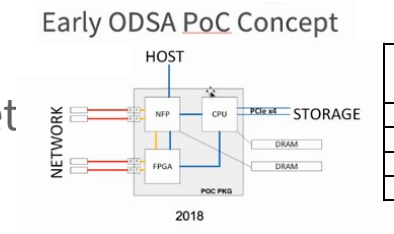
- SLT req'd for some devices to achieve AQLs
- Potential to move SCAN in SLT to reduce cost

Cost Factors

- Rapidly accumulating costs as die are mounted
- No/Limited rework capability (different than PCB assembly)
- **System Level Test Required**
- **Cost of bad SiP, profit of chiplet, and quality liability contracts will drive KGD requirements**

KGD Sensitivity to Chiplet Builder Business Model

- Example Chiplet



Chiplet	Quantity	Chiplet Cost
FPGA	1	$10.00
CPU	1	$20.00
NFP	1	$10.00
DRAM	2	$4.00

- High Level Chiplet-Builder Financial Summary

Builder	Value
Negotiated Chiplet Yield (KGD)	98%
Number of Chiplets in SiP	5
Total SiP Yield	90.4% *does not include assembly yield loss
Self Incurred Scrap Cost	$4.61
SiP Cost	$48
SiP Price	$96
SiP Margin (no scrap)	50.0%
SiP Margin (w/ scrap)	45.2%
Scrap Cost Margin Impact	4.8%

Per SiP, the builder-incurred scrap cost is -$4.60 (4.8% margin impact)

-1% change of KGD yield has a -2.5% impact on CM% for this scenario

An additional Chiplet reduces margin by -1%

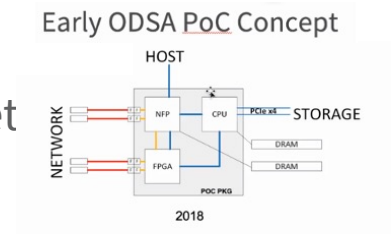
KGD Sensitivity to Chiplet Builder Business Model

- If you are wearing the “Builder” hat then:
  - KGD should be as high & predictable as possible
  - Clause in contract to make **Chiplet Provider responsible for scrap cost**
  - Provide as many of the Chiplets yourself to reduce scrap cost (scrap cost = COGS ≠ASP)
  - Balance “right” number of Chiplets so that you maximize the overall SiP yield

- Let’s explore KGD Sensitivity to Chiplet-Provider Business model with a **contractual obligation to pay for scrap cost for a yield excursion**.

KGD Sensitivity to Chiplet Provider Business Model

- Example Chiplet



- High Level Chiplet-Provider Financial Summary

				Not Including Scrap					Including Scrap Cost	
Chiplet	Quantity	Chiplet ASP	Chiplet Cost	Chiplet Margin $	Chiplet Margin %	Actual Yield	Negotiated Yield	Chiplet Based-SiP Scrap Cost	Chiplet Margin $	Chiplet Margin %
FPGA	1	$10.00	$2.50	$7.50	75%	96%	98%	$48	$6.54	65%
CPU	1	$20.00	$3.00	$17.00	85%	96%	98%	$48	$16.04	80%
NFP	1	$10.00	$2.50	$7.50	75%	96%	98%	$48	$6.54	65%
DRAM	2	$4.00	$1.40	$2.60	65%	96%	98%	$48	$1.64	41%

2% yield excursion leads to:

-10% margin loss

-5% margin loss
CPU: -2.5% margin loss per 1% delta in actual vs. negotiated yield

-24% margin loss
DRAM: -12% margin loss per 1% delta in actual vs. negotiated yield

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KGD Sensitivity to Chiplet Provider Business Model

- If you are wearing the “Chiplet Provider” hat then:
  - KGD should be as high and predictable as possible
  - Quality contract that requires the “Provider” to pay for scrap costs is very risky (unless you can have predictable and high KDG)
  - If such a clause exists, then the bias will be for the Chiplet providers to sell high value Chiplet in the SiP
  - Sell untested wafers (instead of KGD) to Chiplet Builders and put test/risk on Builder’s books.

Key to Business Model is a High/Stable KGD

Easier Said than Done

- Chiplet test coverage significantly lower than a monolithic package part at the point when you deliver it to your customer:

	Wafer Sort	Final Test	Hot/Cold Testing	Interface Testing	System Level Test	Burn In
Monolithic Package	Yes	Yes	Yes	Yes	Yes	Yes
Single Chiplet	Yes	No	No	No - Die-to-Die interfaces lack signal strength to drive to-and-from ATE. Rely on BIST for D2D testing.	No – and more reliant on interaction with other chiplets.	No

Key to Business Model is a High/Stable KGD
What Can Be Done

- Ways to improve KGD:
  - Add design redundancy to chip features that exhibit high fail rate so can repair-on-the-fly
    - add extra processing cores, extra D2D interface wires, extra memory banks, etc.
  - Test of sub-assembly of chiplets to minimize scrap cost at final-assembly
  - Pre-combinations of die (sub assemblies) from single supplier to reduce the multiplicative impact of yield

Call to Action

- Provide feedback (or share your own) on Chiplet Provider/Builder KGD Business Model on ODSA Google Drive
- What are other ways to have a high and predictable KGD
- What are clauses in quality contracts that exist today that might address KGD and scrap cost to promote an open Chiplet model

Thank you!

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