OPEN POSSIBILITIES.

Known-Good-Die is at the Heart of a Sustainable Open Chiplet Business Model
Known-Good-Die is at the Heart of a Sustainable Open Chiplet Business Model

Roberto Rotili, Sr. Director Marketing & GM, Teradyne
Agenda

• Importance of KGD

• Impact of KGD to the business model

• Challenges & Solutions for High & Predictable KGD
Impact of KGD on Chiplet Work Flow

All About Scrap Cost

Monolithic Silicon – Single Die, Single Package

Cost Factors
- SLT req’d for some devices to achieve AQLs
- Potential to move SCAN in SLT to reduce cost
Impact of KGD on Chiplet Work Flow

All About Scrap Cost

Monolithic Silicon – Single Die, Single Package

Cost Factors
- SLT req’d for some devices to achieve AQLs
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Chiplet-based SiP Heterogeneous Solution – Multiple Die, Multiple Vendors Single Package

Cost Factors
- Rapidly accumulating costs as die are mounted
- No/Limited rework capability (different than PCB assembly)
- System Level Test Required
- Cost of bad SiP, profit of chiplet, and quality liability contracts will drive KGD requirements

Pressure to push Quality Upstream To Minimize Scrap Cost
KGD Sensitivity to Chiplet Builder Business Model

- Example Chiplet

- High Level Chiplet-Builder Financial Summary

<table>
<thead>
<tr>
<th>Builder</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Negotiated Chiplet Yield (KGD)</td>
<td>98%</td>
</tr>
<tr>
<td>Number of Chiplets in SiP</td>
<td>5</td>
</tr>
<tr>
<td>Total SiP Yield</td>
<td>90.4% *does not include assembly yield loss</td>
</tr>
<tr>
<td>Self Incurred Scrap Cost</td>
<td>$4.61</td>
</tr>
<tr>
<td>SiP Cost</td>
<td>$48</td>
</tr>
<tr>
<td>SiP Price</td>
<td>$96</td>
</tr>
<tr>
<td>SiP Margin (no scrap)</td>
<td>50.0%</td>
</tr>
<tr>
<td>SiP Margin (w/ scrap)</td>
<td>45.2%</td>
</tr>
<tr>
<td>Scrap Cost Margin Impact</td>
<td>4.8%</td>
</tr>
</tbody>
</table>

Per SiP, the builder-incurred scrap cost is -$4.60 (4.8% margin impact)

-1% change of KGD yield has a -2.5% impact on CM% for this scenario

An additional Chiplet reduces margin by -1%
KGD Sensitivity to Chiplet Builder Business Model

• If you are wearing the “Builder” hat then:
  • KGD should be as high & predictable as possible
  • Clause in contract to make Chiplet Provider responsible for scrap cost
  • Provide as many of the Chiplets yourself to reduce scrap cost
    (scrap cost = COGS ≠ ASP)
  • Balance “right” number of Chiplets so that you maximize the overall SiP yield

• Let’s explore KGD Sensitivity to Chiplet-Provider Business model with a contractual obligation to pay for scrap cost for a yield excursion.
KGD Sensitivity to Chiplet Provider Business Model

- Example Chiplet
- High Level Chiplet-Provider Financial Summary

<table>
<thead>
<tr>
<th>Chiplet</th>
<th>Quantity</th>
<th>Chiplet ASP</th>
<th>Chiplet Cost</th>
<th>Chiplet Margin $</th>
<th>Chiplet Margin %</th>
<th>Actual Yield</th>
<th>Negotiated Yield</th>
<th>Chiplet Based-SiP Scrap Cost</th>
<th>Chiplet Margin $</th>
<th>Chiplet Margin %</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA</td>
<td>1</td>
<td>$10.00</td>
<td>$3.00</td>
<td>$7.50</td>
<td>75%</td>
<td>96%</td>
<td>98%</td>
<td>$48</td>
<td>$6.54</td>
<td>65%</td>
</tr>
<tr>
<td>CPU</td>
<td>1</td>
<td>$20.00</td>
<td>$3.00</td>
<td>$17.00</td>
<td>85%</td>
<td>96%</td>
<td>98%</td>
<td>$48</td>
<td>$16.04</td>
<td>80%</td>
</tr>
<tr>
<td>NFP</td>
<td>1</td>
<td>$10.00</td>
<td>$2.50</td>
<td>$7.50</td>
<td>75%</td>
<td>96%</td>
<td>98%</td>
<td>$48</td>
<td>$6.54</td>
<td>65%</td>
</tr>
<tr>
<td>DRAM</td>
<td>2</td>
<td>$4.00</td>
<td>$1.40</td>
<td>$2.60</td>
<td>65%</td>
<td>96%</td>
<td>98%</td>
<td>$48</td>
<td>$1.64</td>
<td>41%</td>
</tr>
</tbody>
</table>

2% yield excursion leads to:
- **-10%** margin loss
- **-5%** margin loss
- **-24%** margin loss

CPU: **-2.5%** margin loss per 1% delta in actual vs. negotiated yield

DRAM: **-12%** margin loss per 1% delta in actual vs. negotiated yield
KGD Sensitivity to Chiplet Provider Business Model

- If you are wearing the “Chiplet Provider” hat then:
  - KGD should be as high and predictable as possible
  - Quality contract that requires the “Provider” to pay for scrap costs is very risky (unless you can have predictable and high KGD)
  - If such a clause exists, then the bias will be for the Chiplet providers to sell high value Chiplet in the SiP
  - Sell untested wafers (instead of KGD) to Chiplet Builders and put test/risk on Builder’s books.
Key to Business Model is a High/Stable KGD

Easier Said than Done

- Chiplet test coverage significantly lower than a monolithic package part at the point when you deliver it to your customer:

<table>
<thead>
<tr>
<th></th>
<th>Wafer Sort</th>
<th>Final Test</th>
<th>Hot/Cold Testing</th>
<th>Interface Testing</th>
<th>System Level Test</th>
<th>Burn In</th>
</tr>
</thead>
<tbody>
<tr>
<td>Monolithic Package</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Single Chiplet</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No - Die-to-Die interfaces lack signal strength to drive to-and-from ATE. Rely on BIST for D2D testing.</td>
<td>No – and more reliant on interaction with other chiplets.</td>
<td>No</td>
</tr>
</tbody>
</table>
Key to Business Model is a High/Stable KGD

What Can Be Done

• Ways to improve KGD:
  • Add design redundancy to chip features that exhibit high fail rate so can repair-on-the-fly
    • add extra processing cores, extra D2D interface wires, extra memory banks, etc.
  • Test of sub-assembly of chiplets to minimize scrap cost at final-assembly
  • Pre-combinations of die (sub assemblies) from single supplier to reduce the multiplicative impact of yield
Call to Action

- Provide feedback (or share your own) on Chiplet Provider/Builder KGD Business Model on ODSA Google Drive
- What are other ways to have a high and predictable KGD
- What are clauses in quality contracts that exist today that might address KGD and scrap cost to promote an open Chiplet model
Thank you!