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Synopsys Die-to-Die Test

Test Requirements and Synopsys SHS Support

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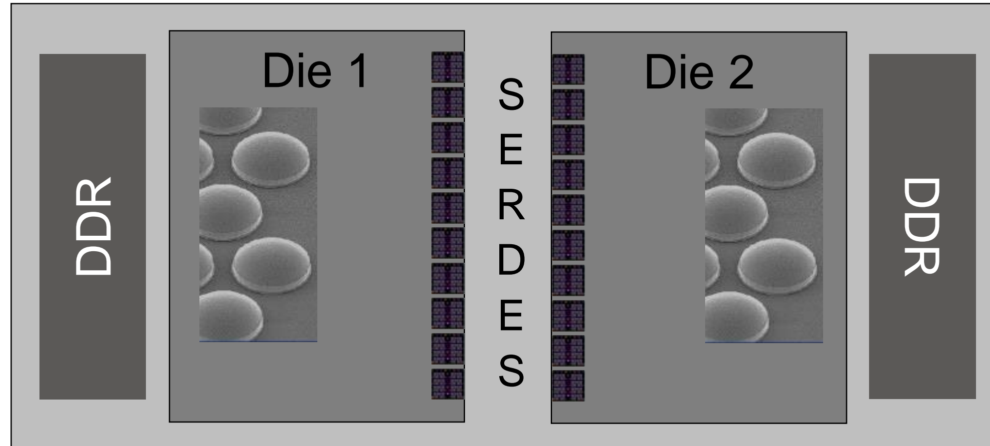
Die-to-Die SerDes PHY Solution

USR/XSR SerDes



- Higher bandwidth, lower complexity & cost
  - 1.8Tbps/mm (56/112Gbps * 16 lanes)
  - **Organic substrate** (low loss), ~50mm reach
  - Standard bumps: 130µm to 170µm
- Higher latency & power
  - Higher latency (if with FEC)
  - 1 pJ/bit

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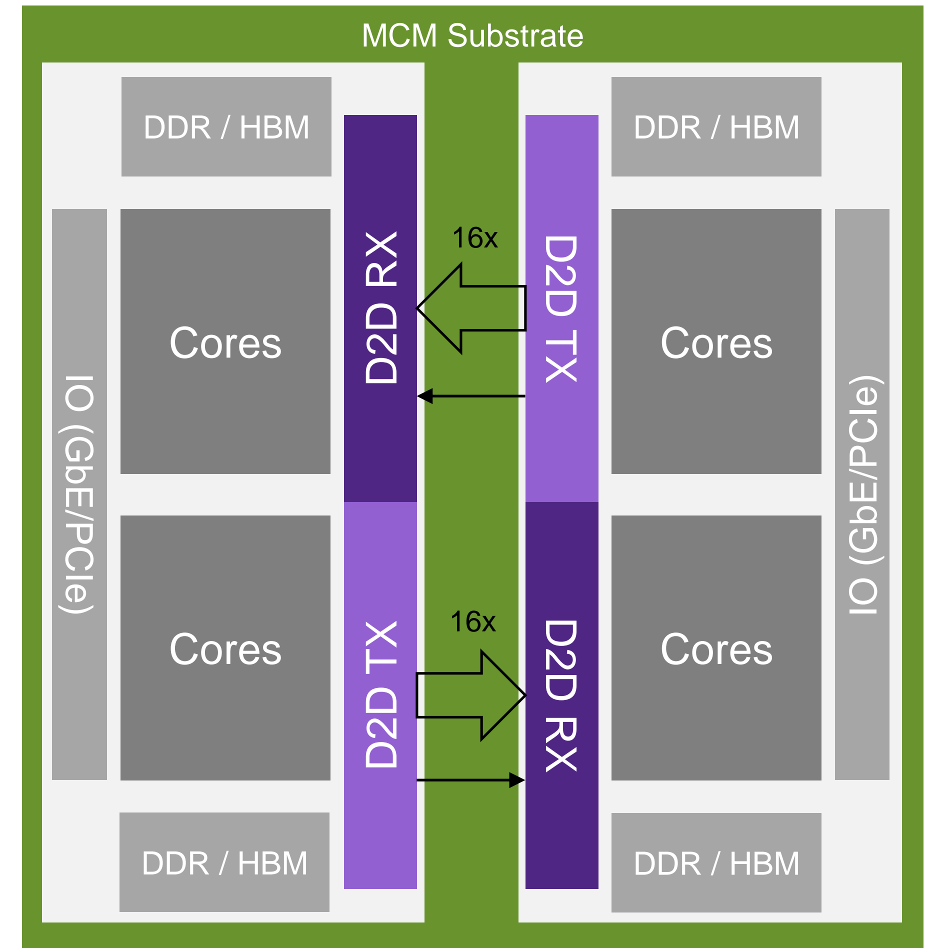
DesignWare Die-to-Die SerDes PHY

Up to 112Gbps per lane for High Density USR and XSR links in MCMs

- Multiple technology nodes
  - ~1.8Tbps/mm aggregate unidirectional BW
  - Low power die-to-die connectivity (1pJ/bit)
  - Low latency and low BER
  - Up to 50mm reach for die-to-die connects in MCM
- 16-lane unidirectional TX and RX macros
  - PAM4 or NRZ encoding and wide data rate range for maximum flexibility
  - Support for C4 Bumps or optional Cu-pillar & µ-Bumps
  - Internal calibration and built-in loopback and diagnostic features for robustness and testability
  - Protocol agnostic Raw-PCS based parallel-side interface
- Complies with OIF-CEI 56G and 112G electrical specs for USR and XSR links



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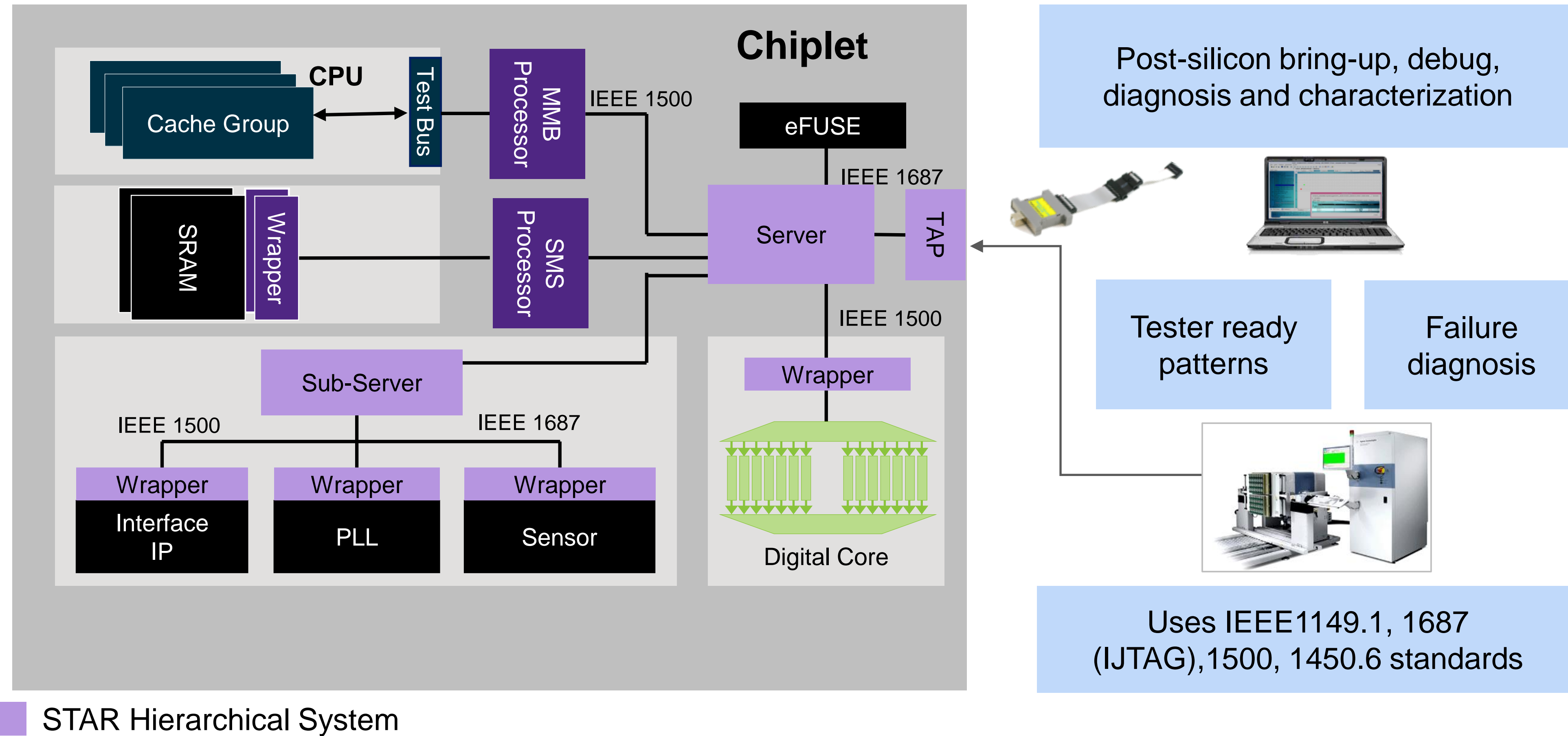
SoC Level Hierarchical Test Management – DW SHS



STAR Hierarchical System

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Die-to-Die Testing
Some High-Level Requirements

- Intra Die Test Management
  - For pre-assembly KGD test
    - Probe access may be limited due to micro bumps
  - Post-assembly to test dies and interconnect between dies
    - Test access needs to be plug-and-play between dies
    - Access from package pins via first/bottom die, then die-to-die via adjacent/next dies in the stack/chiplet assembly
    - Both serial test access and high-bandwidth test access (parallel or SERDES) are needed
  - Supported by IEEE test standards: 1149.1 (JTAG), 1149.10 (HSTAP), 1500/1687 (Core/IP) and 1838 (3D Test)
- Inter Die Test for post-assembly
  - Test through micro bumps or TSV interconnects
  - Static testing for shorts and opens, similar to boundary scan testing
  - At-speed testing is needed, for example far-end loopbacks using PHY protocols, or registered loopbacks
- PHY DFT
  - Die-to-die test support must be included with the DFT of the PHYs that are used for die-to-die communication
  - Micro bumps for die-to-die DFT connection must be part of the standard micro bump layout of the PHYs
  - PHYs must provide die-to-die access in conjunction with the SoC DFT in the dies

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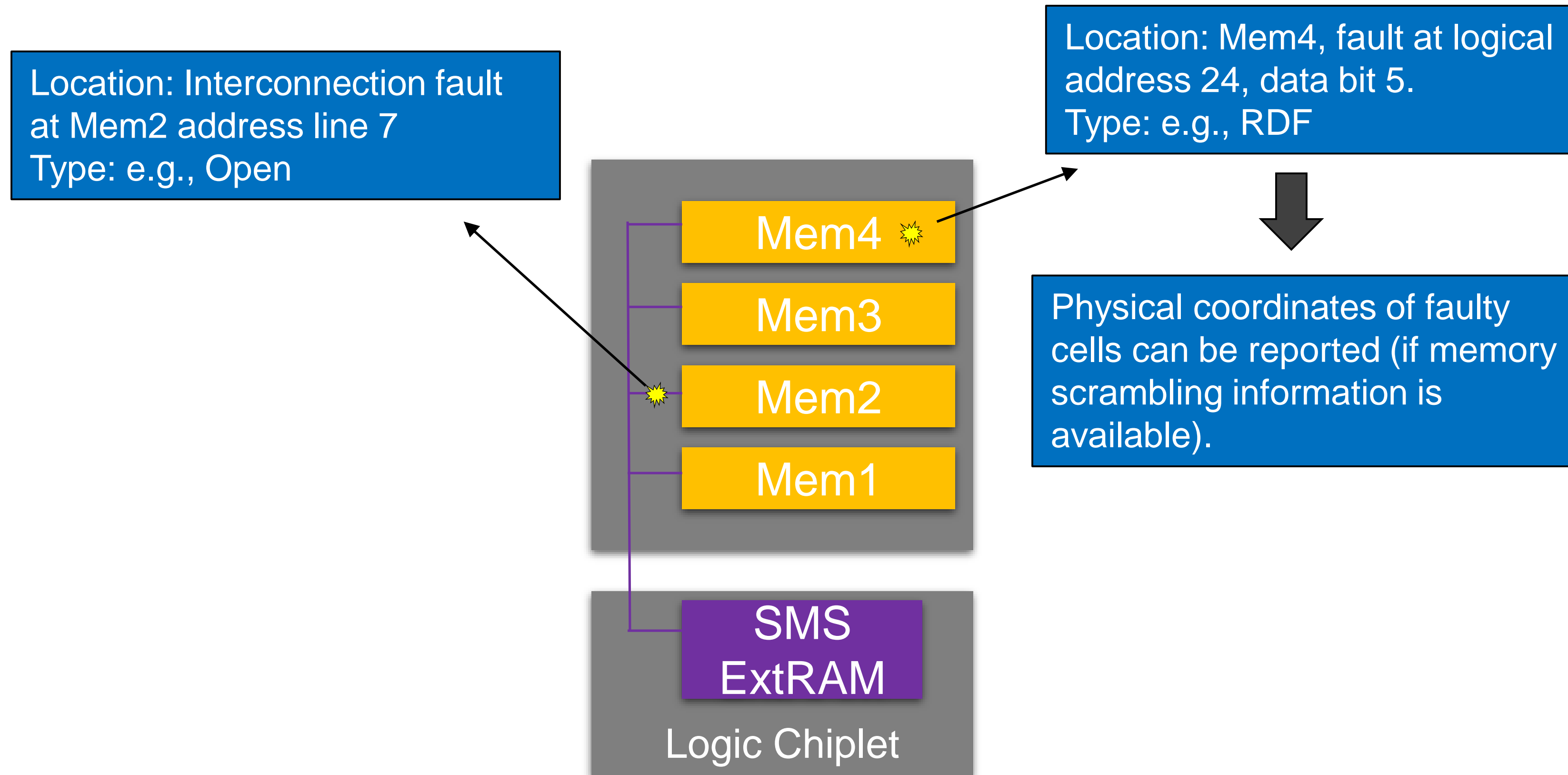
External Memory At-Speed Test & Diagnosis Through PHY



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External Memory Test & Diagnosis

Memory and logic dies: DDR or HBM 2

Test individual die before packaging

External DRAM Memory

test external memory and interconnects

SMS EXTRAM

TAP

SMS Ext-RAM

IEEE 1149.1 access

Digital core compression

SHS – PHY BIST, IEEE 1500

Use TAP to run tests after packaging

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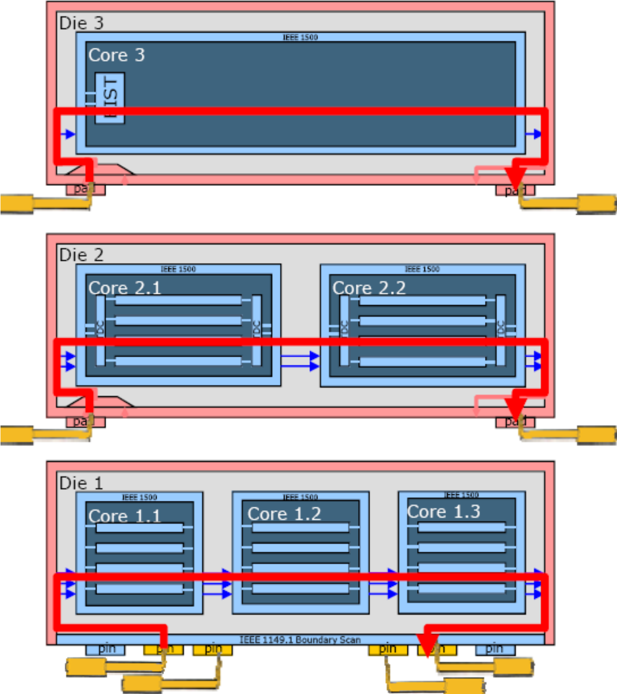
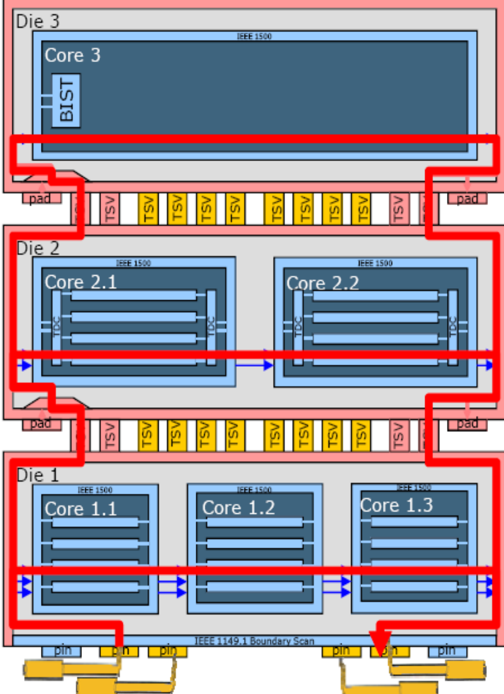
Access at ALL the dies

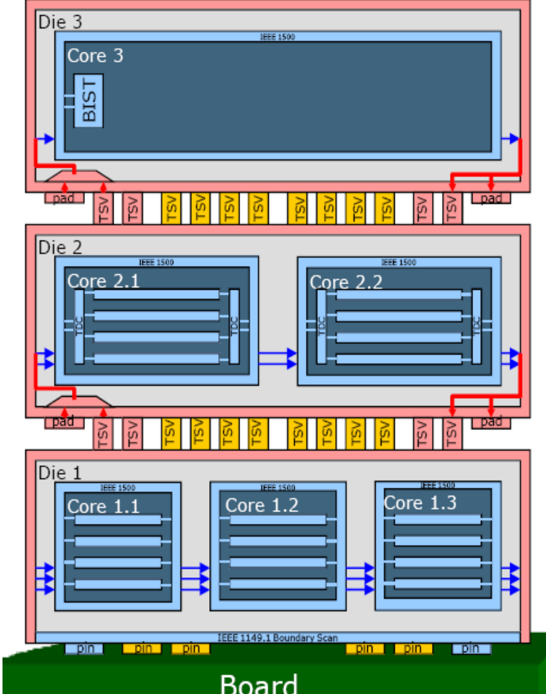
Inter Die Test



Intra Die Test



Package Test



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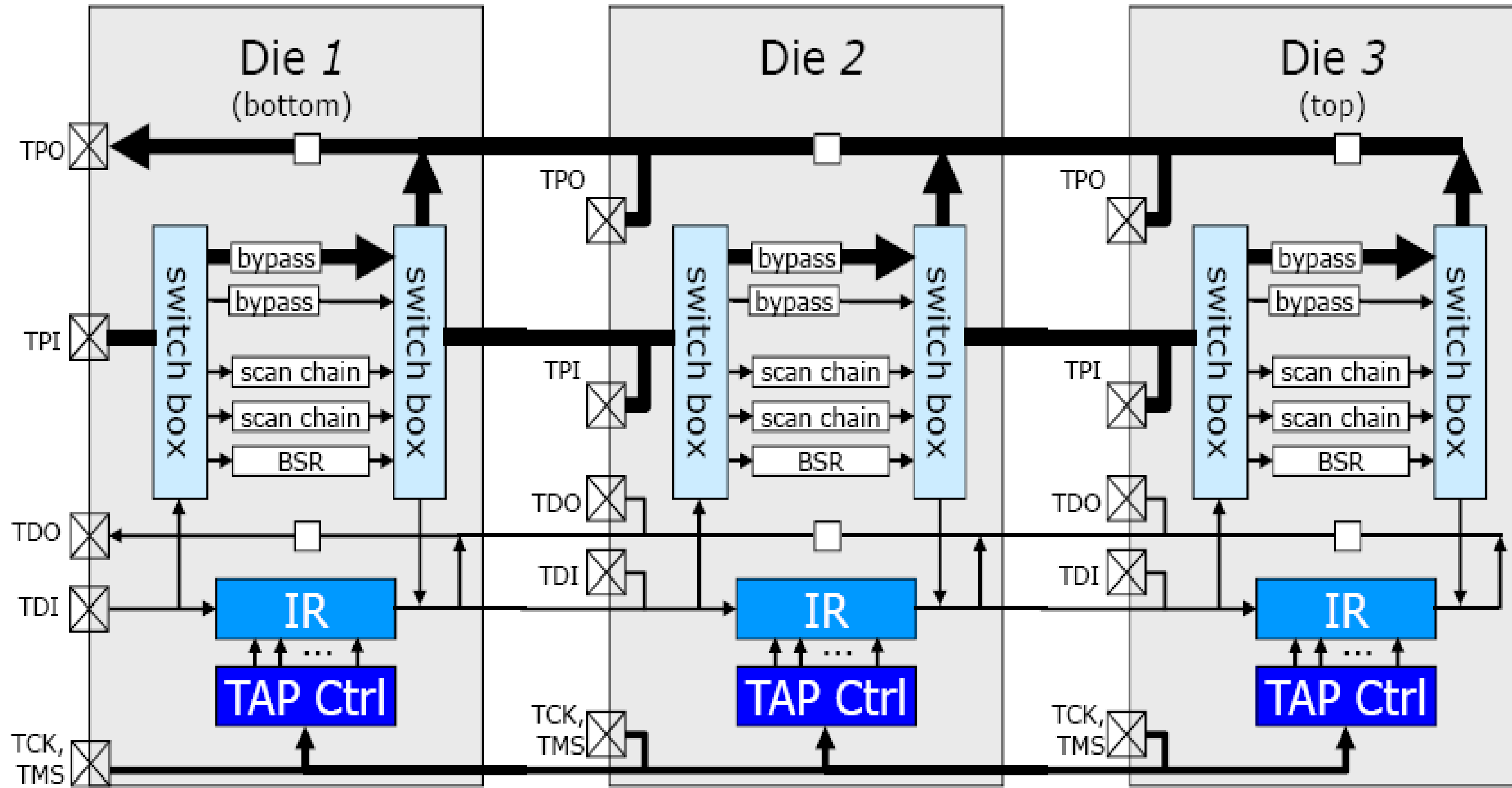
Example Solution



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IEEE 1838 Serial Test Access Ports

- PTAP
  - Primary Test Access Port
  - TCK, TRSTN, TMS, TDI, TDO
- PTAP Controller
  - TAP FSM connected to the PTAP signals
- STAP
  - Secondary Test Access Port
  - TCK_Sn, TRSTN_Sn, TMS_Sn, TDI_Sn, TDO_Sn
  - Connects to PTAP on next die
  - Controlled by PTAP controller and associated control and configuration logic

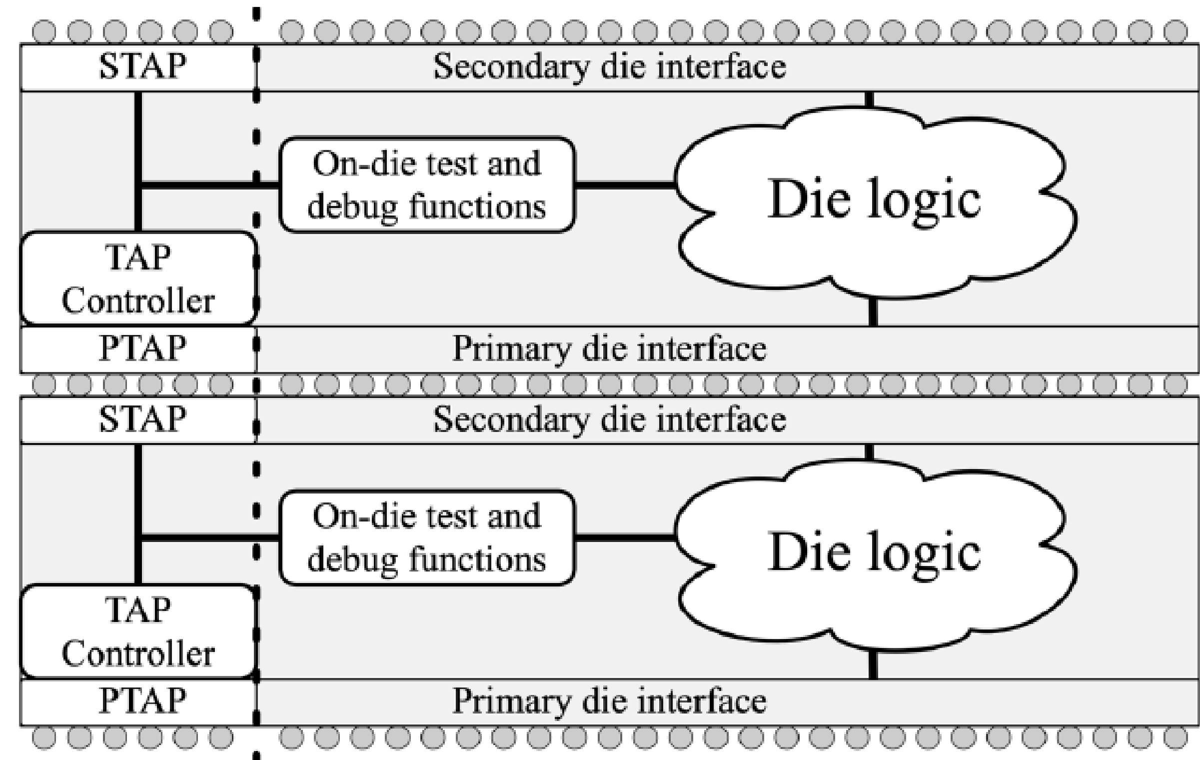

Figure 5: Example of a stack comprised of two semiconductor dies.

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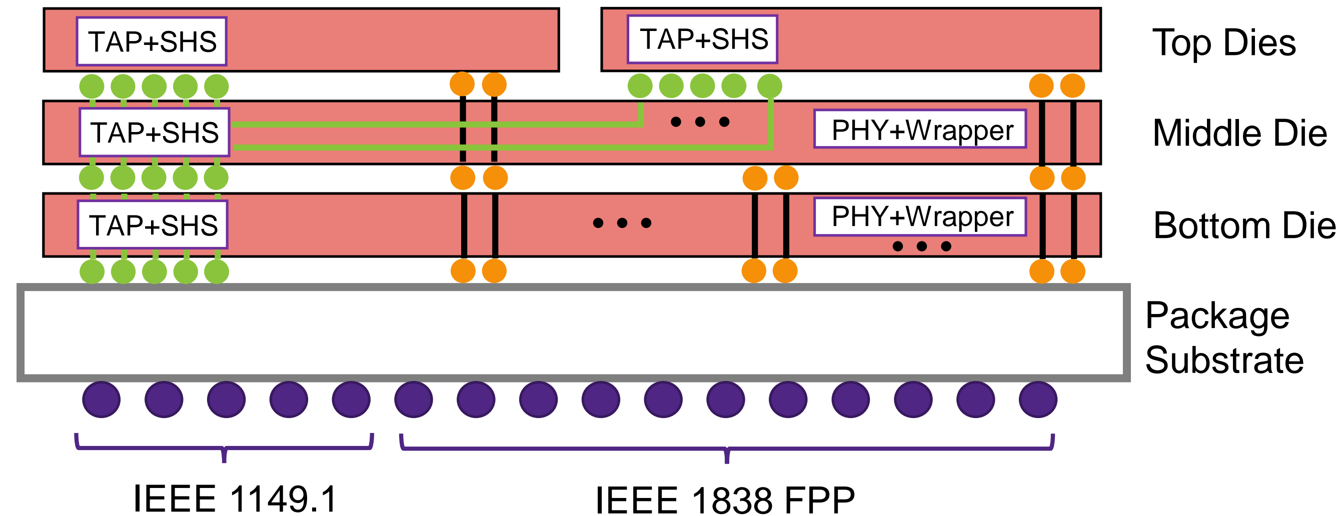
Example of IEEE 1838: SHS for Multi-Die Test



- The Synopsys SHS architecture can support multiple die configurations
  - Green TSVs and micro bumps are SHS network for IEEE 1838 standard's plug-and-play connections
  - SHS supports multiple 1838 die connections, as shown on the middle die, for access to the two top dies
- SHS PHY wrapper supports standard DFT (e.g., IEEE 1500 and 1838) for interconnect test and die-to-die access
- 1838 FPP can be shared with package pins and SHS PHY wrappers distribute FPP between dies, black TSVs and orange micro bumps

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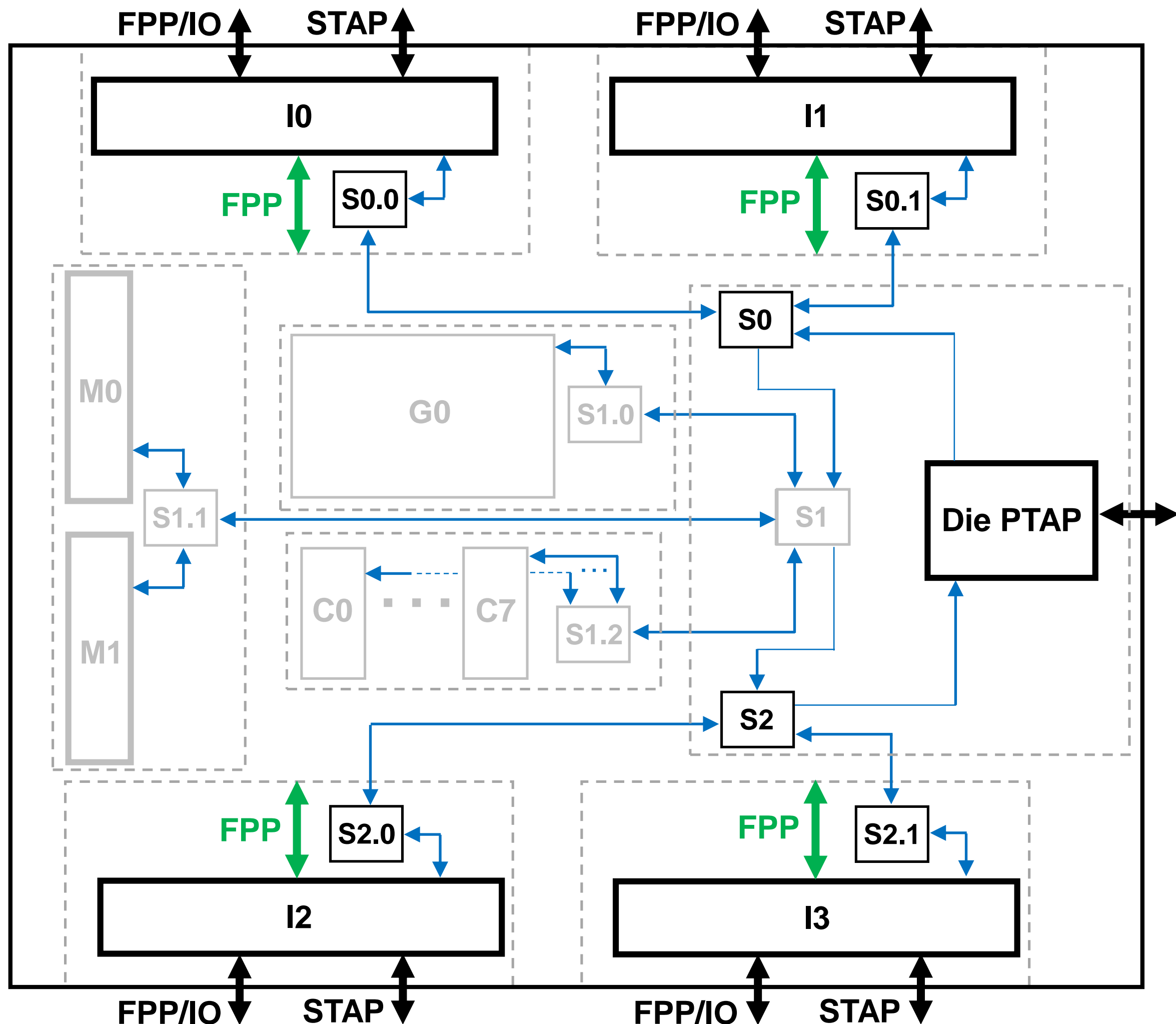
IEEE 1838 Standard Access to Multiple Dies

Support though SHS Hierarchical Network Management



- IEEE 1838 standard has three major components
  1. Serial Test Port Architecture
     - 1149.1 Primary TAP (PTAP) and Secondary TAP (STAPs) on each die, for die-to-die access
  2. Die Wrapper Register (DWR)
     - PHY wrapper register for interconnect testing between die
  3. Optional Flexible Parallel Port (FPP)
     - Provides parallel test access to the dies from the package pins
- Die shown with four die-to-die PHYs (I0 through I3)
  - SHS hierarchical server network provides both die test and 1838 die-to-die access
  - PTAP is the SoC level TAP controller
  - SHS servers (S.n) in hierarchical network provide STAP access/control via PTAP and each die-to-die PHY
  - STAPs connect to associated PTAPs on adjacent/next dies
  - FPP is shared with die IO and distributed to next/adjacent dies via the PHYs

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Thank You