Die-to-Die Interface for Multi-Chiplet AI Systems

Sid Sheth & Wen-Sin Liew
Our team: Leading technologists and proven value creators

- 20+ years of silicon / systems leadership
- Delivered > 100M chips
- Generated > 1B$ revenue in the cloud & enterprise
- 90+ persons; 30% PhDs
(Silicon Valley, Sydney, and Bangalore)

$51M raised from top tier financial and strategic VCs
Multi-Chiplet AI Compute for Scale-Out Inference

- 8-chiplet AI system on a common substrate
- All chiplets are connected through bi-directional 512Gbps BoW D2D interface
- Reason for using BoW
  - Low energy (pJ/bit), high beachfront BW and support cost-efficient organic substrate
  - Interoperability enables heterogenous integration with chiplets from different parties
d-Matrix BoW Interface Specifications

- **Process node**: TSMC 6nm technology
- **Electrical**: One pair of differential clock (forwarded clock), 16-bit single-ended (16Gbps/wire) data bus with AUX and FEC
- **Physical**: estimated area of 0.8mm²
- **Energy efficiency**: < 0.5pJ/bit
- **Beachfront bandwidth**: 0.19Tbps/mm (single-stack design), up to 0.75Tbps/mm (4-stack design)
- **BER**: < 1e-15
- **Silicon availability**: Now
Jayhawk Silicon Success

Jayhawk platform with 2-die MCM and varying trace lengths (3, 15, 25mm)

✓ Successfully achieved initial chip bring up milestone in record time – 8 days!
✓ Industry’s first BoW based silicon on organic substrate (TSMC 6nm process)
Die-to-Die Successful Bring-Up

- Error-free PRBS9/PRBS31 transmission through all 3, 15, 25mm channels!
- 2-D aggregated and per-lane eye scan show excellent eye openings

Aggregated Eye (256Gbps total, PRBS31, 25mm)

16-Lane Eye (16Gbps/lane, PRBS31, 25mm)
Die-to-Die Successful Bring-Up

- Excellent horizontal and vertical eye openings with BER < 1e-15

**Aggregated Bathtub (256Gbps total, PRBS31)**

- 0.64UI @ BER=1e-15
- 163mV @ BER=1e-15
Die-to-Die Key Summary

- 16Gbps/lane, TX=RX=50-Ohm, 0.75V supply and room temperature.
- Ultra-low-energy operation with lower TX driver supply and higher RX termination.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Unit</th>
<th>Remarks</th>
<th>TT</th>
<th>TT **</th>
<th>SS</th>
<th>FF</th>
<th>SF</th>
<th>FS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy/bit</td>
<td>pJ/bit</td>
<td>PHY only</td>
<td>0.464</td>
<td>0.349</td>
<td>0.460</td>
<td>0.496</td>
<td>0.470</td>
<td>0.470</td>
</tr>
<tr>
<td>Horizontal eye opening @ BER &lt; 1e-15</td>
<td>UI</td>
<td>(aggregated 256Gbps)</td>
<td>0.64</td>
<td>0.59</td>
<td>0.62</td>
<td>0.64</td>
<td>0.68</td>
<td>0.65</td>
</tr>
<tr>
<td></td>
<td></td>
<td>25mm channel</td>
<td>0.64</td>
<td>0.59</td>
<td>0.62</td>
<td>0.64</td>
<td>0.68</td>
<td>0.65</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15mm channel</td>
<td>0.66</td>
<td>0.57</td>
<td>0.63</td>
<td>0.57</td>
<td>0.69</td>
<td>0.64</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3mm channel</td>
<td>0.68</td>
<td>0.47</td>
<td>0.56</td>
<td>0.58</td>
<td>0.57</td>
<td>0.61</td>
</tr>
<tr>
<td>Vertical eye opening @ BER &lt; 1e-15</td>
<td>mV</td>
<td>25mm channel</td>
<td>163</td>
<td>141</td>
<td>175</td>
<td>190</td>
<td>172</td>
<td>155</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15mm channel</td>
<td>188</td>
<td>164</td>
<td>185</td>
<td>175</td>
<td>198</td>
<td>190</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3mm channel</td>
<td>212</td>
<td>253</td>
<td>215</td>
<td>200</td>
<td>204</td>
<td>210</td>
</tr>
</tbody>
</table>

** TX Driver=0.6V, TX=50-ohm, RX=150-ohm
Thank You

To the Success of Chiplets