

# January 24 - 26, 2023 DoubleTree by Hilton San Jose ChipletSummit.com



# Die-to-Die Interface for Multi-Chiplet AI Systems

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## d-Matrix: Company Snapshot



Sid Sheth Founder | CEO



Sudeep Bhoja Founder | CTO

### Our team: Leading technologists and proven value creators

- 20+ years of silicon / systems leadership
- Delivered > 100M chips
- Generated > 1B\$ revenue in the cloud & enterprise
- 90+ persons; 30% PhDs (Silicon Valley, Sydney, and Bangalore)

\$51M raised from top tier financial and strategic VCs













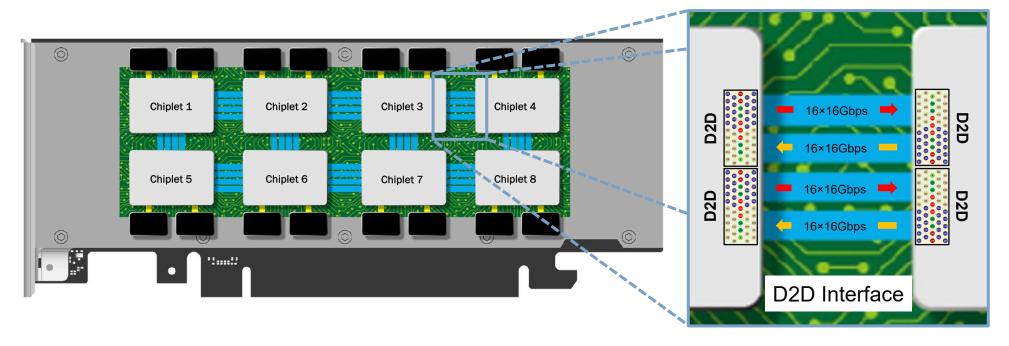






## Multi-Chiplet Al Compute for Scale-Out Inference

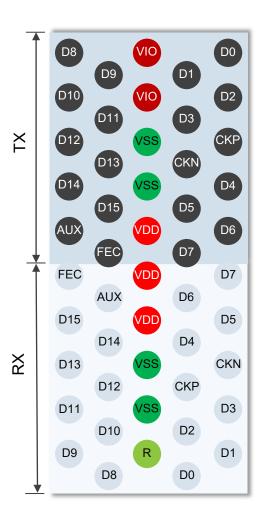
- 8-chiplet AI system on a common substrate
- All chiplets are connected through bi-directional 512Gbps BoW D2D interface
- Reason for using BoW
  - ✓ Low energy (pJ/bit), high beachfront BW and support cost-efficient organic substrate
  - ✓ Interoperability enables heterogenous integration with chiplets from different parties





## d-Matrix BoW Interface Specifications





- Process node: TSMC 6nm technology
- Electrical: One pair of differential clock (forwarded clock), 16-bit single-ended (16Gbps/wire) data bus with AUX and FEC
- Physical: estimated area of 0.8mm<sup>2</sup>
- Energy efficiency: < 0.5pJ/bit</li>
- Beachfront bandwidth:
  0.19Tbps/mm (single-stack design),
  up to 0.75Tbps/mm (4-stack design)
- **BER**: < 1e-15
- Silicon availability: Now





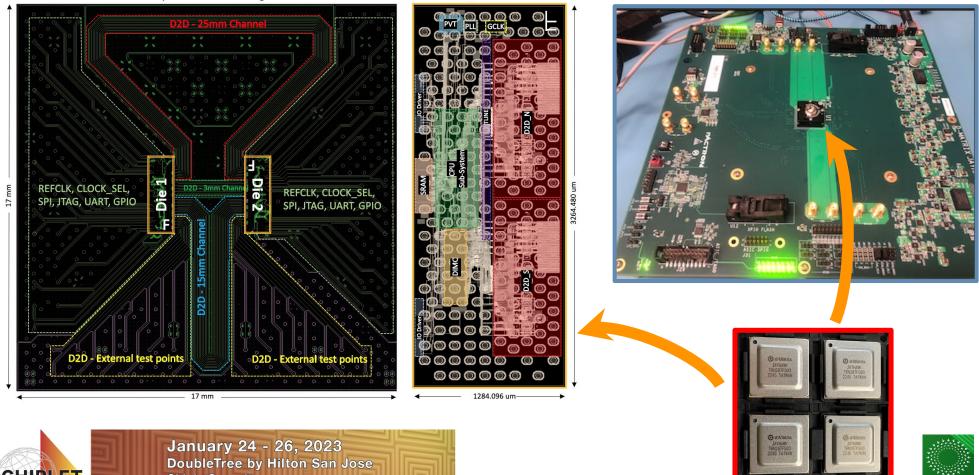
## Jayhawk Silicon Success

JayHawk Substrate Design

#### Jayhawk platform with 2-die MCM and varying trace lengths (3, 15, 25mm)

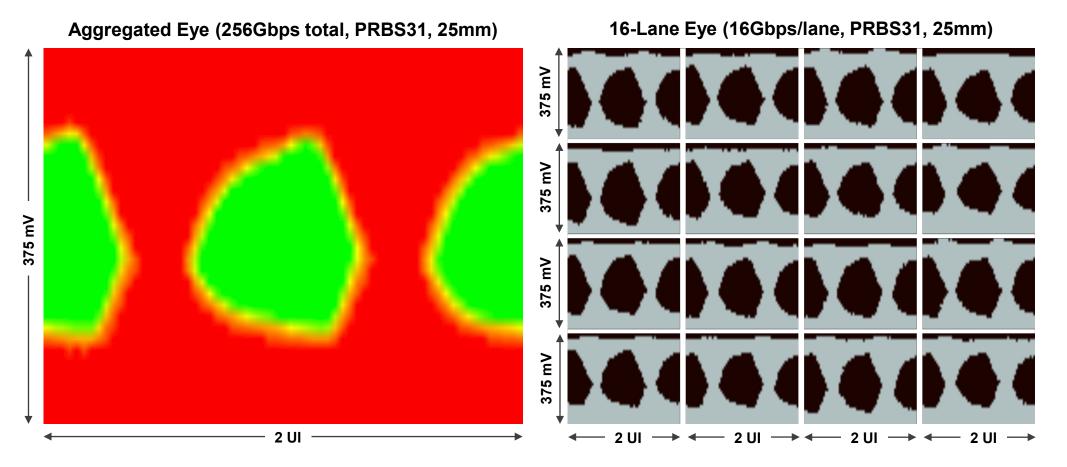
- Successfully achieved initial chip bring up milestone in record time 8 days!
- Industry's first BoW based silicon on organic substrate (TSMC 6nm process)

JavHawk Silicon



## Die-to-Die Successful Bring-Up

- ✓ Error-free PRBS9/PRBS31 transmission through all 3, 15, 25mm channels!
- ✓ 2-D aggregated and per-lane eye scan show excellent eye openings



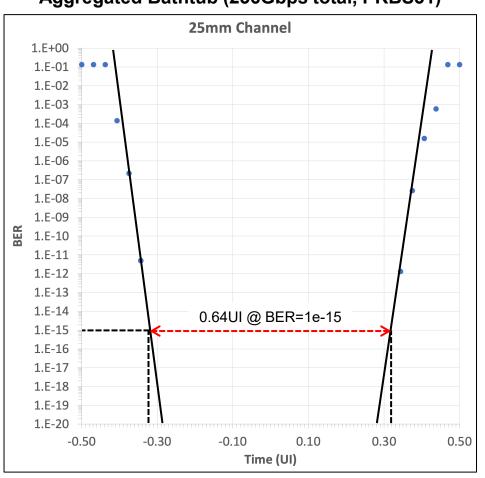




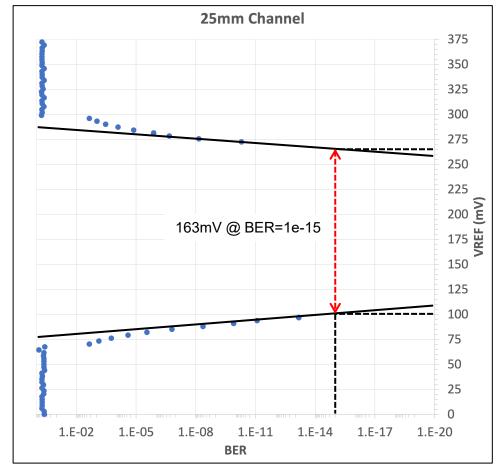
## Die-to-Die Successful Bring-Up

✓ Excellent horizontal and vertical eye openings with BER < 1e-15</p>

#### Aggregated Bathtub (256Gbps total, PRBS31)



#### Aggregated Bathtub (256Gbps total, PRBS31)







## Die-to-Die Key Summary

- 16Gbps/lane, TX=RX=50-Ohm, 0.75V supply and room temperature.
- Ultra-low-energy operation with lower TX driver supply and higher RX termination.

Parameters	Unit	Remarks	TT	TT **	SS	FF	SF	FS
Energy/bit	pJ/bit	PHY only	0.464	0.349	0.460	0.496	0.470	0.470
Horizontal eye opening @ BER < 1e-15 (aggregated 256Gbps)	UI (62.5ps)	25mm channel	0.64	0.59	0.62	0.64	0.68	0.65
		15mm channel	0.66	0.57	0.63	0.57	0.69	0.64
		3mm channel	0.68	0.47	0.56	0.58	0.57	0.61
Vertical eye opening @ BER < 1e-15 (aggregated 256Gbps)	mV	25mm channel	163	141	175	190	172	155
		15mm channel	188	164	185	175	198	190
		3mm channel	212	253	215	200	204	210

<sup>\*\*</sup> TX Driver=0.6V, TX=50-ohm, RX=150-ohm







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## Thank You



To the Success of Chiplets

