Rajamani Sethuram

DFT Engineer, nVidia Corp.

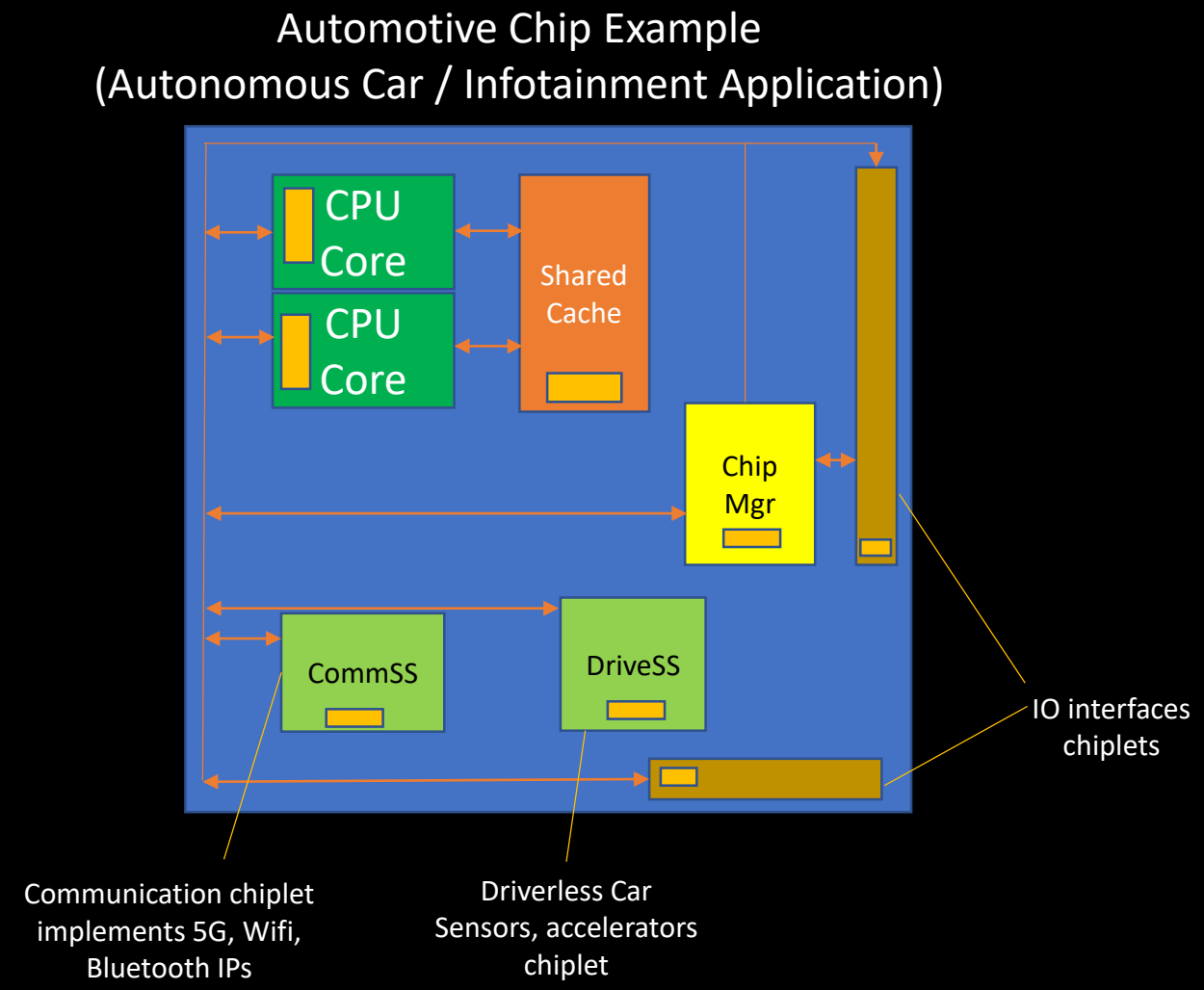
Problems

- Can chiplet Integration standard help
  - Die2Die Testing
  - Test Access Mechanism

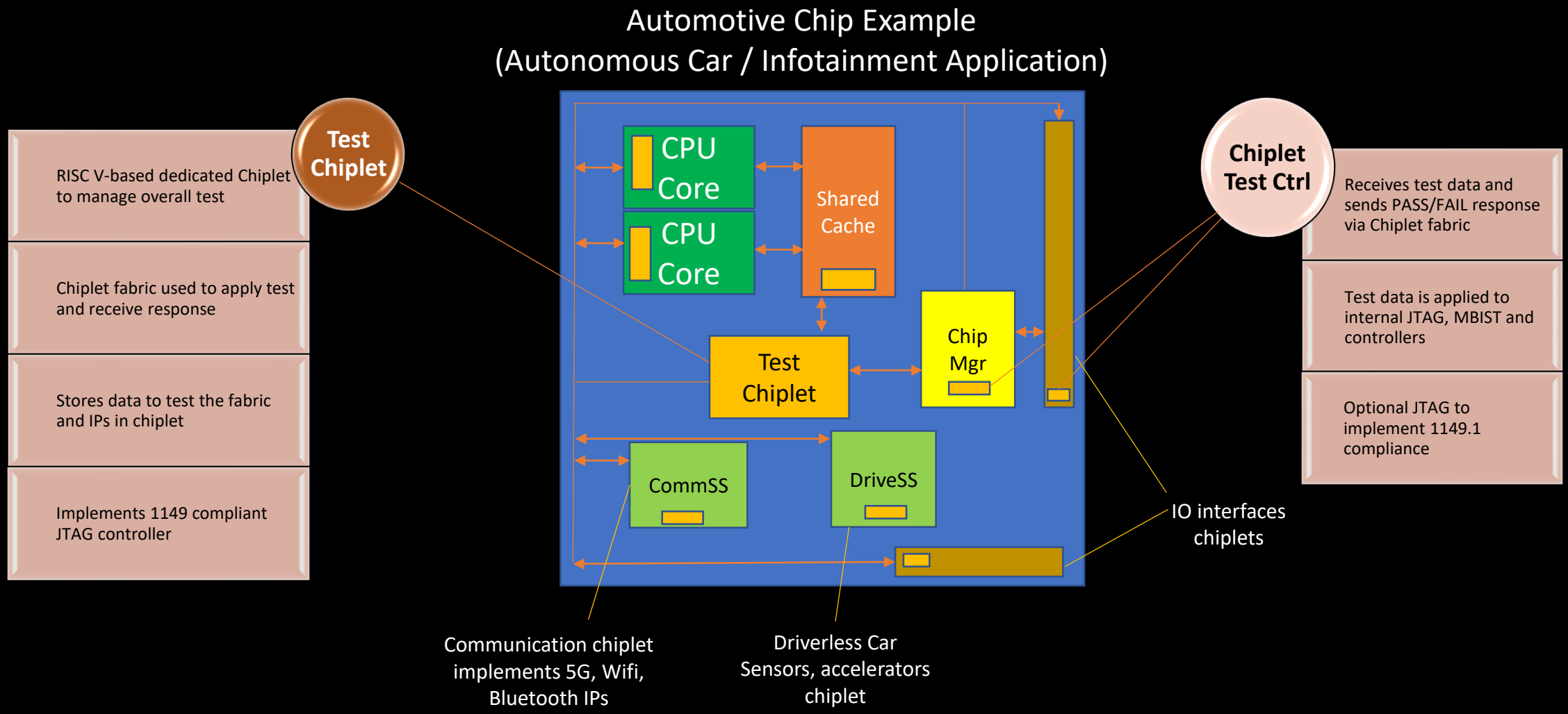
Key Ideas

- Software and Test should co-exist
- Reuse the fabric to also apply test data
  - Long / Serial JTAG chains wrapping around chiplets are not desirable
  - Test and Security Challenges
- Chip integration teams to use system software to run chiplet tests
  - Eases debugging field failures and correlate system test with
  - Helps lower cost and faster TAT

Example Automotive Chip



Proposed Test Arch.



Summary of test solution

- Die-to-Die Testing covered by fabric testing - New
  - Perform sanity read/write transaction to get 100% coverage
  - Test generation support needed from EDA tools as part of chip integration
- Test access mechanism via fabrics – New
  - Develop standards / EDA support for adapters to convert fabric protocol to JTAG / Scan fabrics
- Traditional DFT Solution
  - 1149 Compliant JTAG (boundary scan at chip etc)
  - Chiplet-level DFT to support Scan Isolation, LBIST, MBIST, IOBIST