

Networking

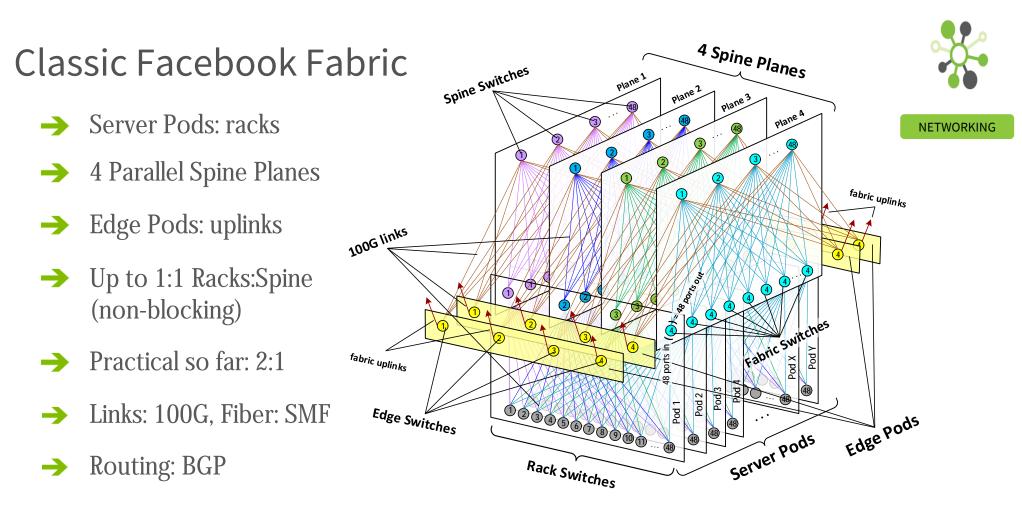
F16: the next-generation fabric

Alexey Andreyev, Network Engineer Facebook, Inc.





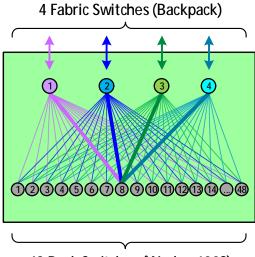




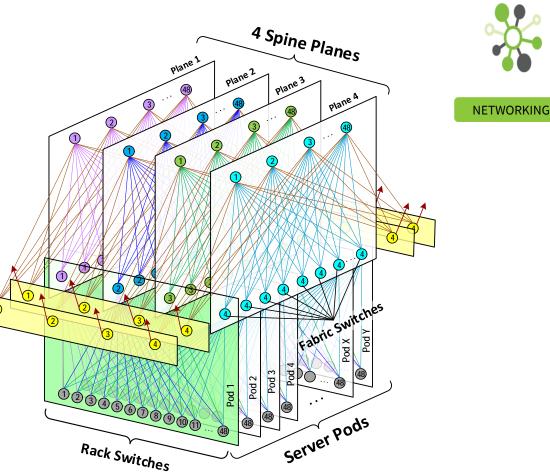




- → Server Pod: 48 racks
- → 4 x 100G per rack (400G)



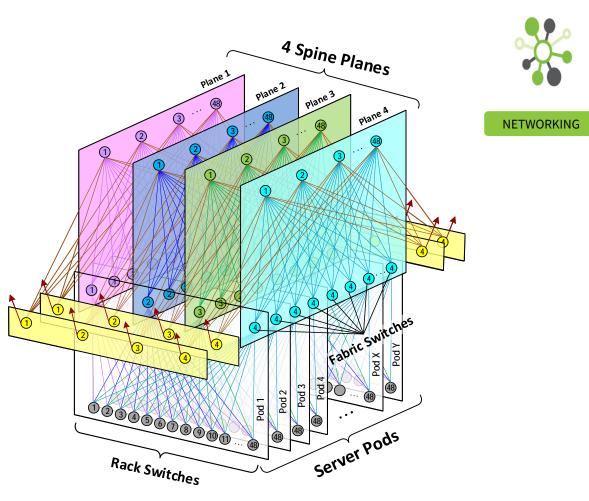
48 Rack Switches (Wedge-100S)





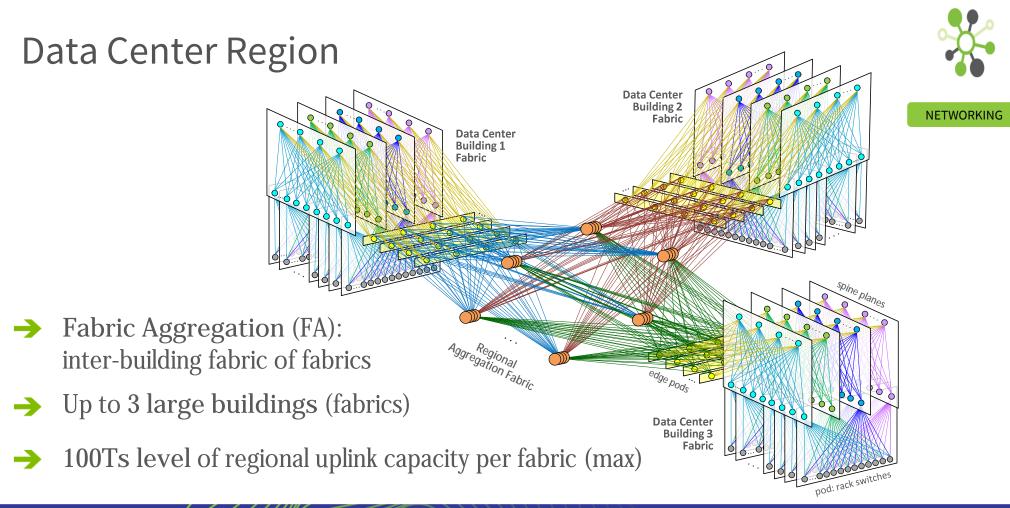
Fabric Spine Planes

- → Scalability without large boxes
- Capacity load balanced between and within the planes
- → Reliability contained failure domains and large-scale ops
- → Flexibility independent planes

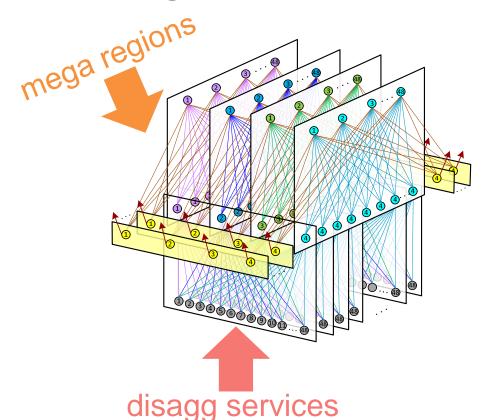








Growing pressures





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- Expanding Mega Regions
 (5-6 buildings) = accelerated
 fabric-to-fabric East-West demand
- Compute-Storage and AI disaggregation requires near-Terabit capacity per Rack
- Both require larger fabric Spine capacity (by 2-4x) ...





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DC network – a system with many parameters

- Bandwidth capacity
- Scale and scalability
- \rightarrow Topology and routing
- \rightarrow Regional composition
- → Lifecycle: deployment and retrofits
- → Automation and management

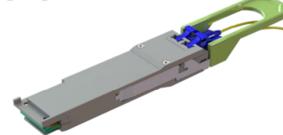
- → Servers and Services
- → Switch ASICs
- → Optics and link speeds
- → Power and cooling
- → Fiber infrastructure
- → Physical space
- $\leftarrow \text{ Timelines: need by vs. technology availability and development } \rightarrow$





Optics

- → Concerns: 400G availability @ scale
- → We start large no time for new tech to ramp-up
- → Risky dependency on bleeding-edge tech
- → High cost of early adoption
- → Interop for upgrade / retrofit paths
- → Large-scale ISP and OSP structured fiber plants

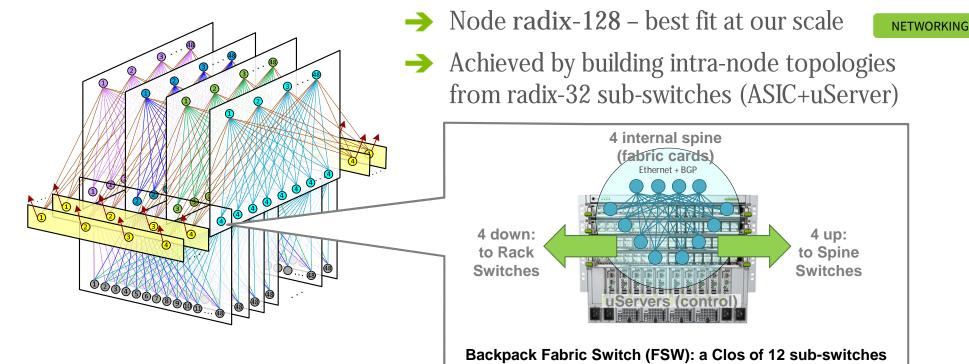






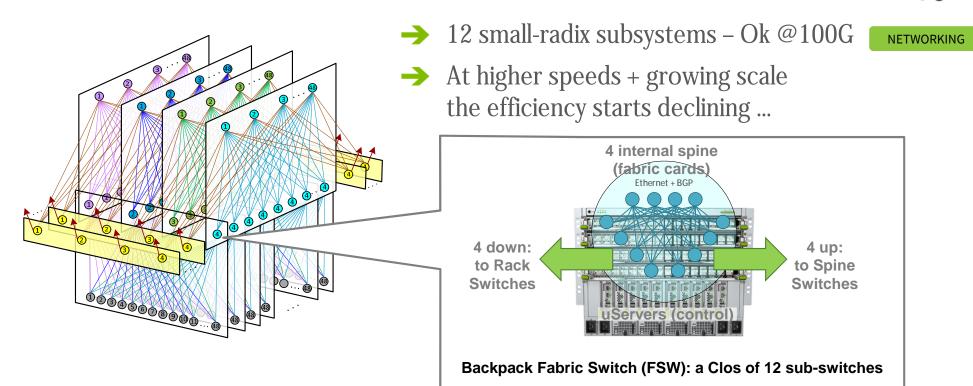




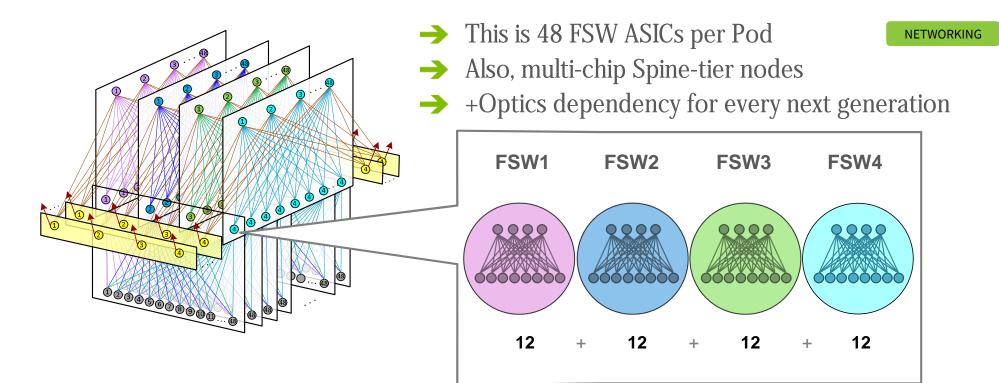




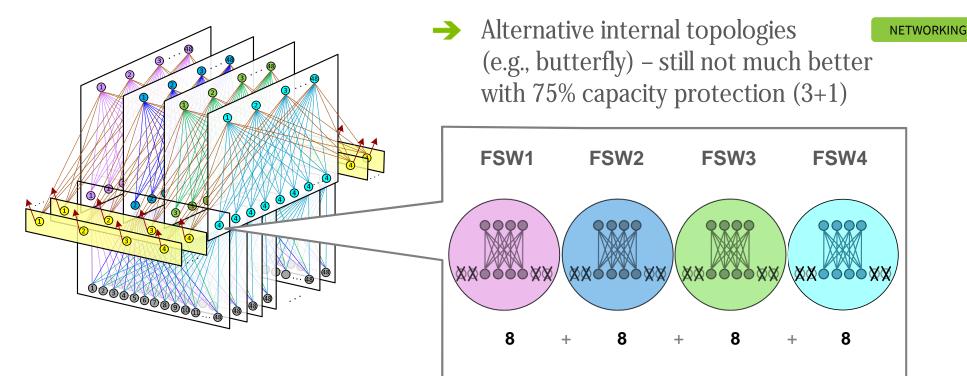










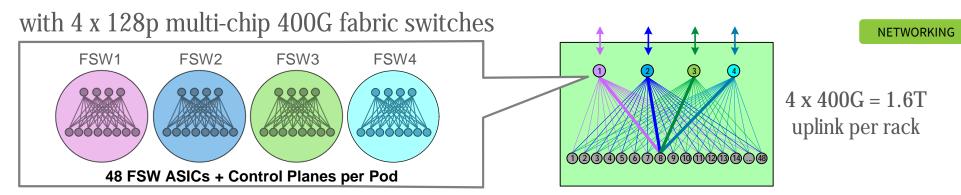








What's Next?



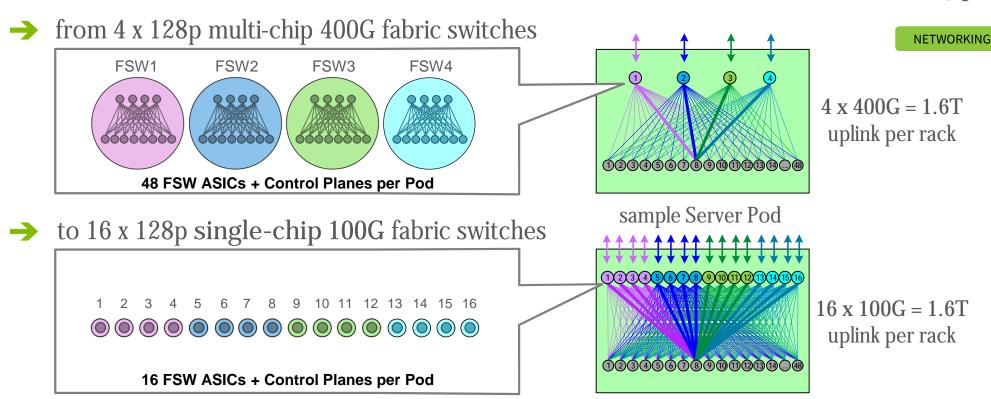
How would we achieve the next 2-4X after 1.6T?

- → Adding more fabric planes on multi-chip hardware = too much power...
- → Increasing link speeds = would need 800G or 1600G optics in 2-3 years...





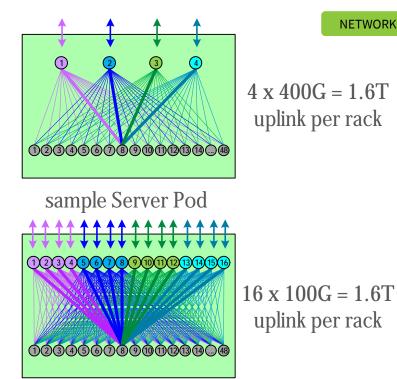
Introducing F16 fabric





Introducing F16 fabric

- Same ASIC building block as multi-chip \rightarrow candidate: Broadcom Tomahawk-3
- Same rack uplink bandwidth capacity \rightarrow as 4 x 400G: up to 1.6T per TOR
- 3X+ less chips and control planes = \rightarrow TCO and Ops efficiency







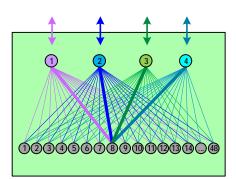


NETWORKING

 $4 \times 400G = 1.6T$ uplink per rack

Introducing F16 fabric

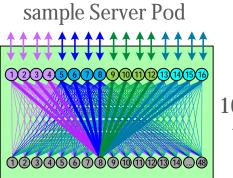
- → 2X+ less power/Gbps than 100G F4 fabrics
- Mature and available optics, instead of high-volume bleeding edge ramp-up: OCP 100G CWDM4
- → Realistic next-steps scalability:
 - optimized for power in current and future generations
 - 200G or 400G optics as the way to achieve the next 2x or 4x



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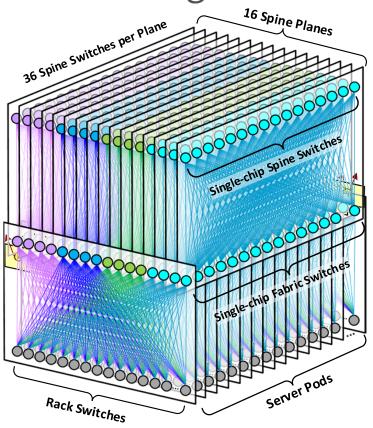
 $4 \times 400G = 1.6T$ uplink per rack



16 x 100G = 1.6T uplink per rack



F16 fabric design



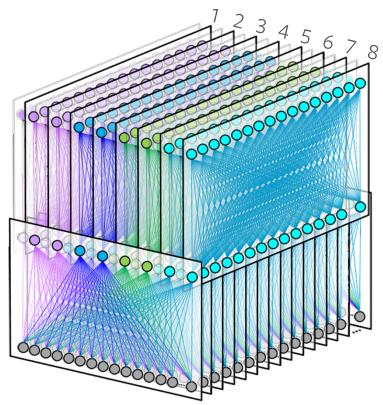


- Up to 16-plane architecture: NETWORKING achieving 4X capacity with 100G links
- Up to 1.6T capacity per rack
- Single-chip radix-128 building blocks
- Locked Spine scale at 1.33:1 from start (36 FSW-Spine uplinks for 48 Racks/Pod)
- No Edge Pods replaced with direct Spine uplinks to new large-scale Disaggregated FA



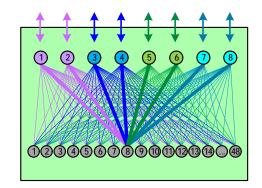


F16.8P: 8-plane variant





- → Physical Infra and fiber designed and built for full F16
- → Starting number of parallel planes: 8
 - **800G** capacity per rack (8 x 100G)



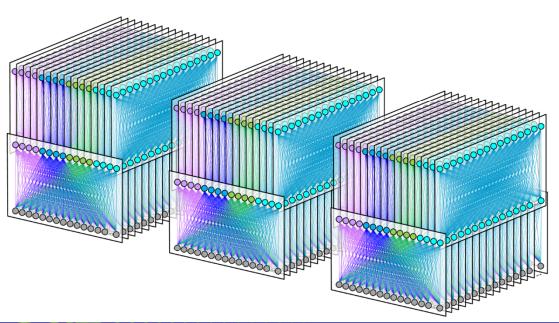




F16 region evolution: HGRID

- → Edge Pods → direct Spine-FA uplinks
- No device is big enough to mesh F16 fabrics – disaggregated solution required
- Goal: mega-region beyond 3 fabrics

each F16 fabric = 576 Spine Switches (SSWs)





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F16 region evolution: HGRID



Partial Mesh = additional routing and reachability considerations

slice = all Spine Switches (SSWs) of the same number

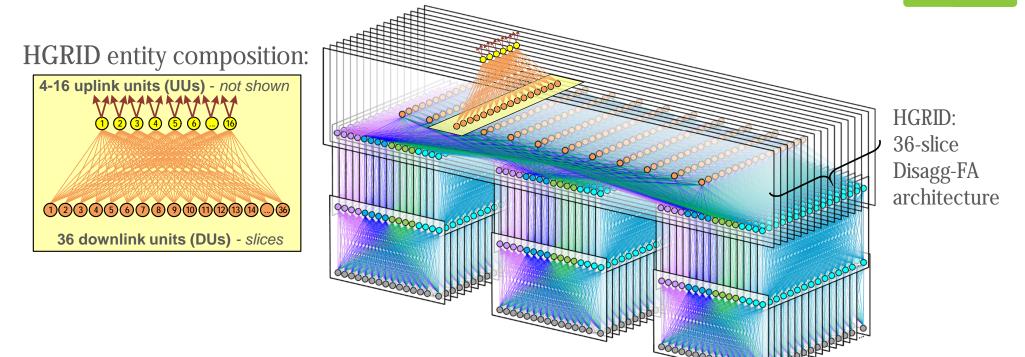






F16 region evolution: HGRID

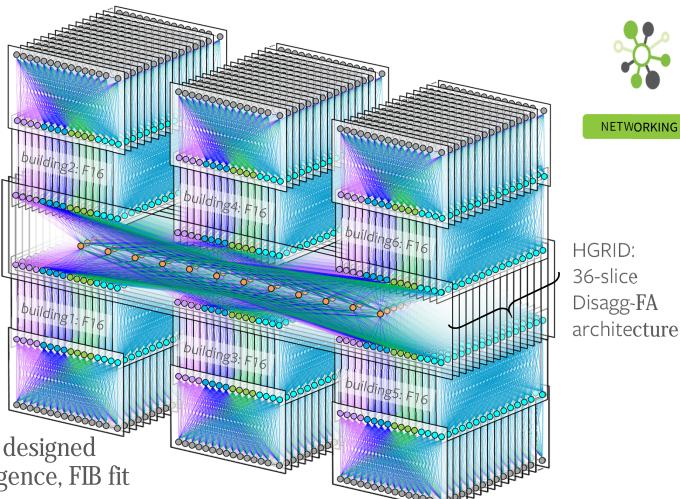






F16 mega-region

- → Sample 6-building region with full-size F16 fabrics
- Petabit-level regional uplink capacity, per fabric
- Evolution of our
 Fabric Aggregator
 with new building blocks
- BGP routing end-to-end, designed for reliability, fast convergence, FIB fit



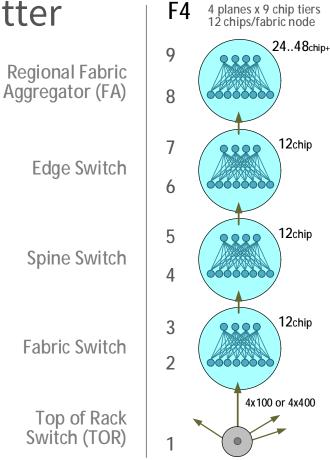




Simpler and Flatter

Over 3X less \rightarrow switch ASICs and control planes in fabric

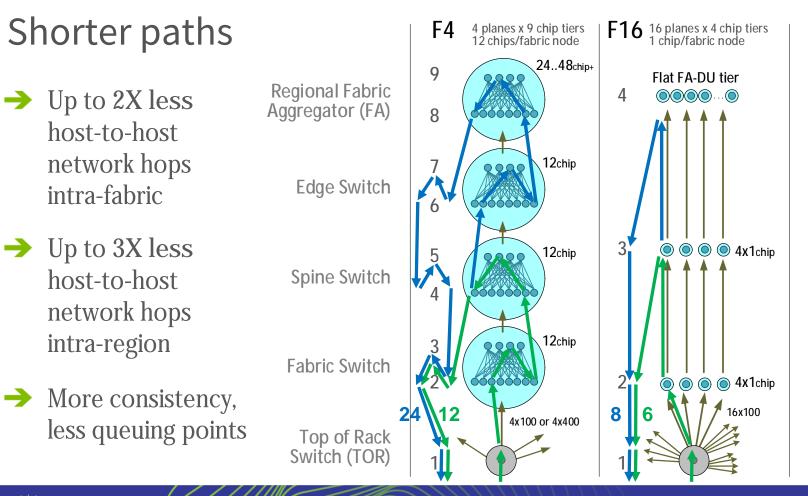
2.25X less \rightarrow tiers of chips in the topology







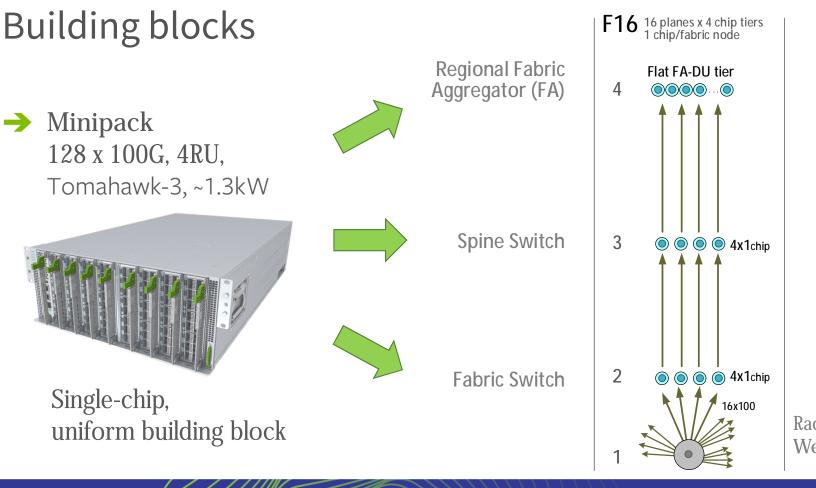












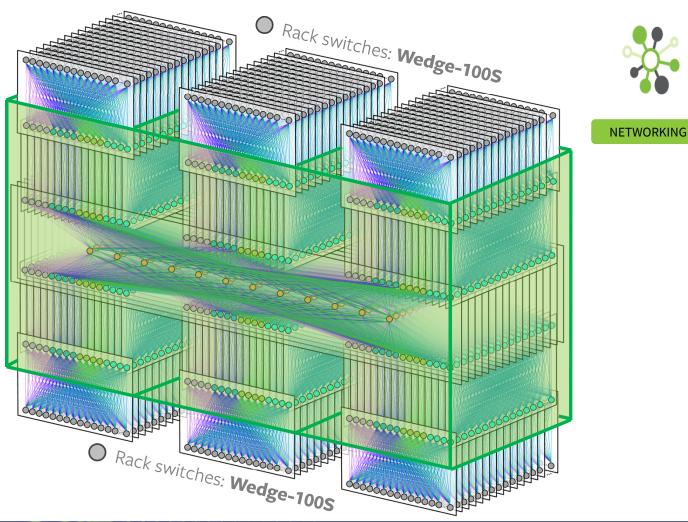
Rack switches: Wedge-100S



Building blocks

→ Minipack 128 x 100G, 4RU, Tomahawk-3, ~1.3kW







Building blocks

→ Facebook Minipack FBOSS



→ Arista 7368X4 FBOSS or EOS



Single-chip, uniform building block modular PIMs = interface flexibility







To summarize

- → F16 fabric: achieving 4X bandwidth at scale, without 4X faster links
- → 8 planes, 16 planes: new dimension of scaling
- → 100G links: not forced to adapt next-gen optics from early day1
- → Power savings: both now and in the future iterations
- → Next steps: clear path to the next 2-4X on specific tiers or all-around







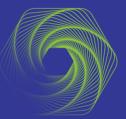
To summarize

- → Simpler: single-chip large-radix systems improve efficiency
- → Flattened: 3X+ less ASICs, 2.25+X less tiers, 2-3X less hops between servers
- → Minipack: one flexible and efficient building block for all roles in fabric
- → HGRID: disaggregated aggregation scaling the multi-fabric regions in both bandwidth and size









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OCP Global Summit | March 14–15, 2019



