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Heterogeneous Integration Roadmap

NOVEMBER 9-10, 2021

Heterogeneous Integration Roadmap

Madhu Iyengar, Principal Engineer, Google
WIlliam Chen, Fellow, ASE
Ravi Mahajan, Fellow, Intel
Kanad Ghose, Distinguished Professor, Binghamton University

on behalf of the HIR Team

OCP Summit, Wed, Nov 10, 2021

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Heterogeneous Integration Roadmap (HIR)

Launched 10-10-2019
24 chapters
590 Pages
Free download
Download Link
https://eps.ieee.org/technology/heterogeneous-integration-roadmap

- Sponsored by 3 IEEE Societies (EPS, EDS & Photonics) together with SEMI & ASME Electronics & Photonics Packaging Division
- Comprehensively covering microelectronics technology ecosystem
- Articulates state-of-the-art Advances in Technology & Science, Future directions, Significant roadblocks & Potential solutions
- HIR is the Knowledge Roadmap & Knowledge Supply Chain for the Heterogeneous Future

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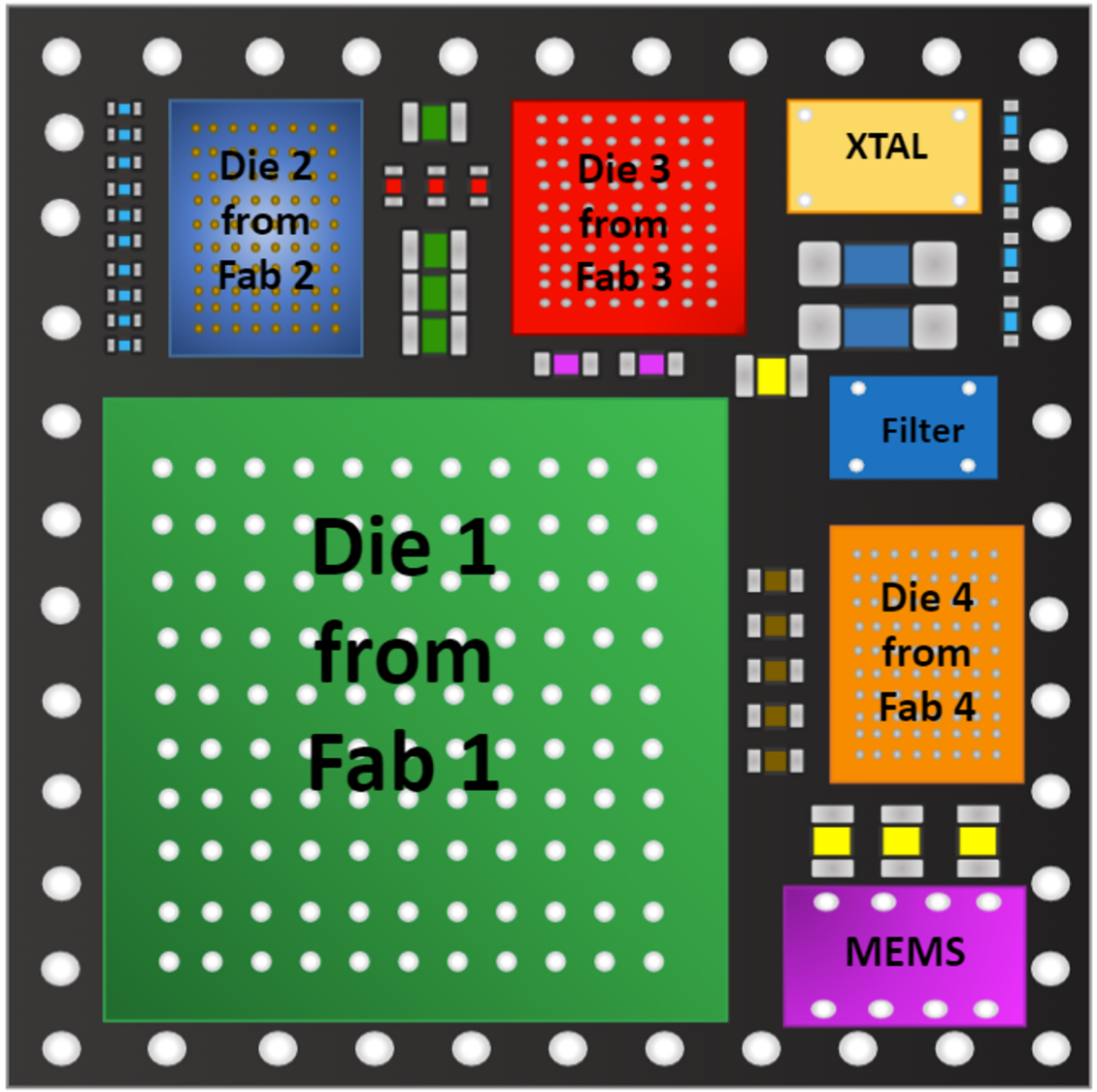
Heterogeneous Integration:

HETEROGENEOUS INTEGRATION ROADMAP

Heterogeneous by material, component type, circuit type, node and bonding/interconnect method & sources



HI is the integration of separately manufactured components into a higher-level assembly
that, in the aggregate, provides enhanced functionality and improved operating characteristics.

IEEE Press Release 10-10-2019

PISCATAWAY, N.J.--(BUSINESS WIRE)--IEEE, the world's largest technical professional organization dedicated to advancing technology for humanity, today announced the 2019 release of the **Heterogeneous Integration Roadmap (HIR), a roadmap to the future of electronics identifying technology requirements and potential solutions. The primary objective is to stimulate pre-competitive collaboration among industry, academia and government to accelerate progress. The roadmap offers professionals, industry, academia and research institutes a comprehensive, strategic forecast of technology over the next 15 years. The HIR also delivers a 25-year projection for heterogeneous integration of emerging devices and materials with longer research-and-development timelines**

Heterogeneous Integration Roadmap

An Application Driven Roadmap

Market/System Applications

- High Performance Computing & Data Center
- Mobile
- Medical, Health & Wearables
- Automotive
- IoT
- Aerospace & Defense

Heterogeneous Integration Components

- Single Chip and Multi Chip Integration (including Substrates)
- Integrated Photonics
- Integrated Power Electronics
- MEMS & Sensor integration
- 5G Communications & Beyond

Cross Cutting Technologies

- Materials & Emerging Research Materials
- Emerging Research Devices
- Test
- Supply Chain
- Security
- Thermal Management
- Reliability (new chapter for 2021)

Integration Processes

- SiP
- 3D +2D & Interconnect
- WLP (fan in and fan out)

Co-Design & Simulation

- Co-Design & Simulation – Tools & Practice

Beyond Miniaturization Tunnel

Photo credit: Prof. H.-S.P. Wong, Stanford

At 2020 ERI Conference the Plenary Speaker, (Prof Philip Wong, Stanford University, and TSMC Chief Scientist) gave talk “Future is System Integration. He illustrated semiconductor research near the end Moore’s Law like a person walking out of a long tunnel seeing green field & sun light.

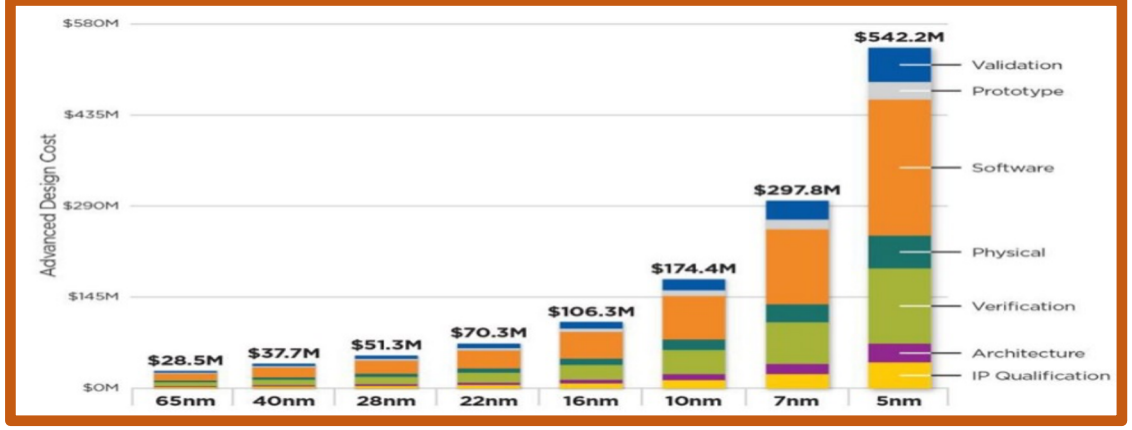
During Moore's Law time the single focus is miniaturization towards the next set of nodes.

As one emerges from the miniaturization tunnel, opportunities for research outlook & innovations becomes infinitely brighter and broader.

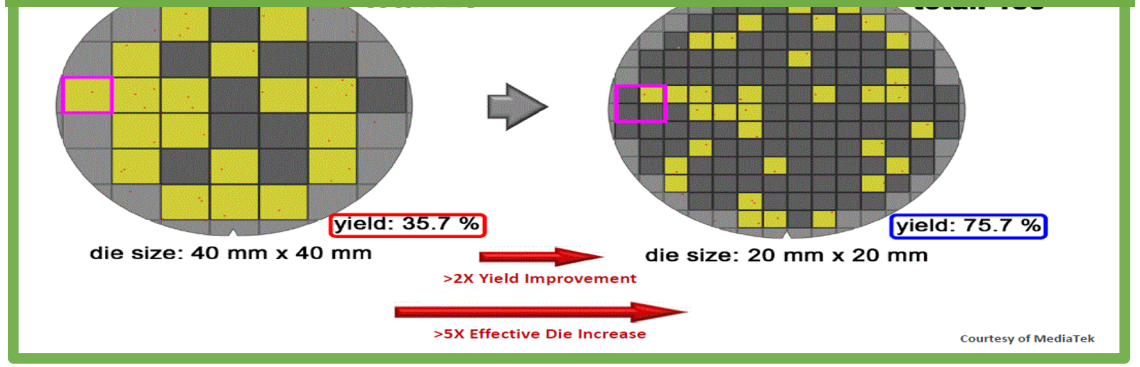
Photo Source: S. Mitra, HIR Symposium Feb 24, 2021

Heterogeneous Integration Key Drivers

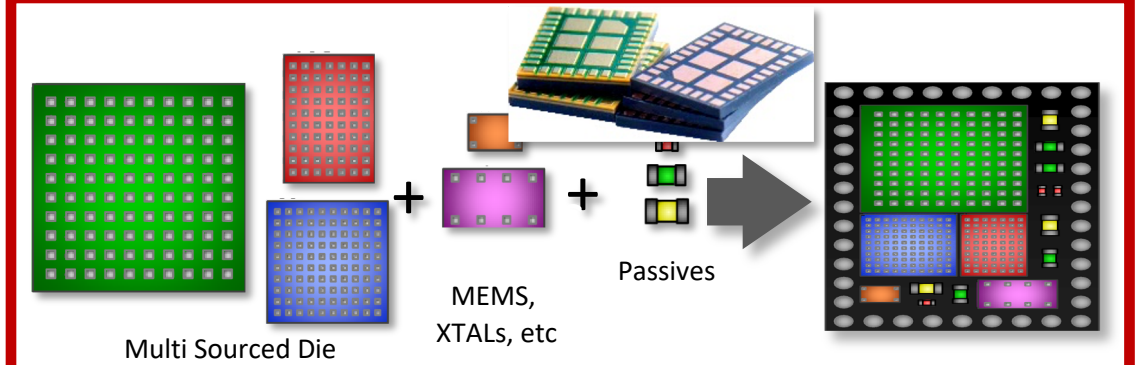
Single Digit Nodes Dev Cost



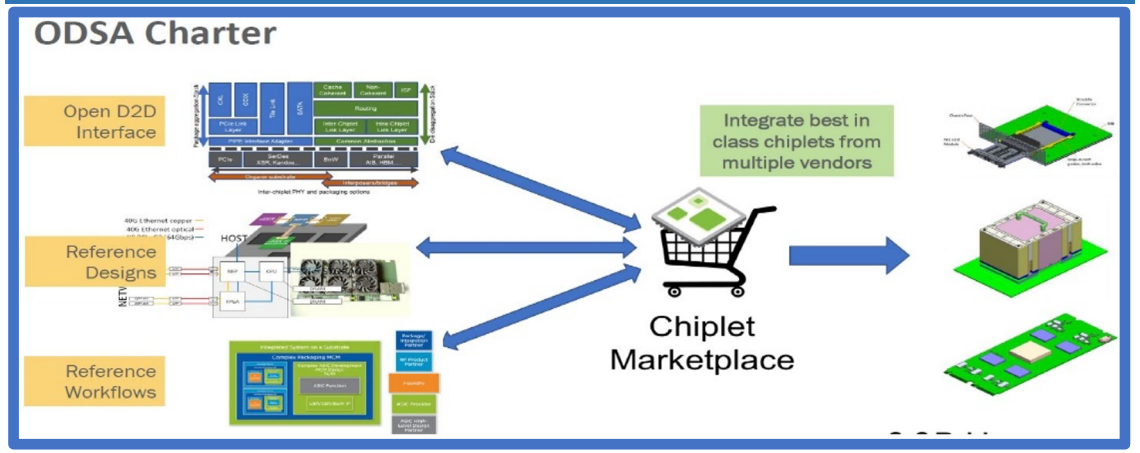
Adv Si Nodes Optimal Design & Yield (chiplet)



Si Node & Functonal Optimization

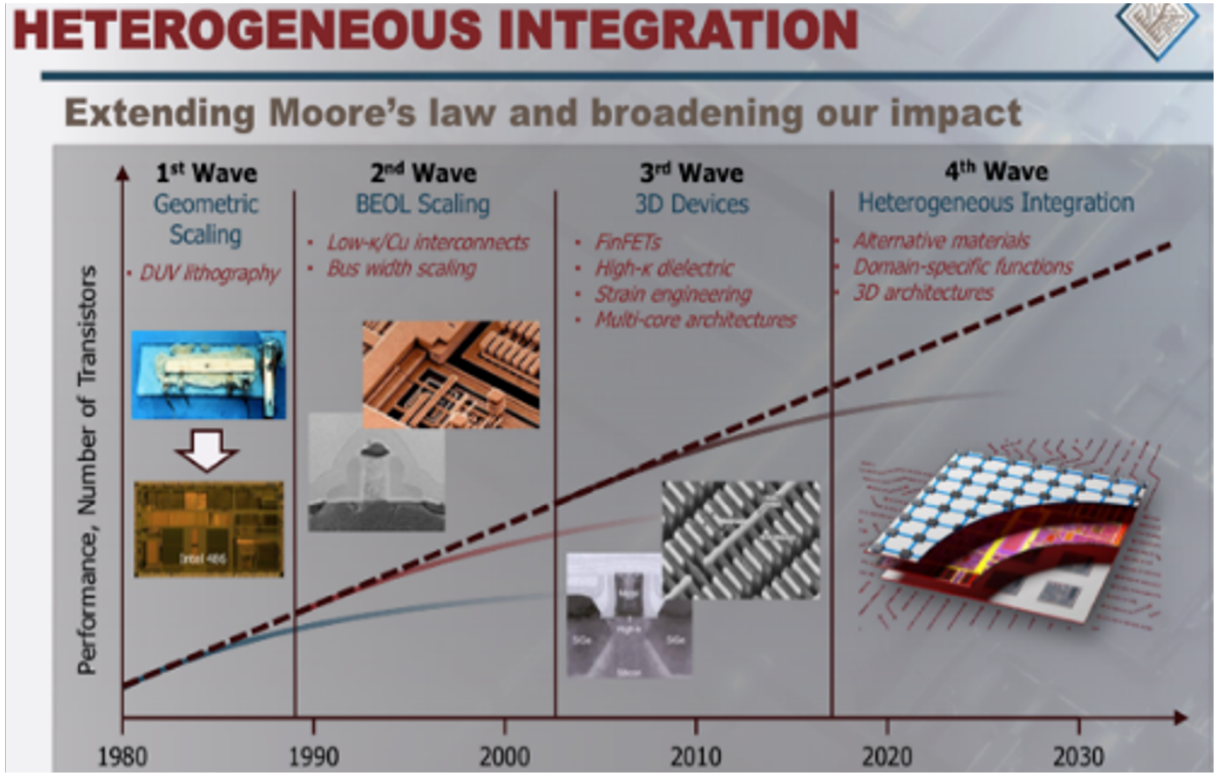


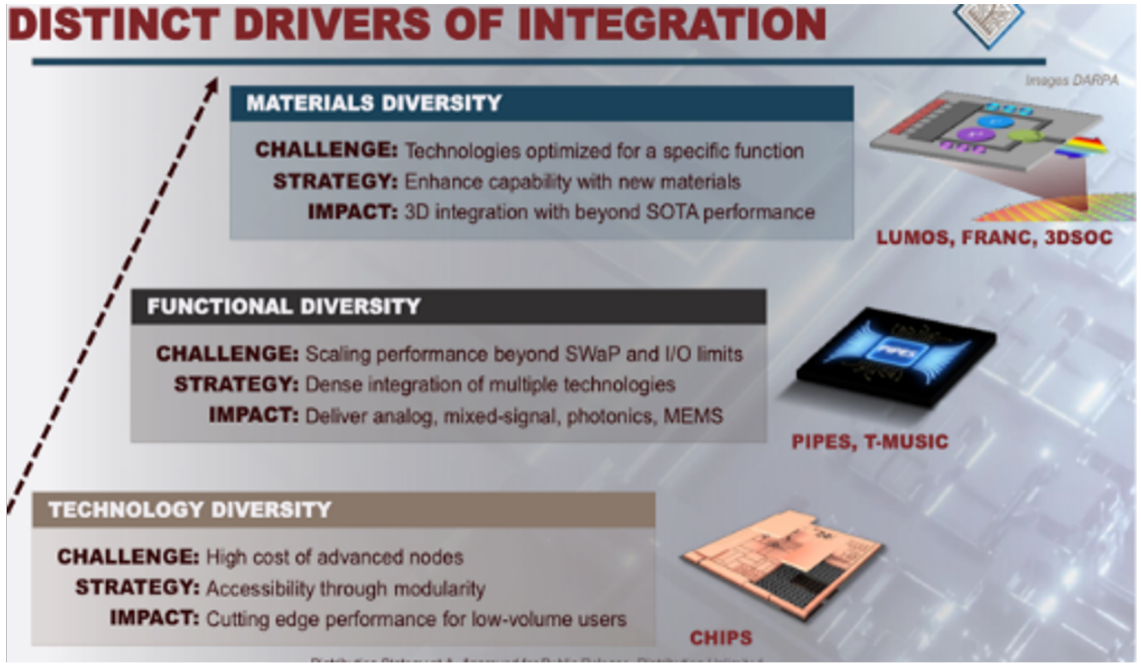
ODSA Chiplets Vision

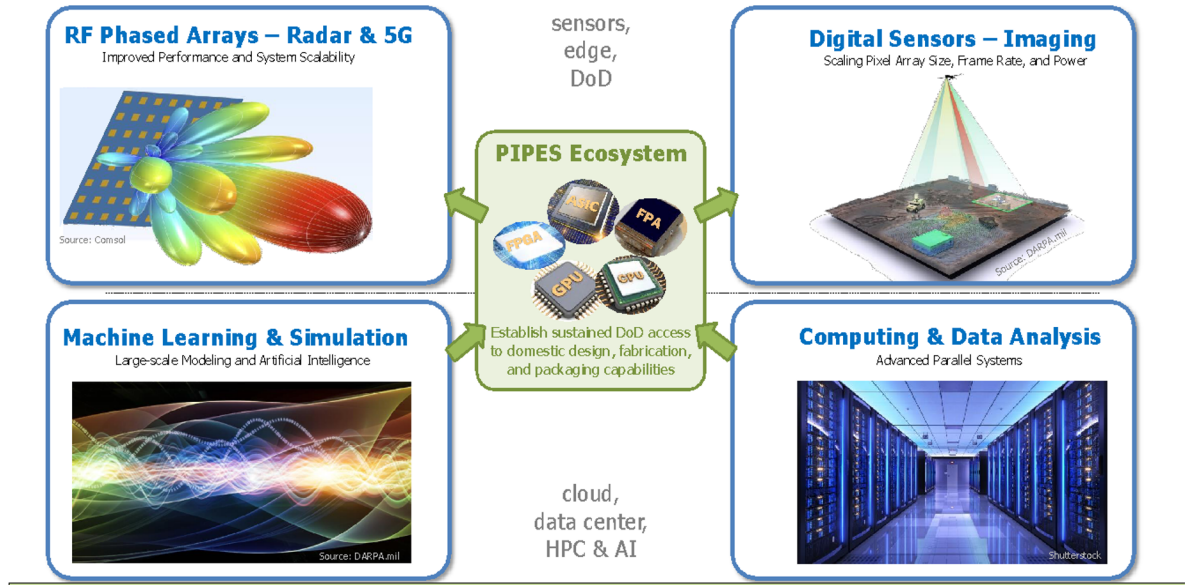


Presentation: “Accelerating Electronics and Photonics Innovation for Revolutionary Microsystems” Dr Gordon Keeler
DARPA, Heterogeneous Integration Roadmap Annual Conference 02-24-2021

Heterogeneous Integration in DARPA Electronics Resurgence Initiative (ERI)







Facilitating DoD Access: Create an ecosystem for package-level optical signaling, enabling disruptive advances for artificial intelligence, phased arrays, sensors and processing.

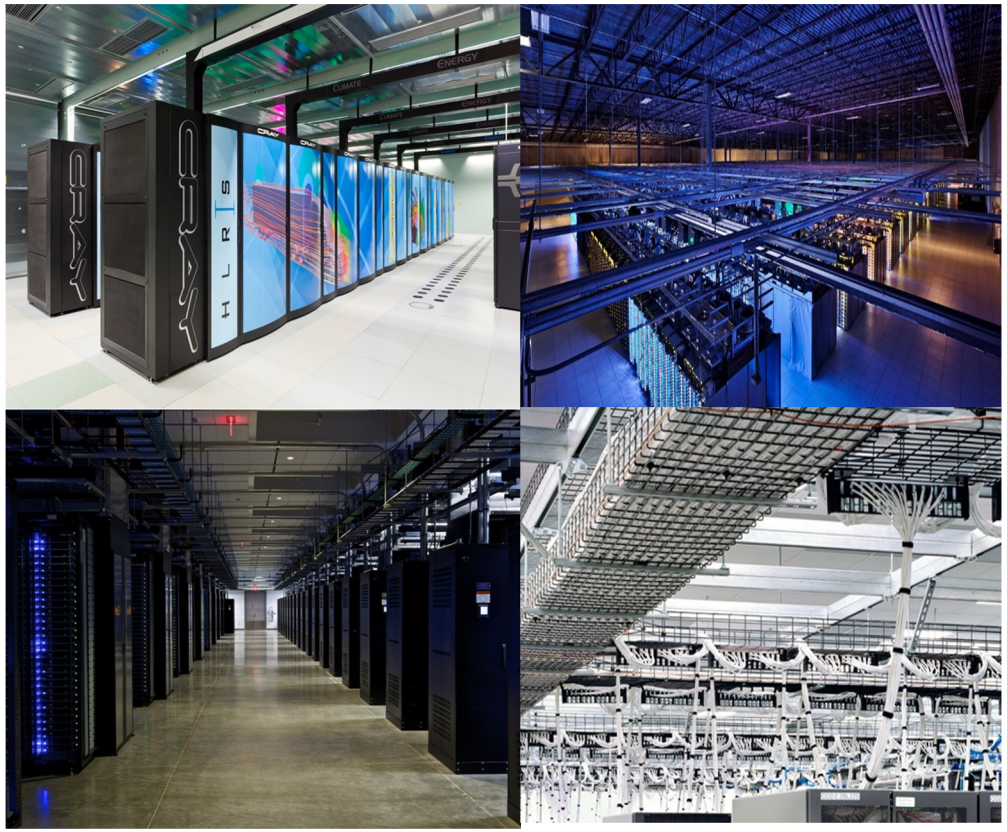
Heterogeneous Integration Roadmap for HPC and Data Centers

Reference: Heterogeneous Integration Roadmap Chapter 2, 2019 + 2020 update

This Technical Working Group (TWG) focuses on future needs, future requirements, and potential solutions for realizing Heterogeneous Integration that integrate processing elements, accelerators, storage, IO etc. for the following market segments:

- HPC Systems
- Scale-out Systems
- Data Centers
- High-end Networking

Specifically, this TWG explores the system-level implications related to performance, power management, security, power distribution issues and others



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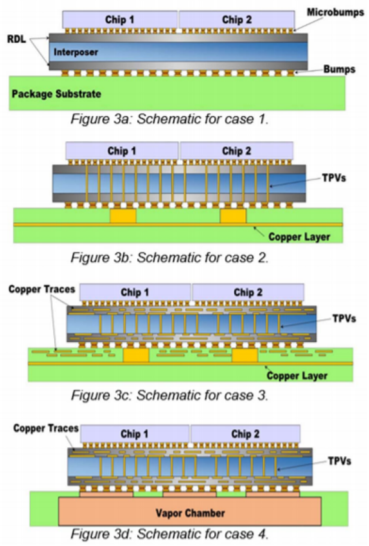
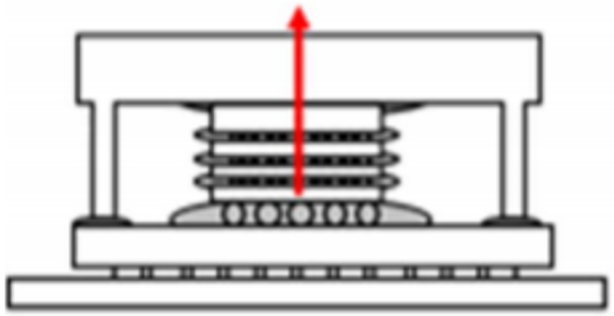
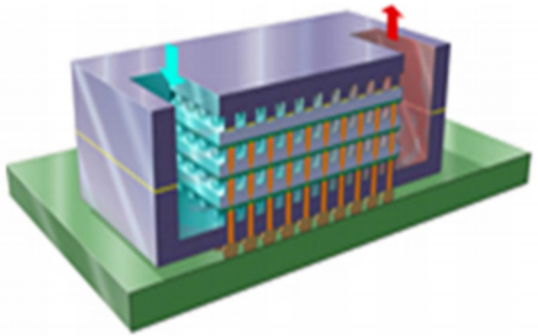


1. 2D chip with stacked memory on a silicon/glass interposer



2. 3D stacked die with conduction interfaces



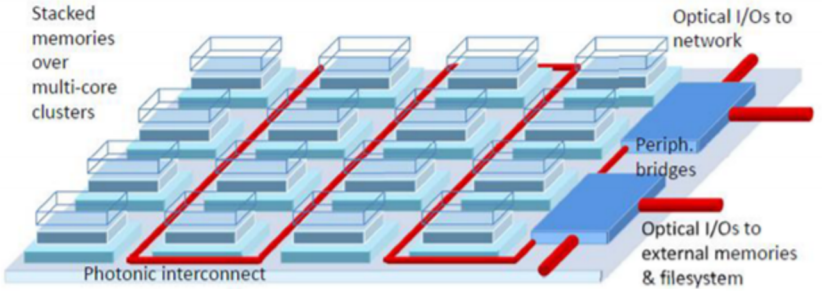
3. 3D stacked die with embedded liquid cooling

Canonical Thermal Heterogeneous Integration Problems

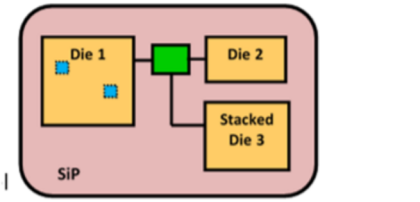
Chapter 20, 2019 IEEE Heterogeneous Integration Roadmap (link)

Chair: Madhu Iyengar (Google)

Co-Chairs: Azmat Malik, Weihua Tang (Intel)



4. Optics/photonics based Heterogeneous package

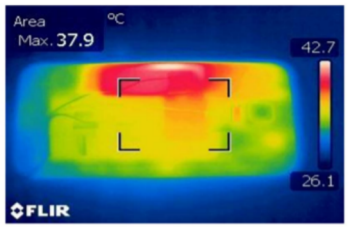


On-die voltage regulator

Package-level DC-to-DC level shifter/voltage regulator

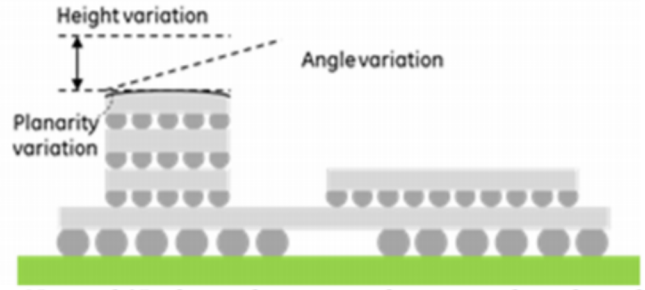
Figure 16: Package level DC to DC VR schematic

7. Voltage Regulators in a Heterogenous Package



: Temperature contour data for the external surface of a SmartPhone [10]

6. Mobile application chipset (package on package, fan out, bridge)



Notional 3D chip architecture and anticipated topology challenges

5. Harsh environment (military, aerospace, automobile)

Research Areas In Thermal Management

Chapter 20, 2019 IEEE Heterogeneous Integration Roadmap (link)

[A] Thermal Interface Materials

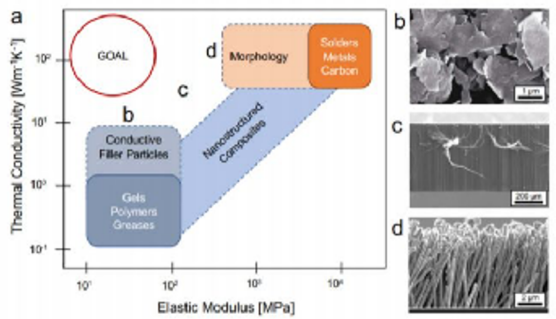
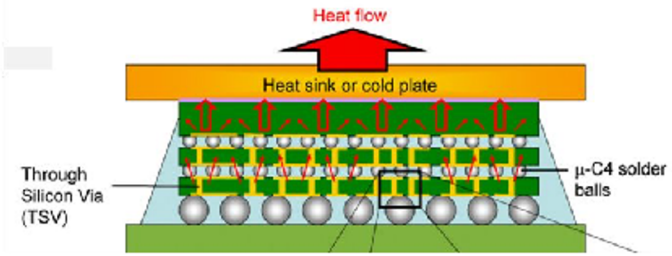


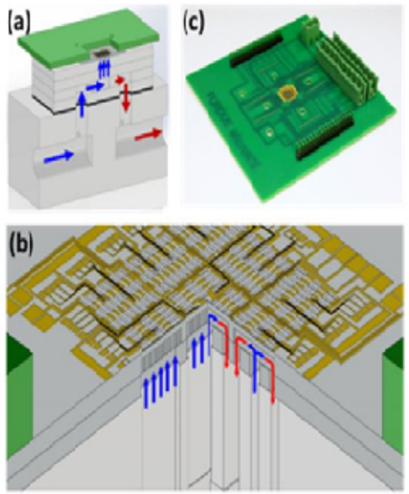
Figure 17 (a) Two common strategies can be employed to create high-performance TIM composites [14], (b) an example of graphene-polymer composite [15], (c) vertically grown nanotubes [16-17], (d) vertically electrodeposited nanowires [14, 18]

[B] System thermal limits for HPC multi-chip modules

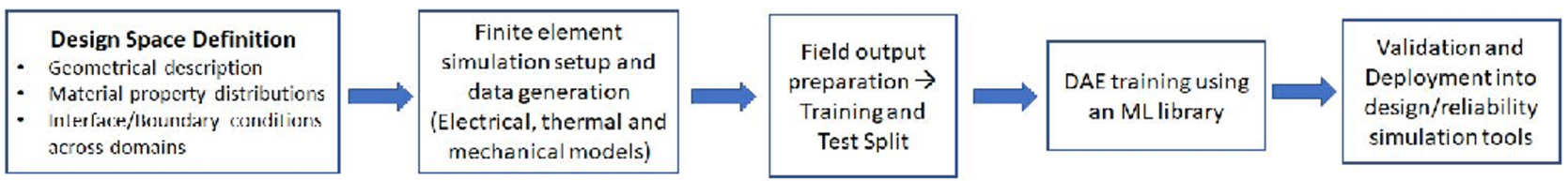


A 3D chip stack using advanced materials in the conduction heat flow path.

[C] Embedded liquid cooling of chip & chip stacks



[E] Thermomechanical Modeling for Heterogeneous Integration



[D] Advanced Thermal Materials for Thermal Management

Thank you for Listening

In full acknowledgement of the spirit of dedicated collaboration of Heterogeneous Integration Roadmap Technical Working Groups

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Summary and Call to Action

- We are at a unique period in time where the global convergence of technology chaos & business disruption are suddenly joined by the Covid 19 Pandemic still spreading around the world.
- There is immense need for a pre-competitive technology roadmap addressing future vision, difficult challenges, potential solutions.
- Heterogeneous integration (e.g SiP & Chiplets) is a powerful technology direction for system/subsystem integration.
- Data Center & Cloud Future – Major driving forces of innovations in Heterogeneous Integration system & packaging architecture, materials, equipment , sensors, devices, 2D & 3D delivering function, value, & time to market.

HIR and OCP collaborations can enable next gen Heterogeneously Integrated Systems

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