



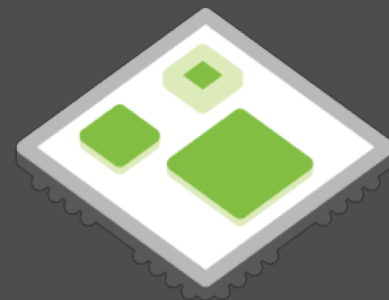
Design Tools for Chiplet-Based Design

Jawad Nasrullah

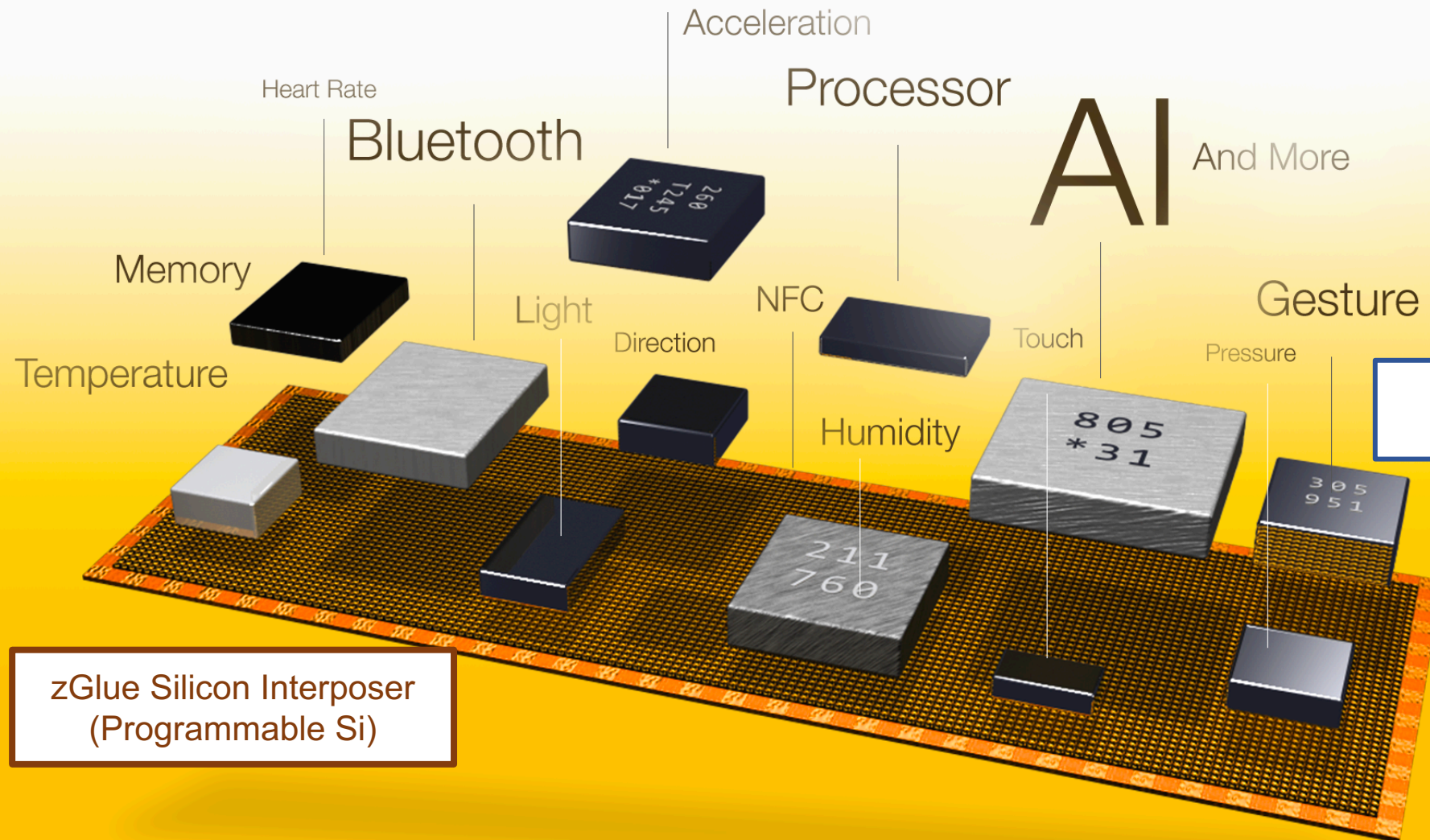
ODSA Project Workshop

March 28, 2019

Consume. Collaborate. Contribute.



zGlue Chiplet-Based IC Technology



Tools Needed for Chiplet Based IC Design

- Electrical Design Entry (Schematic or RTL)
- Layout, 2D and 3D (Package, Interposer, SiP, Si)
- Parasitic Modeling
- Thermal Mechanical Modeling and Simulations
- Electrical and Functional Simulations

EDA Companies Are Offering Most of these Design Tools, though offered in bits and pieces that are difficult to splice together for now.

Packaging PDKs are available for volume customers only.



Tools Needed to Enable Chiplet Marketplace

- Be Able to accurately define Chiplets in electrical, mechanical, and thermal sense.
- A standard data format to define a chiplet will help with trading as well as correct simulations.
- zGlue has developed a data-exchange format to define Chiplets (**Candidate for OCP/ODSA Feature**).

Chiplet Data Models includes definitions for:

- i. Mechanical (used for mechanical and thermal design)
- ii. IO (used for footprints and netlisting)
- iii. Power (used for power simulations)

Chiplet data-exchange feature will allow chiplet vendors to encode and list their chiplets but keep access control.

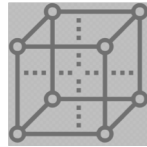


zGlue Design and Fab Flow

Design



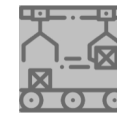
Prototype



Evaluation

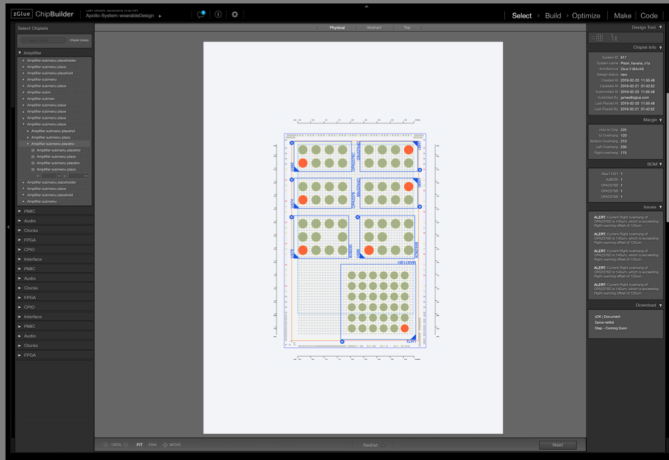


Mass Production



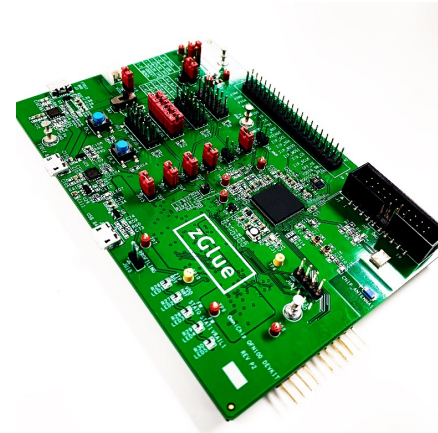
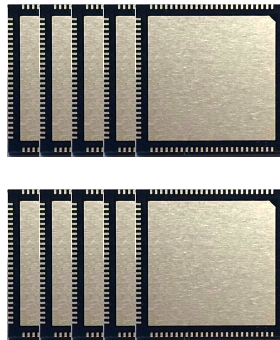
ChipBuilder

zGlue Software



Shuttle

zGlue Prototype Program



Mass Production

Outsourced to zGlue Partners





zGlue ChipBuilder Capabilities

Today

ChipBuilder Basic Launched at CES

- Library of 22 chiplets
- Manual placement of chiplets
- Design capture with schematic
- Automatic routing of chiplets, IOs and powers
- Support for built-in programmable pullup and pulldown resistors, smart fabric controls and interfaces
- Built-in Design Rules Checks and Validations
- Targetted at Ultra-low power embedded devices

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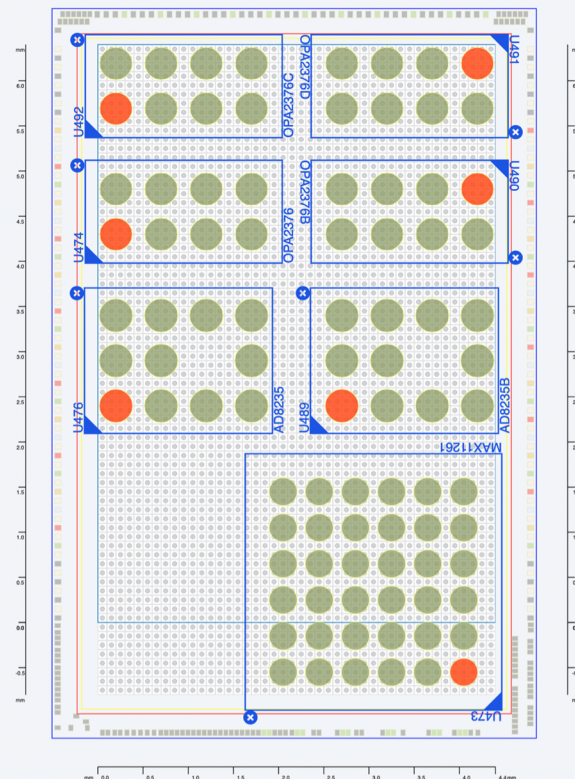
ChipBuilder Pro

New Features

- Library of 100 Chiplets
- **Private Chiplet encoding, sharing, and access-control of chiplets: Candidate for OCP/ODSA Special Feature**
- Download simulation input files for thermal, signal integrity, power integrity analysis
- Designs ready for small-volume runs on a shuttle targeted for early Q3
- Support for higher performance
- Sign up for trial access

▶ **FPGA**

Time (t, min)	Control (N)	100 mg/L (N)	200 mg/L (N)
0.0	0	0	0
0.5	20	18	15
1.0	40	35	30
1.5	60	55	45
2.0	80	75	35
2.5	95	85	30
3.0	100	90	25
3.5	100	90	20
4.0	100	90	40



System ID	617	
System name	Pison_havana_v1a	
Architecture	Zeus 2 (64x44)	
Design status	new	
Created At	2019-02-20	11:55:48
Updated At	2019-02-21	01:42:52
Submitted At	2019-02-20	11:55:48
Submitted By	james@zglue.com	
Last Placed At	2019-02-20	11:55:48
Last Placed By	2019-02-21	01:42:52

chip to Chip	225
to Overhang	120
Bottom Overhang	210
Left Overhang	230
Right overhang	175

ALERT: Current Right overhang of OPA2376D is 140um, which is exceeding Right warning offset of 125um.

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Download ▼

zDK | Document
Spice netlist
Step - Coming Soon



Accelerate Hardware Innovation

CUSTOM CHIPS ON DEMAND