Building an Open Chiplet Economy

An OCP Sponsored Tutorial/Workshop
Chiplet Summit, San Jose California
January 24 2023, 1:00PM – 5PM

Moderator: Cliff Grossner, Ph.D., VP Market Intelligence & Innovation, OCP

Organizer: Bapi Vinnakota, Ph.D., ODSA Project Lead, OCP

OPEN Compute Project®

Community-driven hyperscale innovation for all.

Participating in the New Open Chiplet Economy

1. The Emerging Chiplet Economy (Bapi Vinnakota)
2. Why Does the Market Want Chiplets
   - Chiplet use cases for new applications (Dharmesh Jani, Meta)
   - Open Chiplets to enable a new era of silicon (Amber Huffman, Google)
   - Chiplets in HPC (John Shalf, DoE)
3. Building Chiplets and System in Package (SiP) (Chiplet Vendors and (SiP) Builders)
   - D2D Interface for Multi-Chiplet AI System(Sid Seth, dMatrix)
   - PHY Interoperability Testing (JP Balachandran, Cisco)
   - One Click Chiplet Interconnect (Elad Alon, Blue Cheetah)
   - A Chiplet Reference Platform: Leveraging BoW (Kevin Yee, Samsung; Andy Heinig, Fraunhofer)
4. Arming the Vendors and Builders of the Chiplet Economy
   - Using a Markup Language in Chiplet-Based Design (James Wong, Palo Alto Electron)
   - The Open Chiplet Ecosystem: Accelerating AI Hardware- (Arvind Kumar, IBM)
   - Drop in FPGA Chiplet (Kash Johal, eTopus)
5. Panel Session - Key enablers needed for an open Chiplet Economy: When and How?
   Moderator: Tom Hackenberg Yole
   Members: John Shalf(DoE), Alvin Loke (NXP), Kevin Yee (Samsung), Bapi Vinnakota (OCP) Travis Lanier (Ventana)

What is being Announced Today

- New alliance between OCP Foundation and JEDEC Solid State Technology Association

  Brings together

  - JEDEC's strength in setting global standards for the microelectronics industry
  - OCP's expertise in specifying system level devices seeding emerging technologies and markets

  - To set new global standards for novel device components in emerging markets eliminating market fragmentation and wasteful duplication of efforts

- Automating System in Package (SiP) design and build using Chiplets
  - Chiplet Description Schema (CDXML) specification now released by OCP
    - Enables a standardized Chiplet part description for use with today's EDA tools
    - Allows Chiplet builders to provide electronically description to their customers
  - Integration of CDXML into JEDEC JEP30 underway, JEDEC ratified standard mid 2023

Chiplet Description Schema (CDXML) Automates SiP Design and Build

Chiplet economy as modeled after today's silicon business will require

- Standardized design models to ensure operability in EDA workflows
- Standardized design and integration workflows for SiPs
- Integration to build SiPs in the context of multi-chiplet modules for 2.5D stacked, and 3D Integrated circuits
- Electronically readable descriptions include following information:
  - Thermal
  - Physical/Mechanical
  - Behavioral
  - Power, Power/Signal Integrity
  - Electrical, Test
  - Security information

schema.xsd

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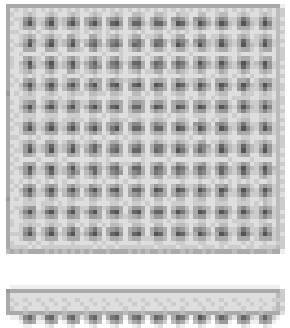
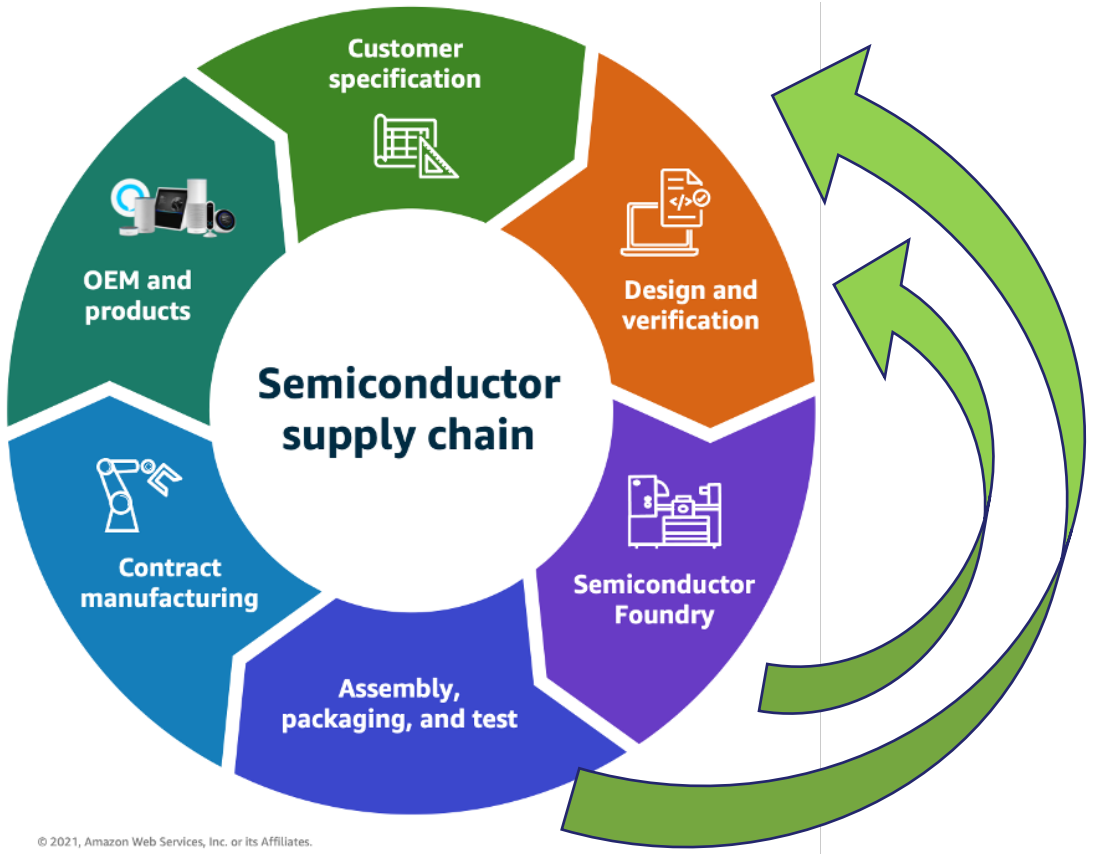


Chiplets Will be Everywhere Chips Are

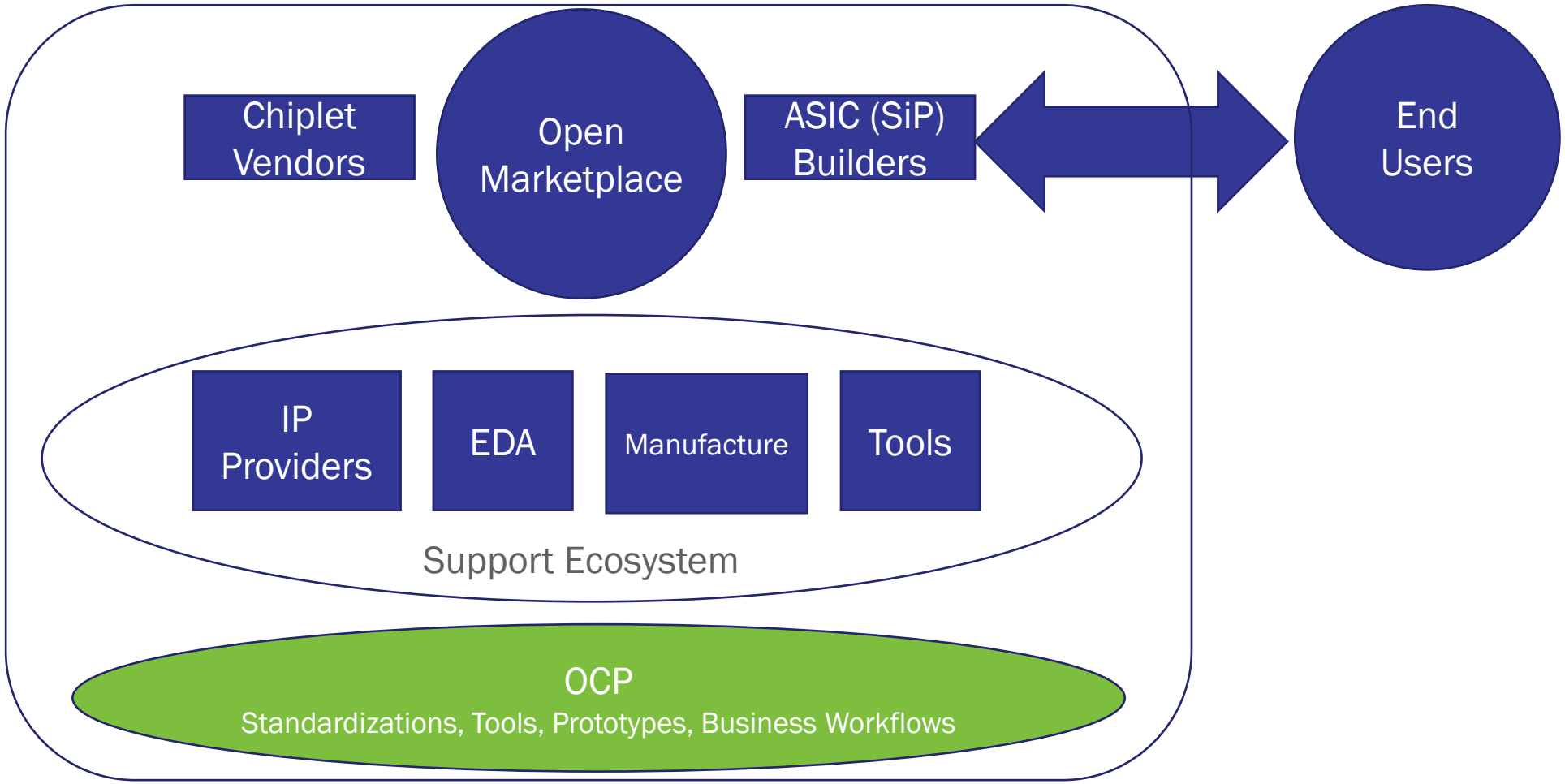
Semiconductor worldwide revenue by end vertical, sales (source: Gartner)

End vertical	Example	% of total 2020	% of total 2025E	2025 revenue projection	2021E-2025E% CAGR
Automotive	ADAS, Infotainment Chassis	8.3%	12.0%	$80.2B	12.4%
Communication	Smartphones	32.9%	31.5%	$210.3B	3.0%
Consumer	TVs, Digital Set-Top Box	10.4%	10.5%	$70.3B	2.6%
Data processing	PCs, Servers, Storage Media	37.7%	33.8%	$225.6B	1.6%
Industrial	Automation, Healthcare, Security	10.7%	12.1%	$80.7B	8.5%

Need new integration across the Value Chain

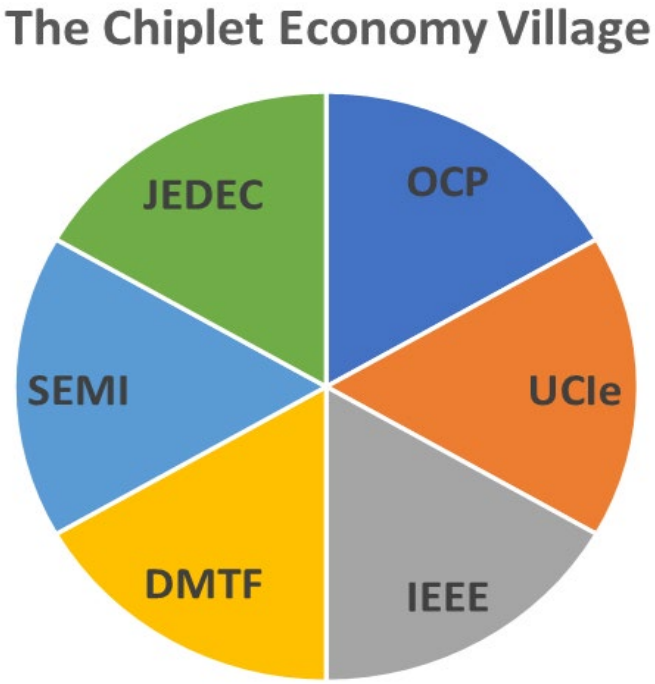


Establishing a New Open Chiplet Economy



Will take a Village

- JEDEC: Microelectronic Industry Standards
- OCP: Modularity and DC Requirements
- UCIe: Chiplet Interconnect & Market Development
- IEEE HIR: Packaging & Assembly Roadmaps
- DMTF: Device Management
- SEMI: Business Models

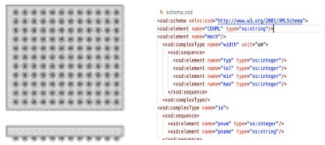


OCP Investing to establish an open Chiplet Economy

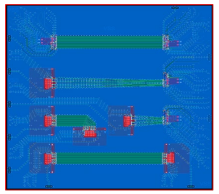
(Accelerating advanced computing)

Open Domain Specific Architecture Project

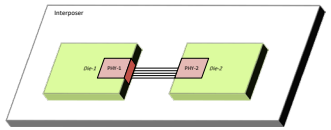
Business Workflows



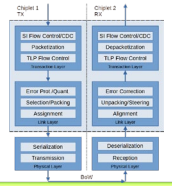
Chiplet Description Schema



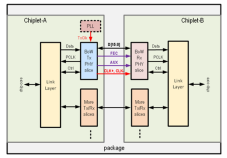
Chiplet Test Bench



Interconnect Comparison Benchmark



Logical Interconnects



Physical Interconnects

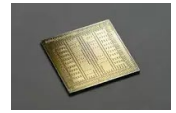
Thermal Management for SiP

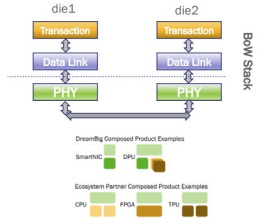
Co-packaged Optics

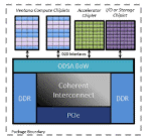
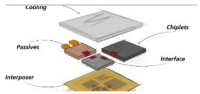
In-package Health Monitoring

ODSA Impact is Significant and Continues to Grow

- Blue Cheetah family of BoW-based D2D solutions
- eTopus/Quicklogic/Comira - BoW/FPGA/Ethernet I/O
- NXP BoW256 PHY development
- BoW PHY Interoperability Testing
- DreamBig BoW based Chiplet Platform for SmartNIC's
- D-Matrix BoW D2D Interface for Multi-Chiplet AI System
- Ventana Micro Systems RISC-V CPU using BoW
- Fraunhofer implements BoW on Samsung 5nm Technology



How YOU can get Involved

- Participate in OCP ODSA Project Workstreams
- Invest to build the Chiplet Economy
  - Chiplets, Tools, and Services

Join

- Project Mailing Lists
- Project Calls

Drive

- Project Focus
- Thought Leadership

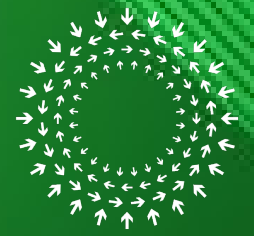
Run

- Project Leaders
- Technical Steering Committee

Contribute

- Specifications
- Products & Facilities

Learn more at opencompute.org!



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