Time Drive – Wireless Synchronization

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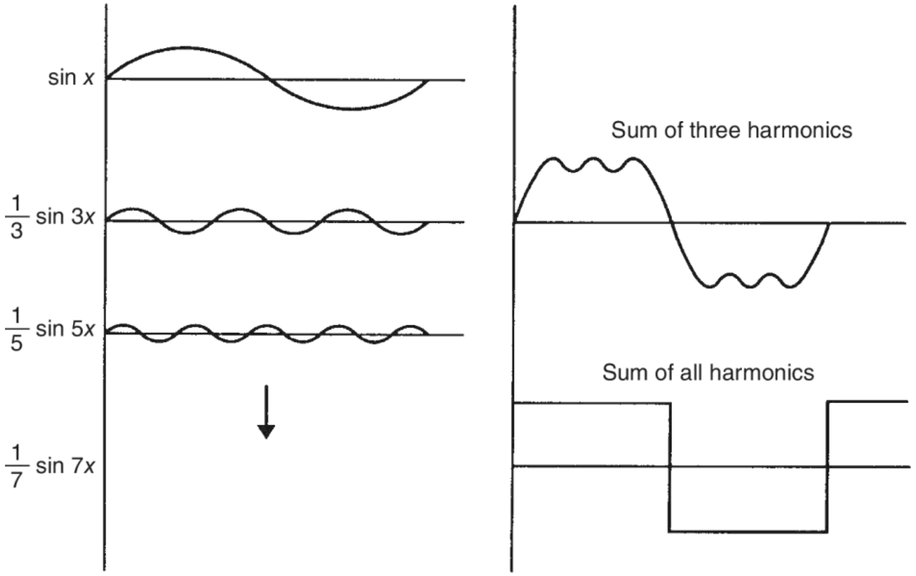
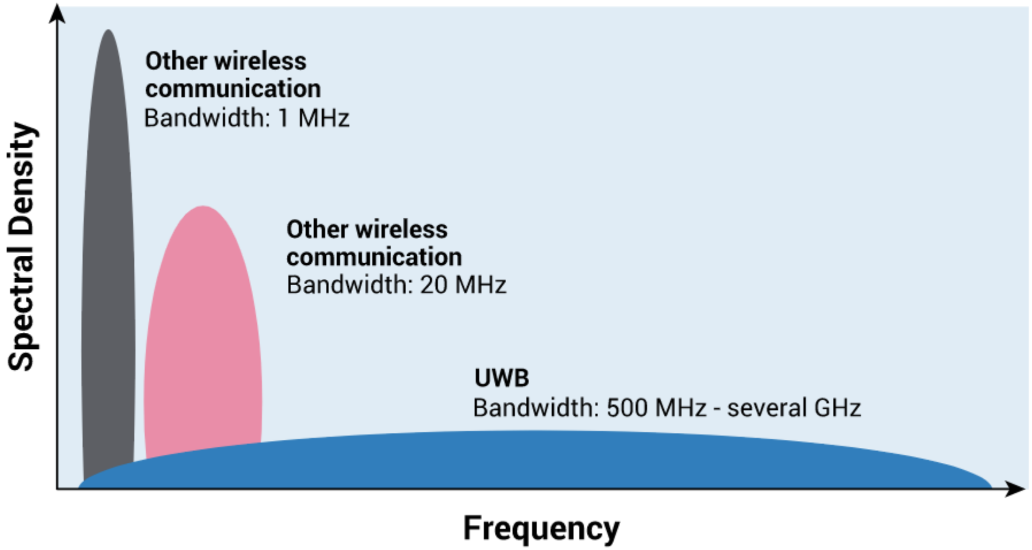
How about the last feet (Wireless)

- GNSS Time Synchronization requires antenna connection
- Wi-Fi is not the best for Time Synchronization
- UWB can be a good candidate with some modifications
- Time Card requires a PCIe slot which is not available on laptops
- Existing MAC is too big to be placed in a laptop on cell phone

How to sync end users

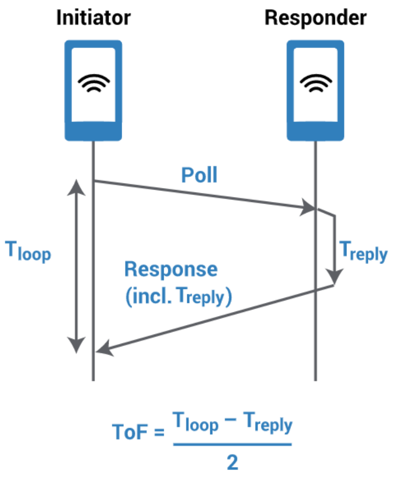
- UWB (Ultra-Wideband)
  - IEEE802.15.4-2011 / IEEE 802.15.4z-2020
  - Large bandwidth approximates ideal square wave better with sharper edges
  - Sharp edges allow precise timestamping of packet reception and transmission

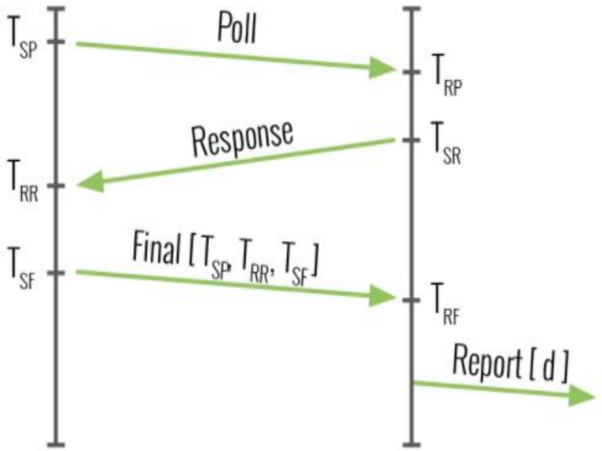




Traditional UWB application

- Ranging
  - UWB devices have a 40-bit counter running at ~64GHz , one tick ~15 ps
  - Each packet sent or received is timestamped using this counter
  - Range between devices calculated using Time of Flight * Speed of Light
  - Accuracy degrades as response time increases, each end has non-ideal clocks, so time calculations vary with clock frequency variation





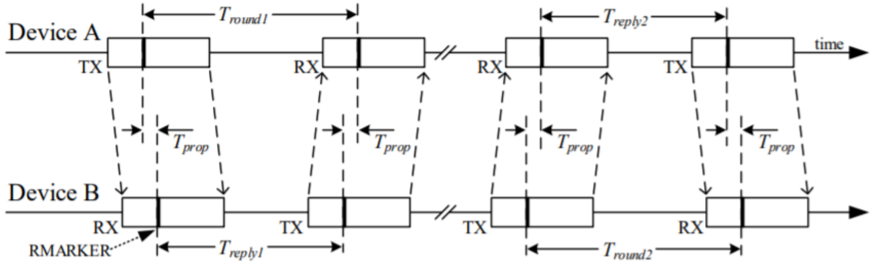
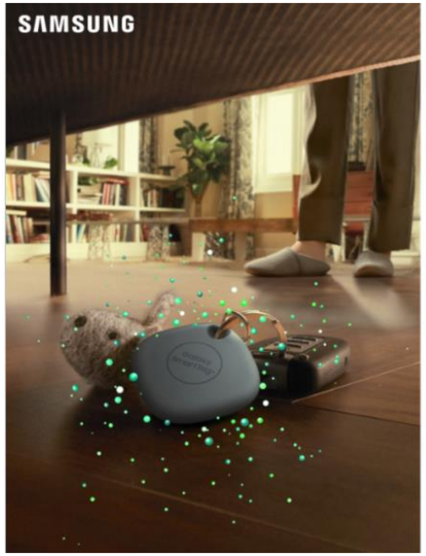


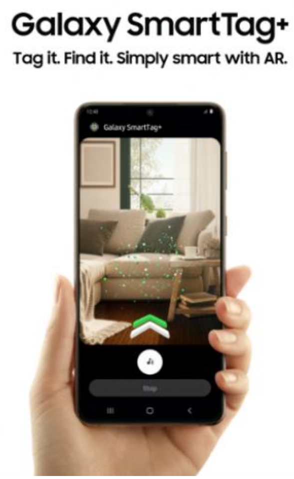
Figure 37: Double-sided two-way ranging with four messages

Commercial UWB

- Apple AirTags
  - Use UWB and BLE together to find the distance and angle to the tag from your phone

- Samsung SmartTag
  - Similar to Apple, uses UWB and BLE together with phone's camera to show you where the tag is





https://engineering.fb.com/2016/02/18/core-data/netnorad-troubleshooting-networks-via-end-to-end-probing/

User Synchronization

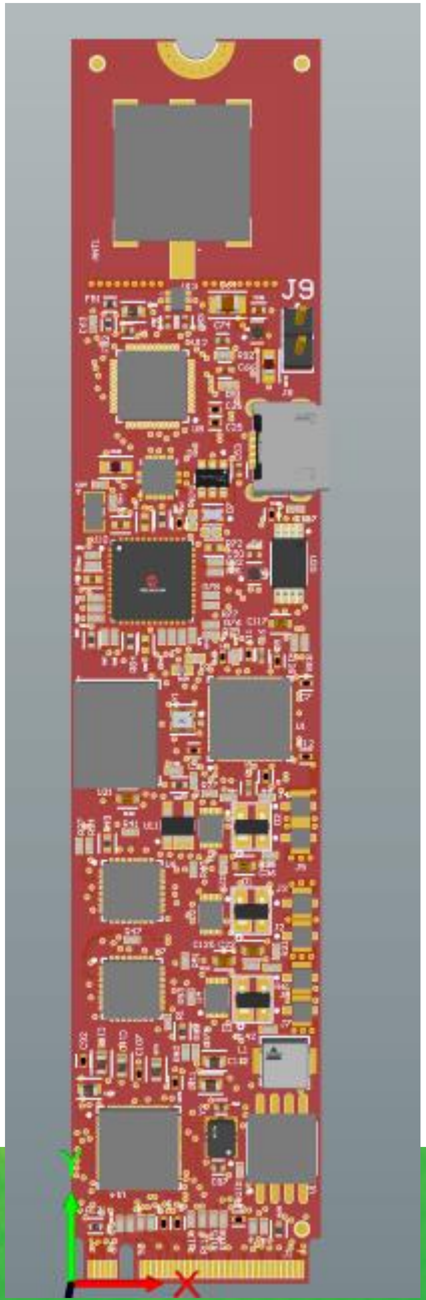
- Synchronize multiple devices to a single "gateway" with GPS
  - Provides GPS synchronization to locations without GPS reception
- Ideally, this "gateway" function would be built into Wi-Fi routers, or standalone device
  - Users could install as needed per household, synchronize every device

GPS Ultra-wideband Gateway (GUG)

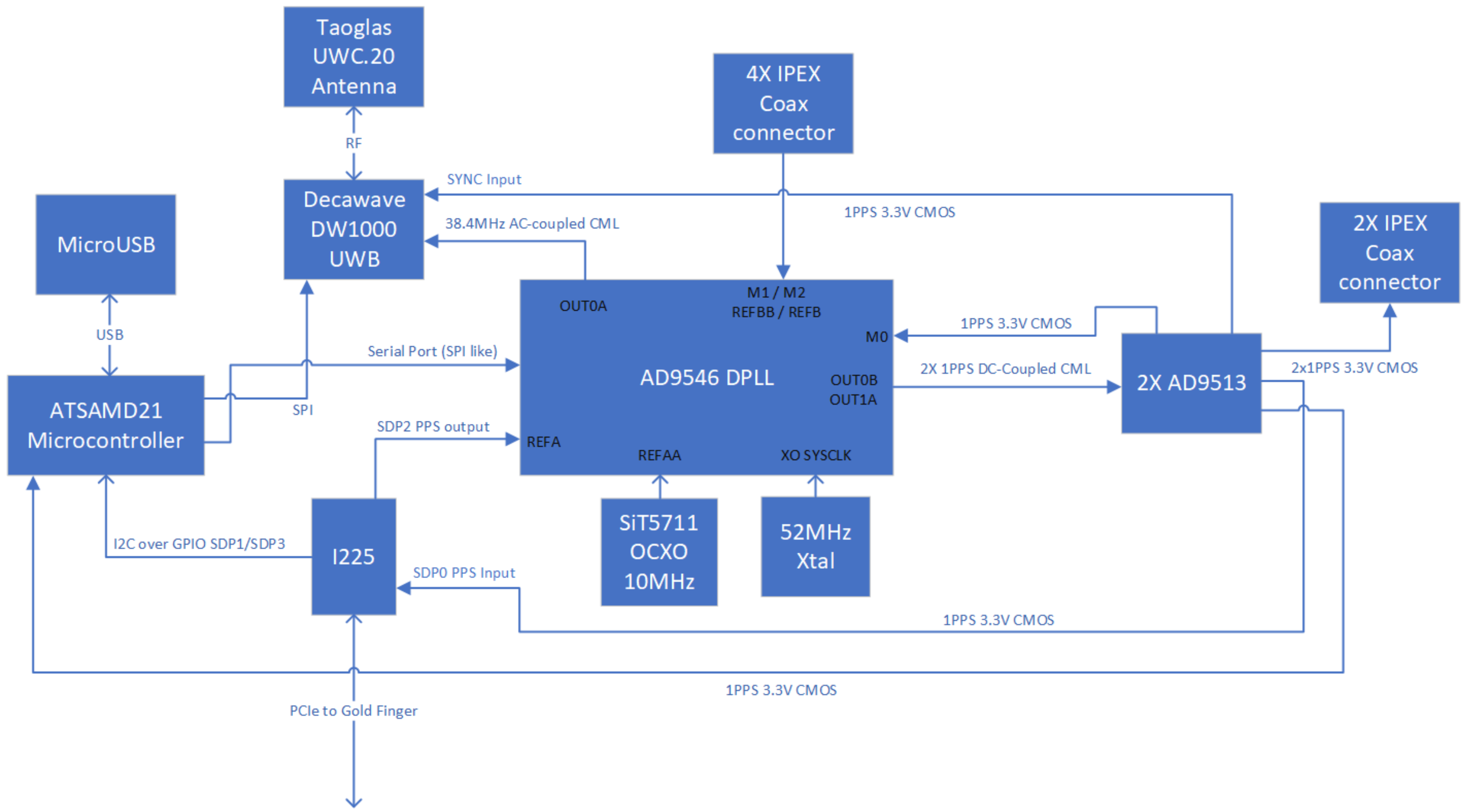
UWB Endpoint (M.2 design, Time Drive)

Time Drive

- First prototype of a UWB endpoint, M.2 formfactor
  - Intel I225 NIC chipset as PCIe endpoint
  - Decawave DW1000 as UWB chipset
  - Analog Devices AD9546 DPLL
    - Frequency and phase control, timestamping input, 1PPS outputs
  - ATSAMD21 as onboard microcontroller
  - SiT5711 OCXO for stability
- Hardware design on Time-Appliance-Project github
  - https://github.com/opencomputeproject/Time-Appliance-Project/tree/master/TimeDrive
  - Please contact us if interested in assisting in development



Time Drive Operation



Time Drive PTM

- Intel's I225 is one of the first NICs supporting PTM
- PTM is to PCIe what PTP is to Ethernet a means of synchronizing two devices via hardware Timestamping
- With PTM, Time Drive will sync the system clock with more precision than even the Time Card

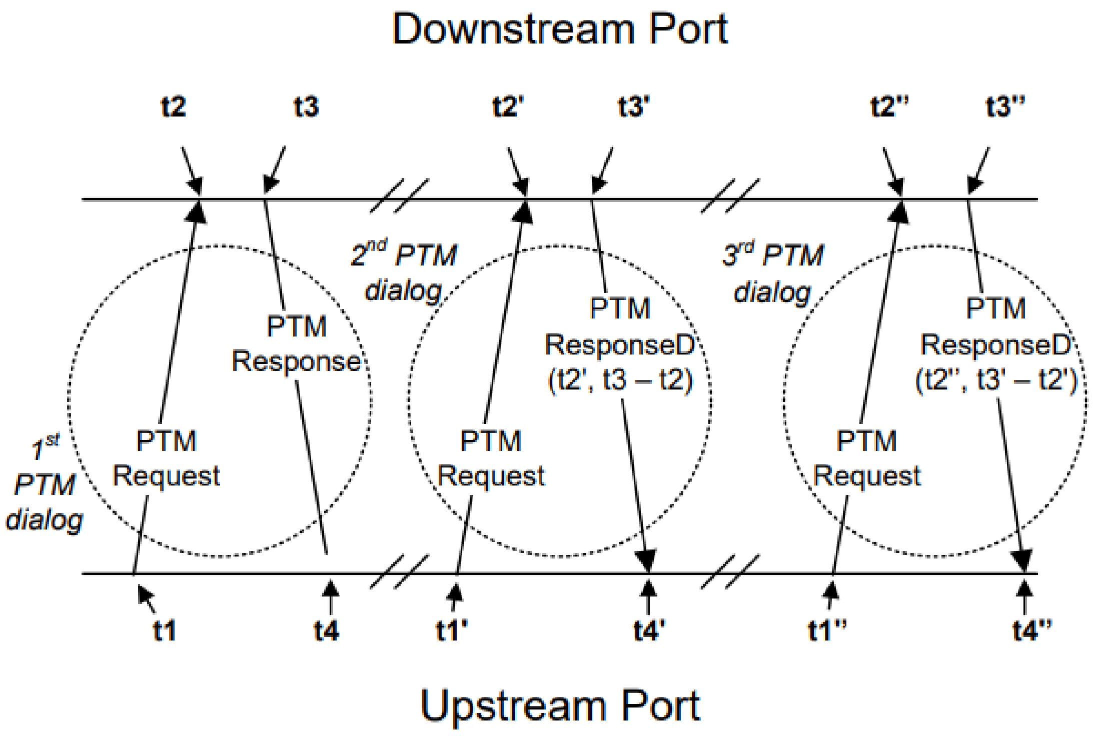
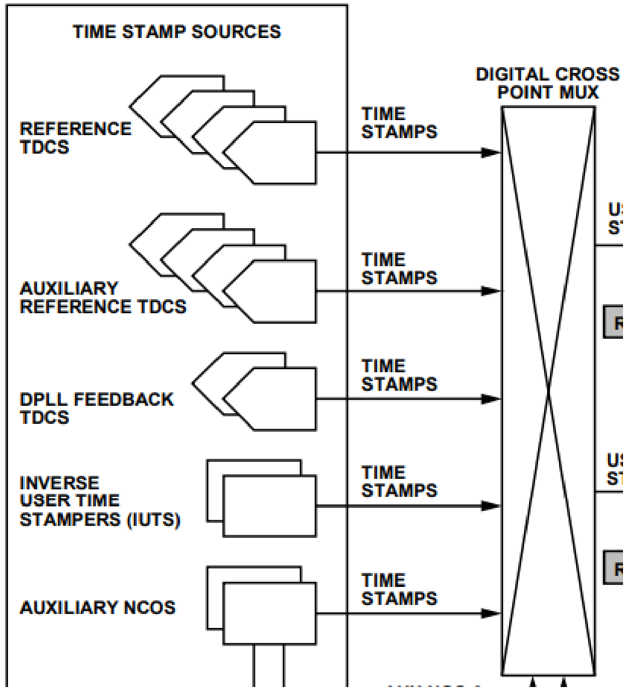


Figure 6-b: Precision Time Measurement Link Protocol

Time Drive Measurements

- AD9546, Analog Device's DPLL designed for 1588 use cases, has multiple TDCs, with up to 8 TDCs for external inputs. Time Drive exposes 4 inputs, the same as a Time Card
- Typical timestamping in FPGAs is done synchronous to the internal logic, usually either 125MHz or 200MHz , +/- 2.5ns precision
- AD9546's TDCs provide measurements well into the picosecond range, allowing for a order of magnitude more precise Timestamping



TIME TO DIGITAL CONVERTER (TDC) SPECIFICATIONS

Table 23.

Parameter	Min	Typ	Max	Unit
TDCs				
Frequency Range			200	kHz
Pulse Width	5			ns
Time Stamp Jitter				
Root Mean Square (TDC_{Jrms})		5	11	ps
Peak (TDC_{Jpk})			250	ps
Retrigger Blackout Period	4.9			µs
Start-Up Time		6		ms

USER TIME STAMPERS (UTS) SPECIFICATIONS

Table 27.

Parameter	Min	Typ	Max	Unit
LATENCY				
Fractional Seconds Format		4	6	µs
PTP Format		5	7	µs
THROUGHPUT RATE				
SCLK = 50 MHz with Address Looping			446	kSPS
SCLK = 50 MHz			324	kSPS
SCLK = 25 MHz			16	kSPS
TIME OFFSET				
Range	−29.8		+29.8	ns
Resolution		3.55		fs

Thank You

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