ACCELERATING INNOVATION THROUGH CHIPLETS
OCP/ODSA WORKSHOP

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The Case for Chiplets

"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected." [1]

Gordon E. Moore

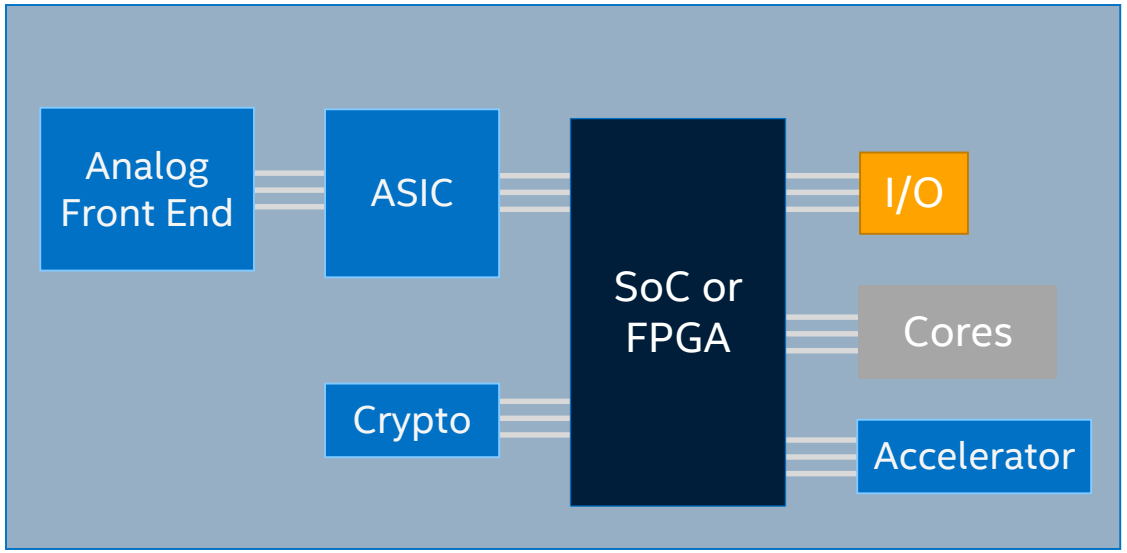
[1] 3rd Page of Moore's 1965 paper, "Cramming more components onto integrated circuits"

Why are Chiplets Now Interesting?

Heterogeneous Integration advantages (you can mix processes) → **Not New**

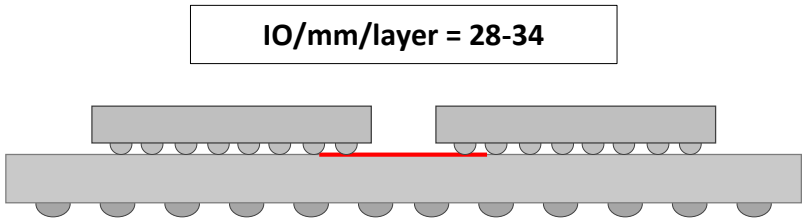
Time-to-market advantages (no need to port everything to a new node) → **Not New**

Advanced Packaging Technology → **New!**



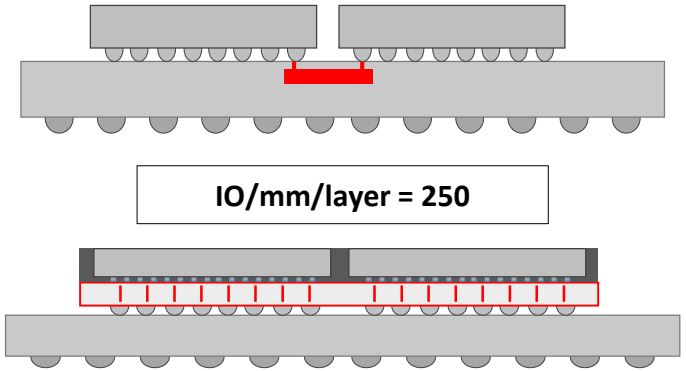
Packaging Technology

Standard Flip-Chip Packaging Technology



FCXGA, FCCSP

Advanced Packaging Technology

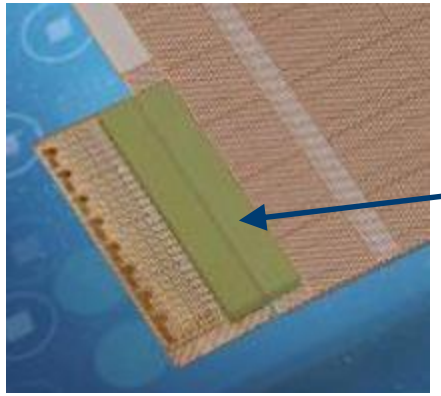


EMIB

Silicon Interposer

Advanced packaging technology provides 7-8x IO density increase

When Wires Are Free



Silicon Bridge or Interposer

- 500 wires/mm → 4,000 wires in Intel® Stratix® 10 FPGA EMIB
- Typical interposer → USD 0.0005 per wire
- Conclusion: spend very little at each end of the wire
  - *Don't spend silicon on serialization, complex SERDES, encoding schemes, I/O training, pre-emphasis or equalization*
  - *More Gbps/wire is not better when you can go wider*

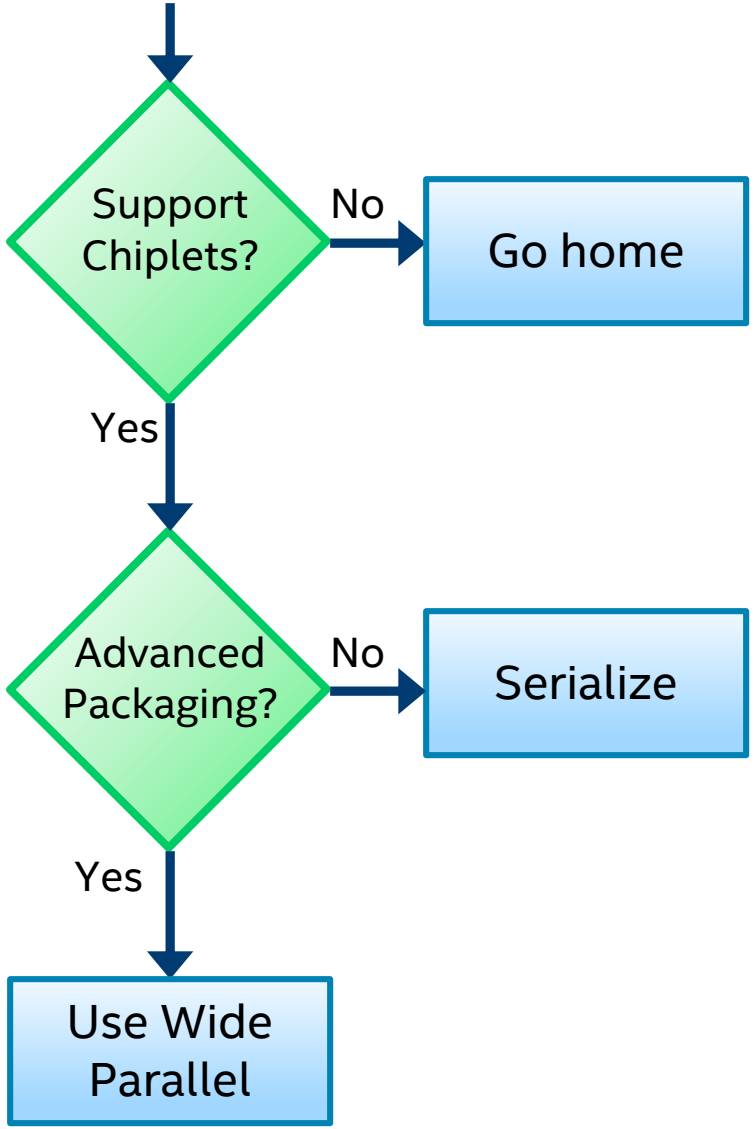
Google's FASTER Trans-Pacific Cable (2016)

- 6 fiber pairs: 12 "wires"
- Cable cost USD 300M → USD 25M per wire
- Conclusion?
  - Spend everything you can at each end of the wire!

5 trillion times more!†

Image Source: US Navy

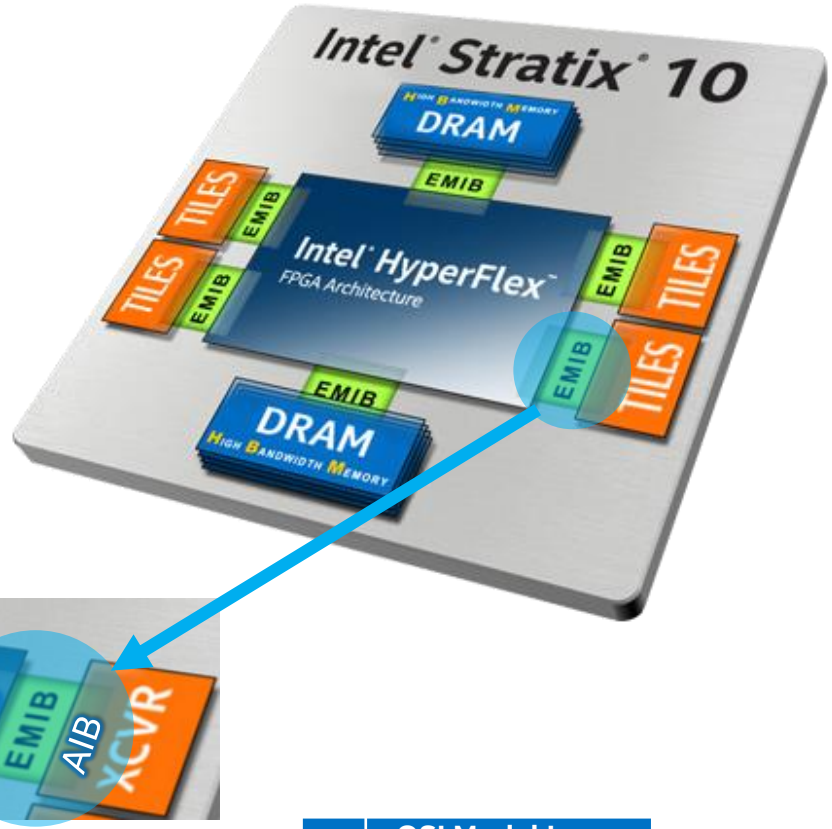
Chiplet Flowchart



AIB Die-to-Die Physical Interface

AIB: Common chiplet physical interface

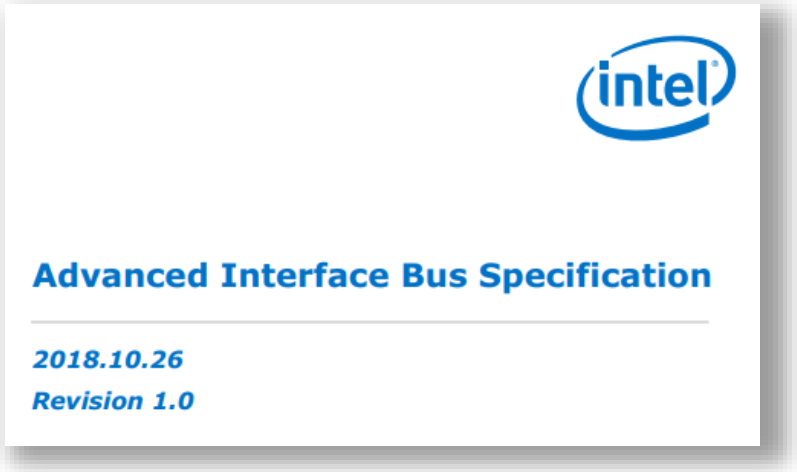
- **A**dvanced **I**nterface **B**us (AIB)
- AIB is a clock-forwarded parallel data transfer like DDR DRAM
- Advanced Packaging with a 2.5D interposer like CoWoS, or EMIB
- AIB is PHY level: OSI Layer 1
- Build protocols like AXI*-4 or PCI Express* on top of AIB



	OSI Model Layer
7	Application
6	Presentation
5	Session
4	Transport
3	Network
2	Data Link
1	Physical

AIB

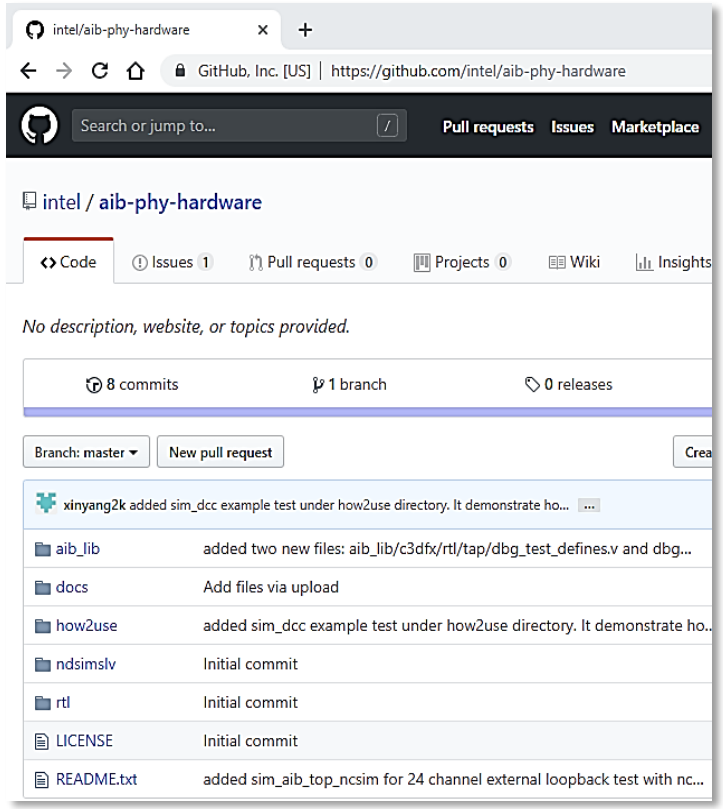
AIB Public Releases



AIB Specification Released October 2018

AIB Public Specification includes:

- Electrical specs, bump array mechanicals, data/clock/ control signal definitions, reset handshaking, JTAG reqts
- Available at https://github.com/intel/aib-phy-hardware/tree/master/docs



AIB Open Source Released January 2019

AIB Open Source on GitHub

- Register transfer level (RTL), netlists, generic cell library
- Available at https://github.com/intel/aib-phy-hardware
- Purpose: **reduce development cost**

Designing for Heterogeneous Integration: Interfaces

How to enable design for Heterogeneous Integration?

1. Reduce silicon development cost
   - Make die-to-die interface IP in your silicon technology as close to free as possible
     - AIB Spec and AIB logic design already released (see GitHub)
     - Open source AIB physical design research is in progress
2. Expand access to advanced high-density packaging (next page)

Designing for Heterogeneous Integration: Interposers

Example of Interposer Design Enablement: BroadPak

BroadPak Enabling Chiplet Integration

BroadPak is a 2.5D/3D integrator

- Over 11 years experience in 2.5D/3D design, manufacturing and SIP assembly

Design/manufacturing Services

- Silicon interposer/organic substrate Co-design, Signal/power/thermal integrity
- Silicon interposer/organic substrate manufacturing (no strings attached)
- Advanced assembly

Chiplet Management (upcoming)

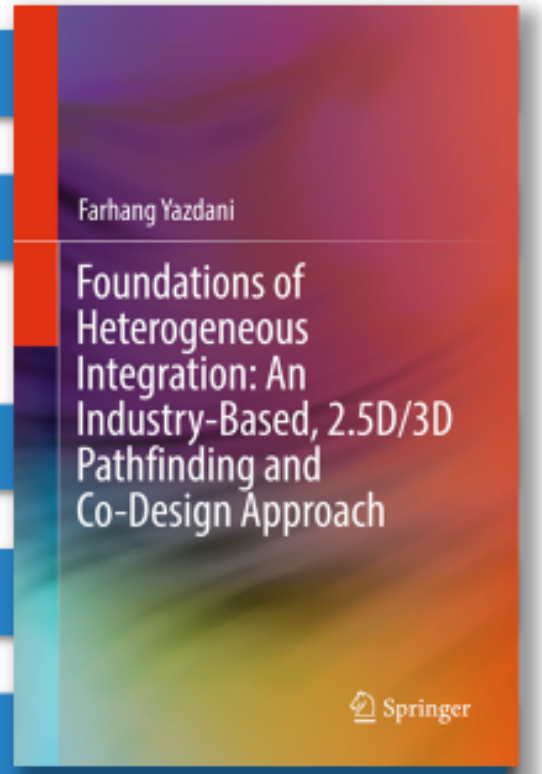
- Work with IP provider to maintain inventory of their IP Chiplet

Support

- Provide guidance and support to IP providers

Book/workshops

- To help newcomers and practicing professionals learn the foundations of Heterogeneous design
- Within 1 year, over 150 universities worldwide acquired BroadPak Book: *Foundations of Heterogeneous Integration: An Industry-Based, 2.5D/3D Pathfinding and Co-Design Approach*



BroadPak
2.5D/3D Technologies

From Farhang Yazdani, President and CTO of BroadPak

Data Rate

AIB 1.0 is 2Gbps/wire today. Why not more Gbps/wire now?

Clearly will be possible

- 112 Gbps XSR SERDES, GDDR6-like 16 Gbps/wire, others with unique signaling technology

Questions to ask:

- Cost
  - How much does it cost to build or license IP in your silicon process?
  - How much silicon area does the interface really use? (PLL, voltage regulators, independent supplies, serializers, encoders)
- Complexity
  - How do you interface your 500 MHz – 1 GHz core chiplet logic to the intellectual property (IP)?
  - How much latency from your core to the other chiplet's core?
  - How do you control training and link states?
- Why does multi-die heterogenous integration make sense now, when it didn't make sense before?
  - *Answer:* **Advanced high-density packaging is enabling technology!**

AIB Technology Drivers

Microbump spacing

- 55u is in production
- 35u would provide a nice doubling of density!

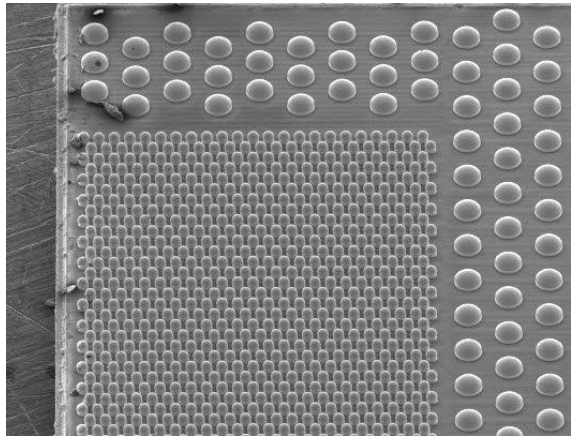
I/O voltage

- Lower voltage would drive lower energy per bit
- Compatibility with current AIB 0.9V I/O chiplets is very important

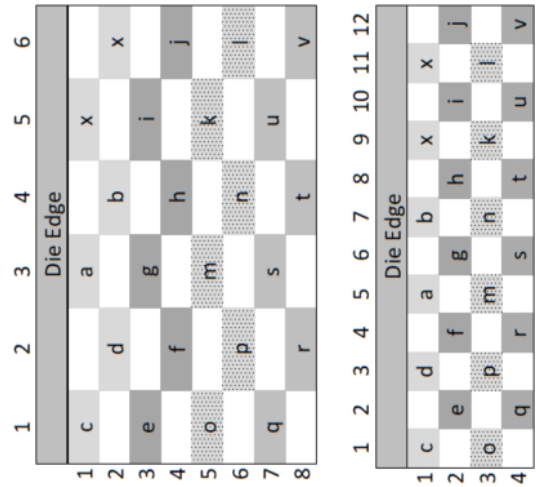
Line rate

- Very high-bandwidth applications such as direct RF sampling analog-to-digital converters (ADCs) or digital-to-analog converters (DACs) will continue to push higher bandwidth
- Doubling the data rate is feasible, watch latency

Microbump spacing + I/O voltage + line rate → **AIB 2.0**



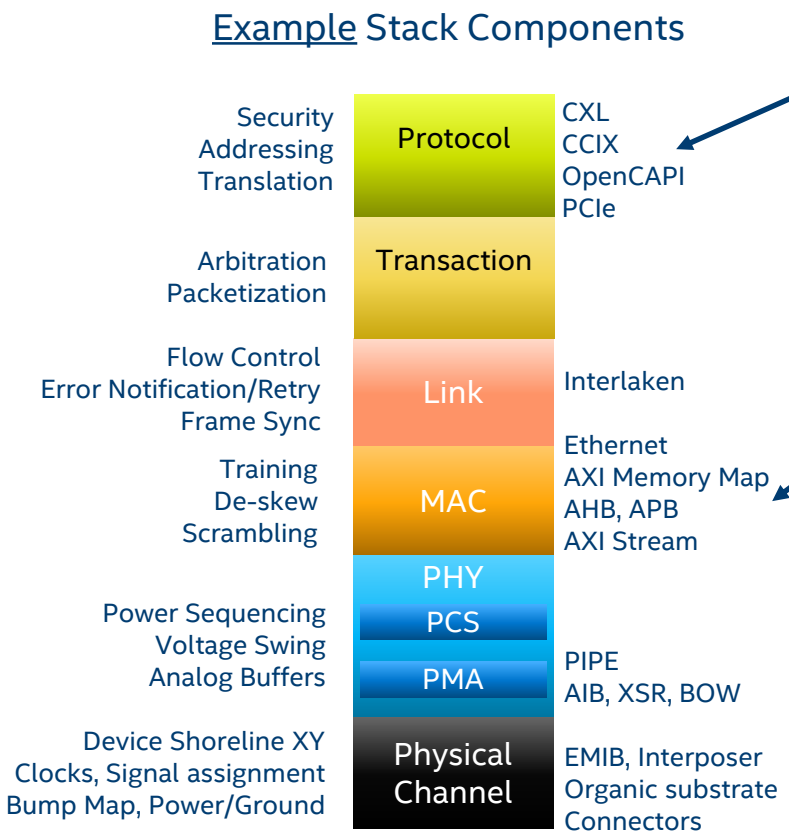
Intel® Stratix® 10 FPGA 55u microbump array



55u to 35u microbump assignment for straight-line routing compatibility

PROTOCOLS ON DIE-TO-DIE INTERFACES

Interconnect Stack



Use Cases & Applications Drive Protocols

- CPU Accelerator Use Cases
  - Software needs a coherent view of host and device attached memory

  → ***Today these accelerators are often PCI Express cards***

- Memory Mapped and Streaming Protocol Use Cases

  → ***These often come from die disaggregation (would build monolithically if it were easy)***
  - Network data (SERDES, MAC)
  - Raw or processed live sensor data
  - Control and status registers
  - Configuration, firmware loading
  - Memory controllers

Protocols On Die-to-Die Interfaces

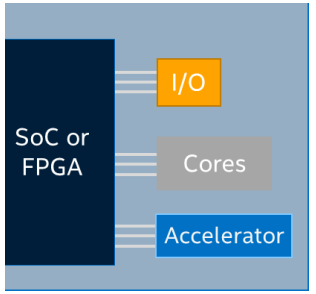
Die-to-Die products need a variety of protocols to meet product goals

- ASIC developers like their AXI*-style lightweight protocols
- Software developers want a coherent memory model

→ *One protocol will not meet all use cases and applications*

Two camps?

- Large scale integration (currently PCIe boards)
  - CXL*, CCIX*, OpenCAPI*
  - Common point at the PIPE layer: build a PIPE shim on your PHY
  - ***Consortia already in place here***
- Monolithic-like (on die module-to-module) developers
  - AXI* Streaming, AXI* MM, APB*, AHB*
  - ***This is where ODSA can help!***



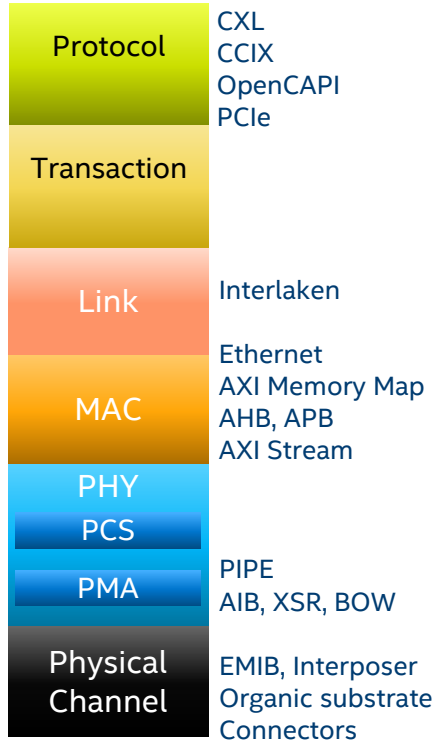
Accelerating Innovation though Chiplets

Advanced packaging is the technology enabler

Building out open source AIB IP to reduce chiplet design cost

“The ODSA aims to define an open interface such that chiplets from multiple vendors that support the interface can be assembled into domain-specific products.” – Bapi Vinnakota

→ ODSA should tackle an ASIC-like module-to-module protocol or protocols for chiplets

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