# OPEN POSSIBILITIES.



NOVEMBER 9-10, 2021

Server

## OpenChiplet: An Open Source Specification for Chiplet Marketplace

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## **Introduction to chiplets**

#### Chiplets are functional, verified, reusable physical IP blocks

Chiplets are key IP blocks taken from a homogeneous chip design and are broken out on their own, and then (re)integrated together *with packaging substrate and interconnect technologies* 



#### Google's history - Nov 2020 OCP

#### • What we see

- Disaggregation in HPC, cloud, datacenter acceleration
  - Yield, cost. Optionality of heterogeneous integration with AMS
  - End application across compute, networking, video
- Option of closed vs open
  - Fragmentation: proprietary standards and captive use cases
  - We want to accelerate open ecosystem

#### • What we would like to see (our wishlist)

- A base level framework to enable open innovation & collaboration
- A chiplet marketplace for high value-add functions
  - PCIe, HBM, SerDes (AMS)
  - Clear documentation on integration assumptions and verification quality measures
- IPs for D2D interface
  - Pre-defined IP blocks to be integrated into silicon by end user
  - Extremely high bandwidth
  - Low speed already there....lets build high speed
- How can we (as an end user) enable open ecosystem
  - Lets have an open discussion.







#### More Datapoints: ODSA Workshop - April'21

#### Analytics from the workshop

Registered: **525**, **>80** companies Attended: **319** attendees, **24** speakers (**60%+** retention rate) [The is the largest attendance of any workshop in the history of OCP]

#### Takeaways

- Given the large attendance, there is a strong interest across the industry to initiate an open chiplet ecosystem.
- Creation of an "Open Chiplet Specification" would enable the chiplet ecosystem.





#### The Need

Chicken-and-egg problem

- Chiplet suppliers won't build chiplets if there is no demand
- Customers won't use chiplets until there are suppliers with chiplets

We need to break the loop

• No "standard" which says how to build interoperable chiplets

DSA based systems of the future will need to break this loop





# A Solution



## The System Requirements ...

- Manageability: Common interfaces and software stack to ease integration.
- Security: Driving higher standards on security and making it mandatory.
- Manufacturability & Testability: Controlling the quality and reliability of chiplets since it will be an expensive failure if a single small chiplet gets assembled incorrectly.
- Physical footprint: Drive common mechanical dimensions for chiplets for ease and optimal system in package integration.

Introducing an open-source solution: OpenChiplet



## **OpenChiplet specification enables the marketplace**

Full stack: software down to packaging

Layered architecture: Include all the components necessary to build an interoperable, multisource chiplet product

Utilize standard interfaces - whether open-source or industry standards

Provide enough programmability for customization from end-user or silicon provider

Introduction : **Specification is published** on GitHub: <u>https://github.com/google/open-chiplet</u>





## Many markets



#### OpenChiplet Management Layer (OCML)

- A base layer allowing the chiplets to be managed out-of-band (D2D PHY link not operational)
  - MIPI I3C is the specified hardware interface
  - Exposes a defined SW API to access the chiplet registers
- "Plug-and-Play" discovery mechanism like PCIe/USB which allows chiplet capabilities to be identified and provisioned
- Provides operational and environmental telemetry data for real-time chiplet monitoring
- Security built-in from Day 1 (see next slide...)
- Opportunities for collaboration: Create an extensible, plug-and-play chiplet discovery and configuration API





#### OpenChiplet Security Agent (OCSA)

- Chiplets purchased on the "open-market" could be a security risk
  - Counterfeit chiplets could be introduced into the supply chain
- Chiplets present a high-value attack surface
  - IO die see all the network traffic
  - Accelerator die process user data
- Make sure we 100% trust all the system chiplets on every boot
  - "Airport model" you don't board the plane until you pass through security
- Cryptographic key exchange with a root-of-trust
  - Chiplets are never the root-of-trust
- **Opportunities for collaboration:** Scrutinize the security model and look for gaps



#### OpenChiplet Build Layer (OCBL)

- This layer specifies how to "build" the chiplet
- Covers all the common ancillary interfaces (clocks, resets, etc.)
- Specifies DFT and system level test
- Requires functional BIST to allow chiplet functionality to be checked in-situ
- Defines in-system repairability and reliability

Opportunities for collaboration: Develop all aspects of the chiplet build layer



#### OpenChiplet Physical Layer (OCPL)

- Specifies the chiplet form-factor and bump-map
- Supports silicon and organic interposers
- Standardized die areas
- Flexibility to shrink and grow to make cost-effective die
- "Mix-and-match" "Lego-style" tiling
- Common naming convention makes chiplet purchasing easier
- Thermal and Electrical requirements are also specified
- Low-power modes are expected

Opportunities for collaboration: Develop chiplet ball-maps



#### OpenChiplet Transport Layer (OCTL\*)

- The mechanism by which high-bandwidth data is moved onto the chiplet
- Transports many common silicon interfaces over D2D to the OpenChiplet
  - PIPE (PCIe, CXL, CCIX)
  - xDMII (Ethernet)
  - DFI (HBM, DDR Memory)
  - ARM system buses (AXI, CHI, APB)
  - $\circ$  ~ Video (HDMI, DisplayPort, MIPI) and video compression
  - Optical Transport (OIF-CEI)
  - Telecoms (OpenRAN)
  - Memory (SRAM, FLASH, M-RAM, ReRAM)

• **Opportunities for collaboration:** Develop a transport layer for each protocol. Support for each protocol may

need a dedicated chapter in the specification



#### OpenChiplet High Speed Layer (OCHS\*)

- Defines the high-speed or analog I/O interfaces
- Will typically leverage the protocol specifications and standards
  - NRZ, PAM4, etc.
- Could also extend to Silicon Photonics
  - optical to/from the chiplet
- Could also cover non-obvious use cases into consumer applications using analog I/O
  - Wireless transceivers: e.g. Bluetooth/WiFi chiplets
  - Analogue sensors and transducers: DACs, ADCs, thermal, ultra-sonic,
  - Biometric interfaces: fingerprint, ...

Opportunities for collaboration: Create innovative chiplet use-case concepts



## **Example: Next generation system**

- Three accelerator die (CPUs, ML, Video Encoder), connected to a common hub, the System Controller
  - Spec diagram. Lots of system missing.
- Two IO chiplets providing high-speed IOs or analog I/O
- System Controller acts as the Security Agent root
  - The root authenticates and enumerates the OpenChiplets present in the SIP via I3C



#### CALL TO ACTION

- Lots of opportunity to innovate and collaborate
- Invite stakeholders throughout the silicon and systems supply chain to work together in making the standard robust





## Thank you!

