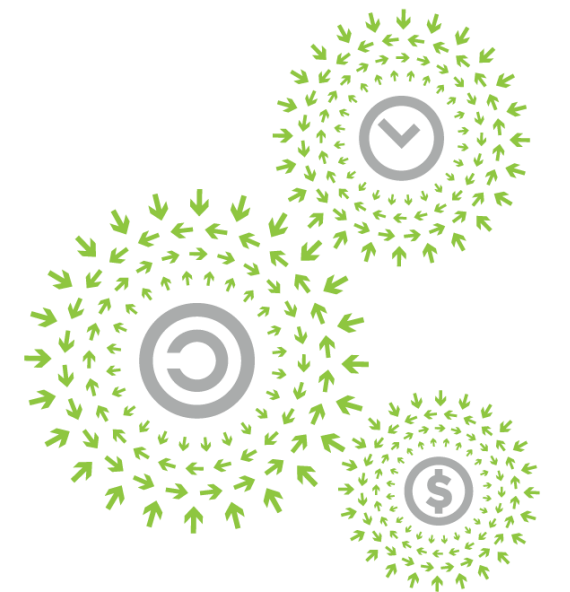# Datacenter-ready
Secure Control Module
for Open Accelerator Infrastructure (**OAI-SCM**)

SERVER

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OPEN PLATINUM™

OCP REGIONAL SUMMIT

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Modular Building Block Architecture (MBA)

- Clearly defined physical dimensions, power, cooling, management, and input/output ports

- Module interoperability in various **OAI** Systems

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- Clearly defined physical dimensions, power, cooling, management, and input/output ports

- Module interoperability in various OAI Systems

- **MBA** is a _Catalyst_ for interoperable _Innovation_!

OAI-SCM Facilitates MBA

- A datacenter-ready secure control module for OAI

- **OAI-SCM** streamlines the design and deployment of OAI Modules for Hyperscale Datacenters

OAI-SCM Facilitates MBA

- A datacenter-ready secure control module for OAI

- *OAI-SCM* streamlines the design and deployment of OAI Modules into Hyperscale Datacenters

- Drives a common and Secure Monitoring, Control, and Remote Debug for various OAI Modules and Systems (firmware, diagnostic tools, manufacturing tools, at-scale remote debug)

OAI-SCM Tenets

- Modular, Interoperable: Clear delineation of **OAI-SCM** from the rest of the OAI System via a standard Interface (**OAI-SCI**)

- OAI Modules are stateless

- OAI-SCM holds control bits secured via a Root of Trust Chip (RoT) and Chains of Trust

- OAI-SCM provides a common datacenter interface (1GE, BMC, RoT, …)

- Flexible Architecture for modular implementation

- Flexible form factors while maintaining the same interface (OAI-SCI)

- A common set of SCM circuitry and logic may reside on Host Interface Board (OAI-HIB)

- The same firmware

- The same look and feel

The Datacenter-ready Secure Control Module for OAI
(OAI-SCM)

&

The Datacenter-ready Secure Control Interface
(OAI-SCI)

Standalone OAI-SCM

- Remote Control, Management, and Debug at Cloud-scale

- Receives Power (12V, 3.3V Stand-by, …) over OAI-SCI from the PDB or the HIB

- Includes:

    The main PowerEn, PowerGood, and Reset functions for power-up and power-down sequences

    BMC for OAI-level monitoring, control, diagnostics, and remote debug and for Rack Management Interface

    FAN/PSU/HIB/PDB/UBB/OAM/Chassis/Module Control

    Realtime Clock (RTC) and its battery

    RoT and TPM for Security (attestation for all firmware and programmable devices)

    Flash Devices for infrastructure-level FW controlled by RoT (OAM maintains its own FW and provides attestation to RoT)

    Clearly defined JTAG and I^{2}C Trees

    Front-IO (**LEDs,** {**RJ45**: 1GE for BMC}, {**RJ45**: Presence/PowerEn/Throttle Control}, {**RJ45**: 1GE for Connection Manager})

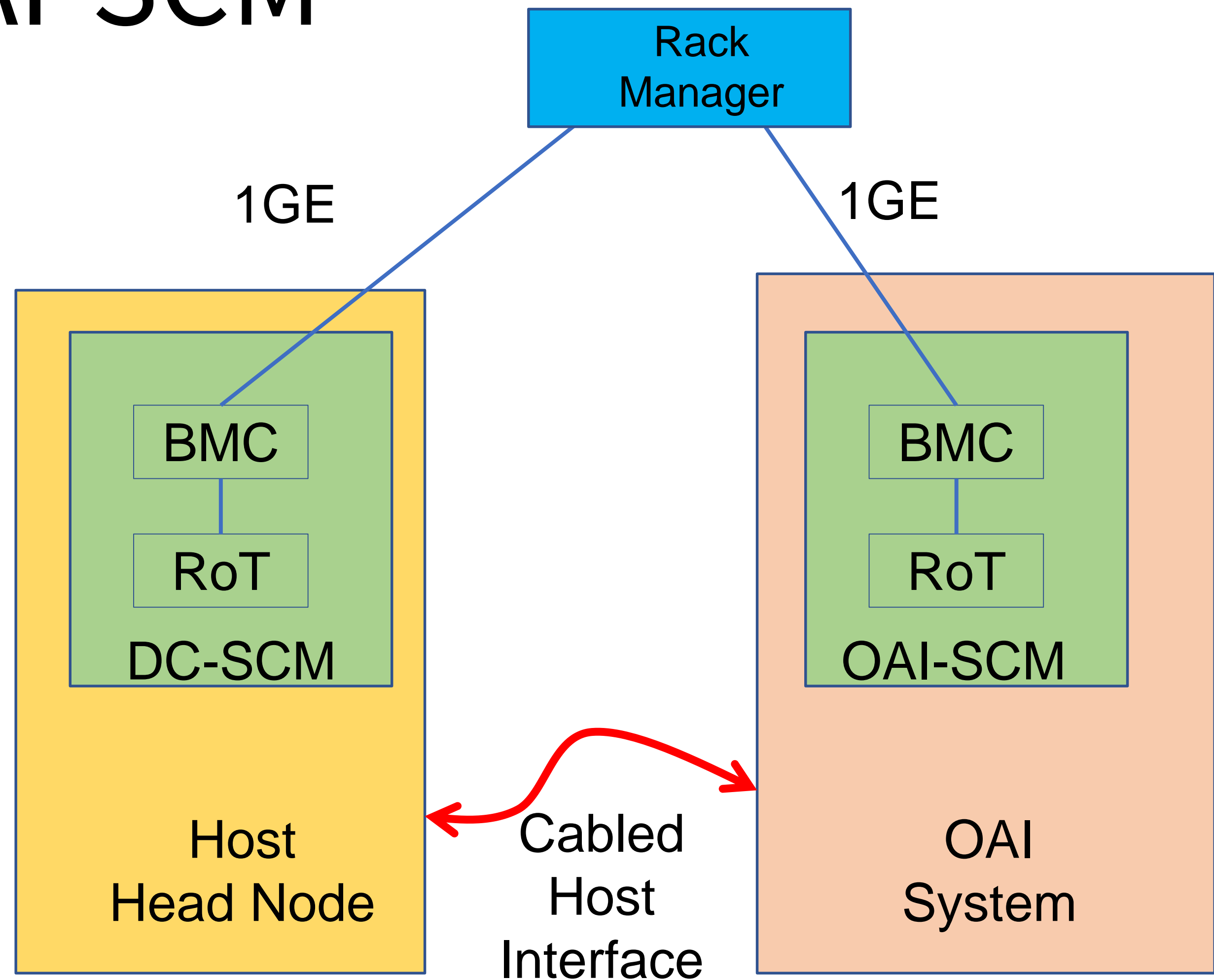# OAI Host Interfaces

Accommodating various implementations:

- Disaggregated Host
- Integrated Host
- Multi-UBB or Multi-Host OAI Systems

Host DC-SCM and OAI-SCM
(Disaggregated Host)

- The Host and the OAI System will have their own independent set of BMC and RoT chip

Rack Manager

1GE

1GE

BMC

RoT

DC-SCM

Host
Head Node

BMC

RoT

OAI-SCM

OAI
System

Cabled
Host
Interface

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Disaggregated Host-to-OAI Interface (draft)
via a Re-timer Card in a PCIe Slot

| Signal Name	Pin Cnt.(MB1)	Direction	Function
Host interface x16 Diff.	32	BI	For host interface x 16 signal
SMCLK/SMDAT	2	BI	Host BMC to OAM system BMC
Bifur_ID0	1	OUT	To host for host interface bifurcation
Bifur_ID1	1	OUT	To host for host interface bifurcation
Present Pin	1	OUT	Cable present for MB, PD on baseboard, PU on Re-timer card to IO EXT
100M CLK	2	IN	Host interface 100M CLK(From host's CLK Gen)
WarmRST	1	IN	warm reset from host
host interface Reset	1	IN	if it's PCIe, then PCIe RST
Diff. reference GND			
USB	2	BI	USB from host to OAM system BMC
Accel_PWR_EN	1	IN	From host SYS_PWRGD, to enble Accel system power
Accel_PWRGOOD	1	OUT	Accel system pwrgd back to host

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Host DC-SCM and OAI-SCM
(Integrated Host)

- BMC and RoT of the Integrated Host extend management, control, and security to the whole OAI System
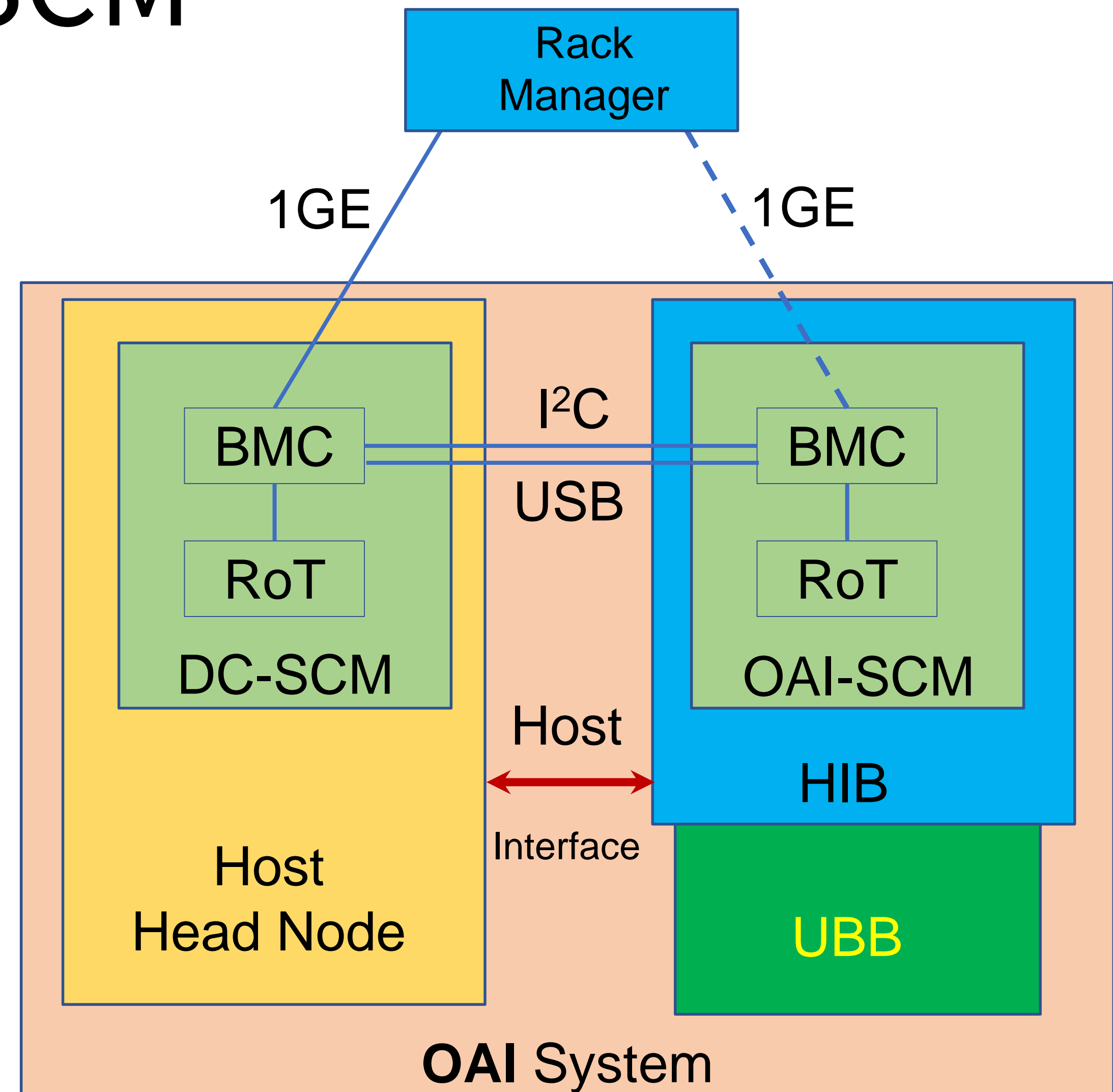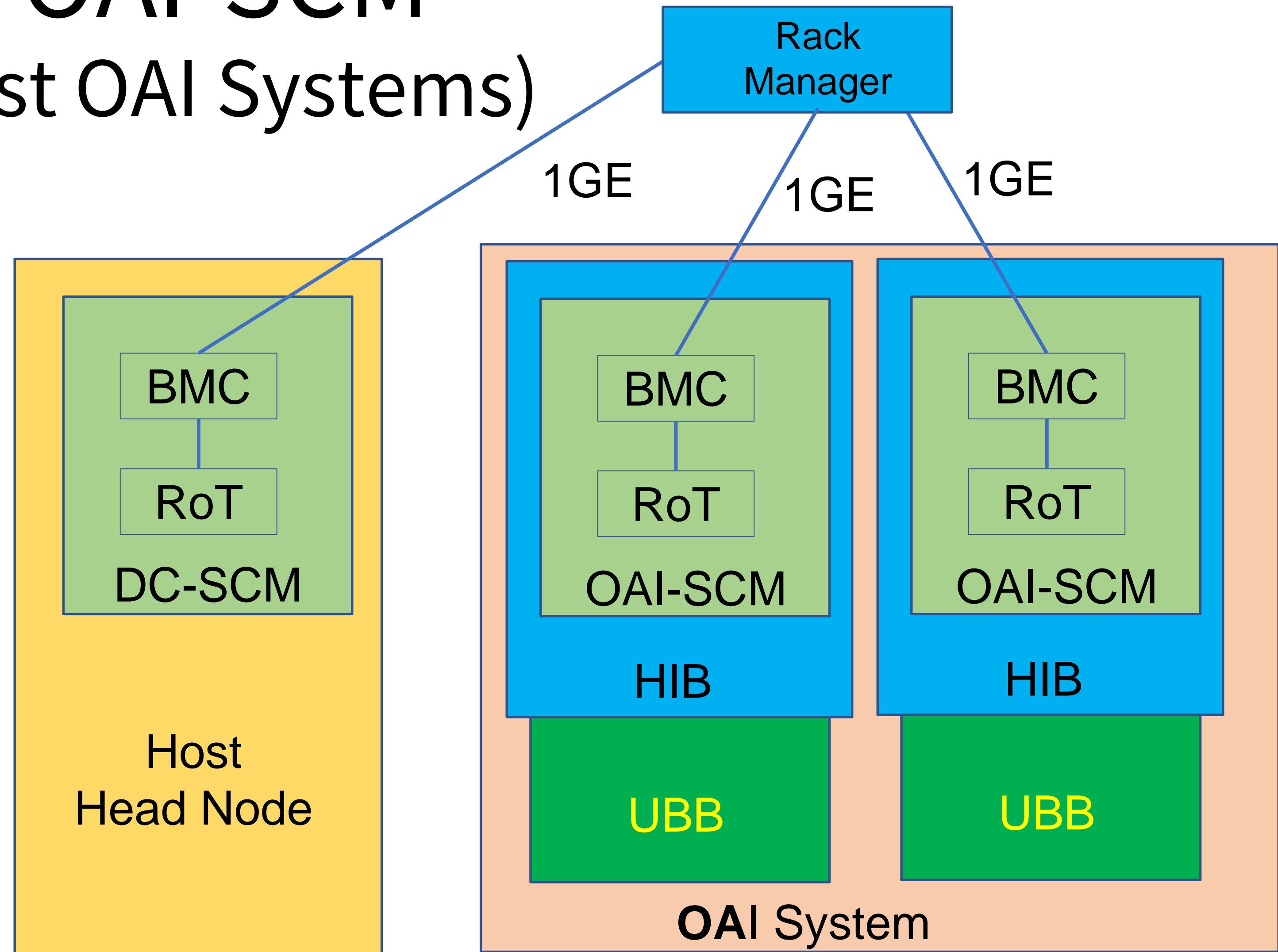
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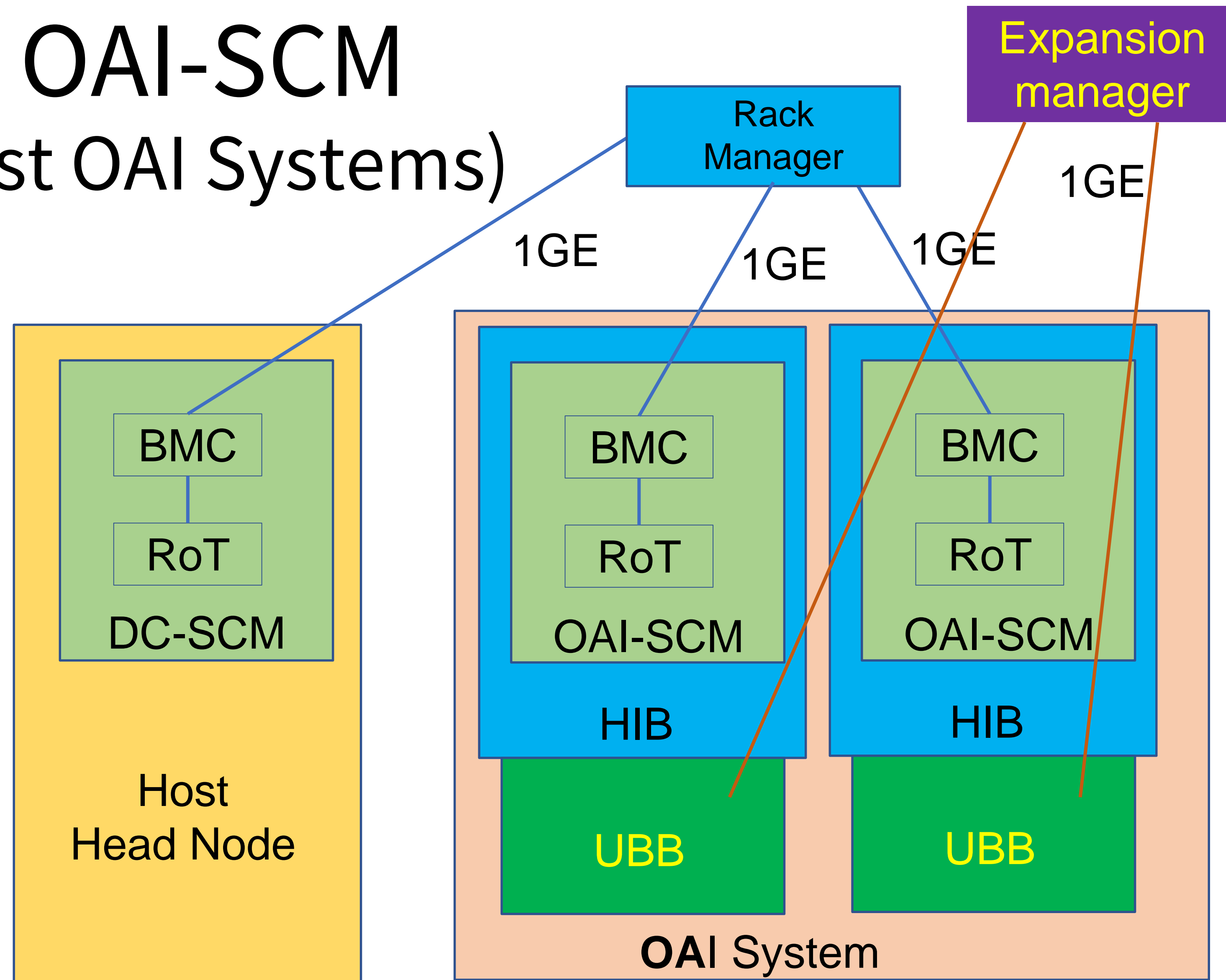
- Expansion Manager to control Expansion Ports
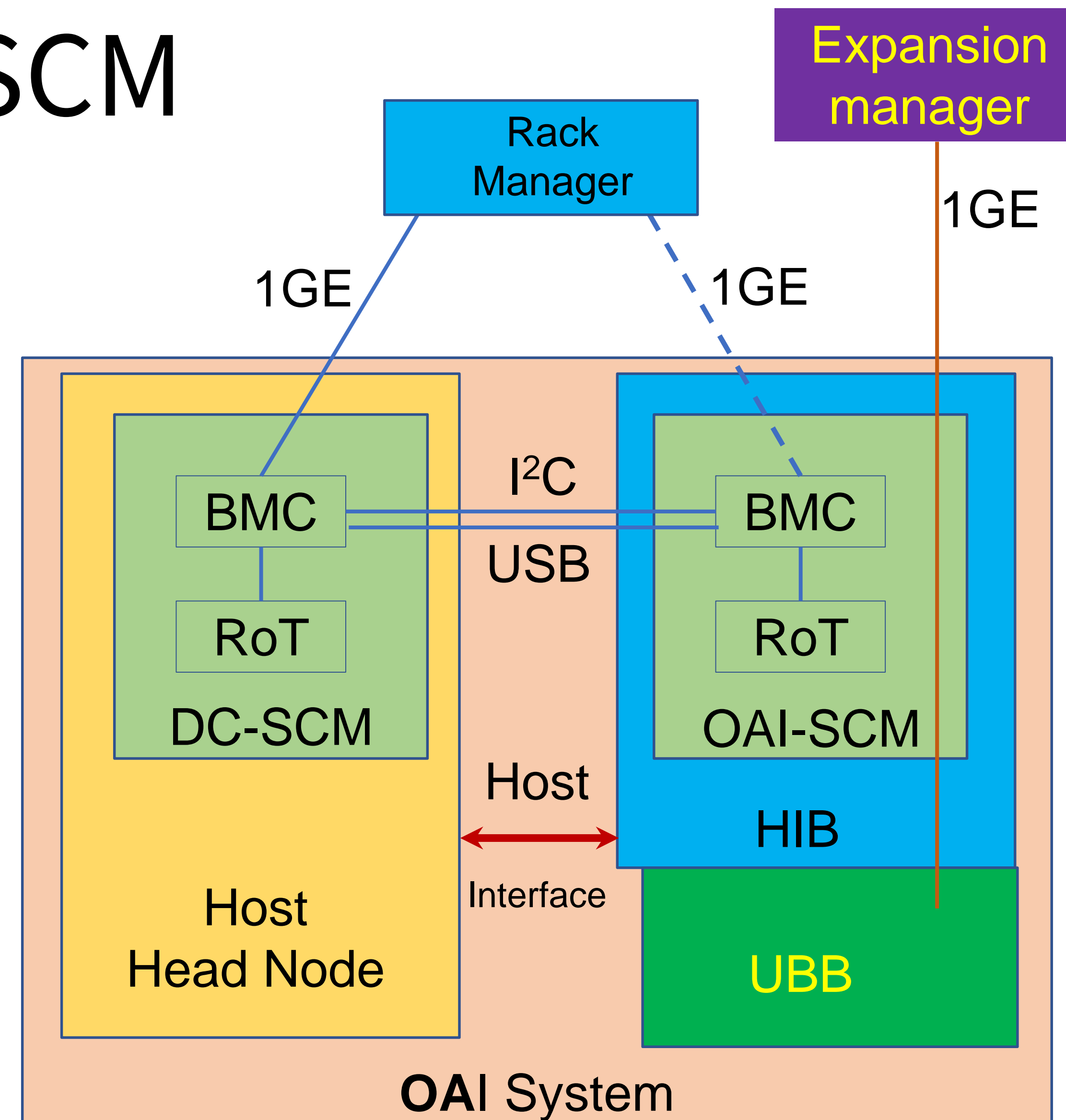
Host DC-SCM and OAI-SCM
(multi-UBB or multi-Host OAI Systems)

- Consolidated power/cooling for the OAI System

- Independent BMC/RoT

- Each UBB/HIB will have its own BMC/RoT

Rack Manager

1GE   1GE   1GE

Host Head Node
- BMC
- RoT
- DC-SCM

OAI System

OAI-SCM
- BMC
- RoT

HIB

UBB

OAI-SCM
- BMC
- RoT

HIB

UBB

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Rack Manager

Expansion manager

1GE 1GE 1GE 1GE

BMC

RoT

DC-SCM

Host
Head Node

BMC

RoT

OAI-SCM

HIB

UBB

BMC

RoT

OAI-SCM

HIB

UBB

OAI System

Power Enable, Power Good, Reset# Sequence

1. OAI-SCM provides Presence# to and receives Chassis_PowerEn and Throttle signals from the Rack Manager (Chassis_PowerEn controls all DC Power including Standby power)

2. OAI-SCM Asserts Power_En to Modules such as UBB

3. Every Module enables its VRs, HSCs, etc..

4. The output all VRs, HSCs, etc. reflect Module_OK

5. Based on all Modules Okay, SCM drives OAI_PowerGood

6. Clocks/PLLs stabilize

7. Later, SCM negates OAI_Reset# to allow OAMs etc. to run

The BMC of SCM may choose to hold OAI in Reset#, to negate PowerGood, or not to assert Power_En based on Firmware etc.

Power Enable, Power Good, Reset#
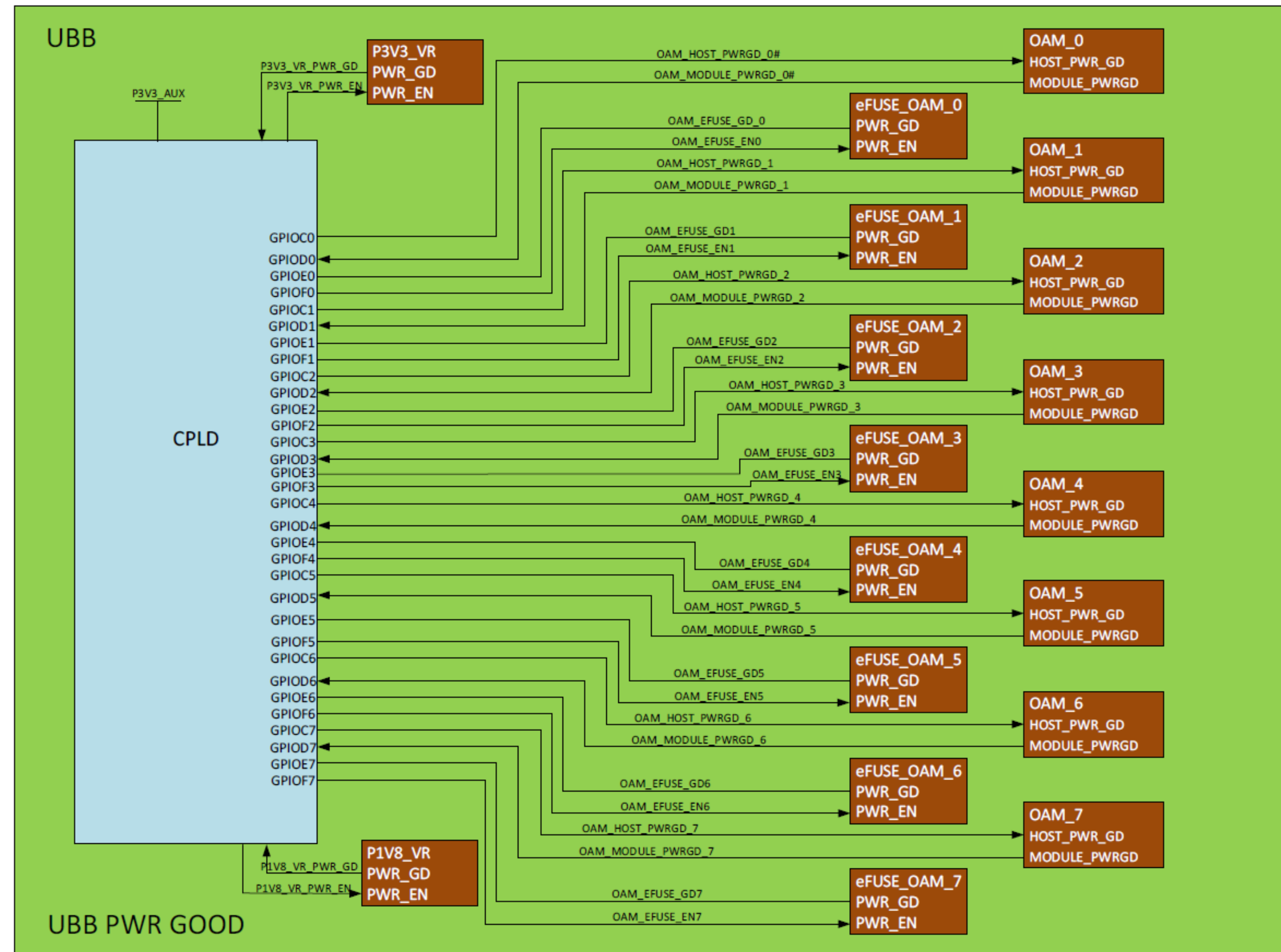
OAI-SCM Interface (OAI-SCI)

- Receives Power Rails

- Controls Power UP and Power Down Sequences of OAI Modules

- Controls PowerGood, SystemHardReset# (clears sticky bits), and WarmReset# (resets state machines, but preserves error status registers)

- JTAG to control devices on HIB and UBB

- I^2C to control devices on HIB, UBB, and other OAI Modules

- UBB/OAM Power Brake control

- Critical Signals such as ThermTrip#

- Communications (UART, I^2C, ...)

- Pin-reducing sGPIO (LD, CLK, Di, Do) between SCM/HIB CPLD and UBB CPLD
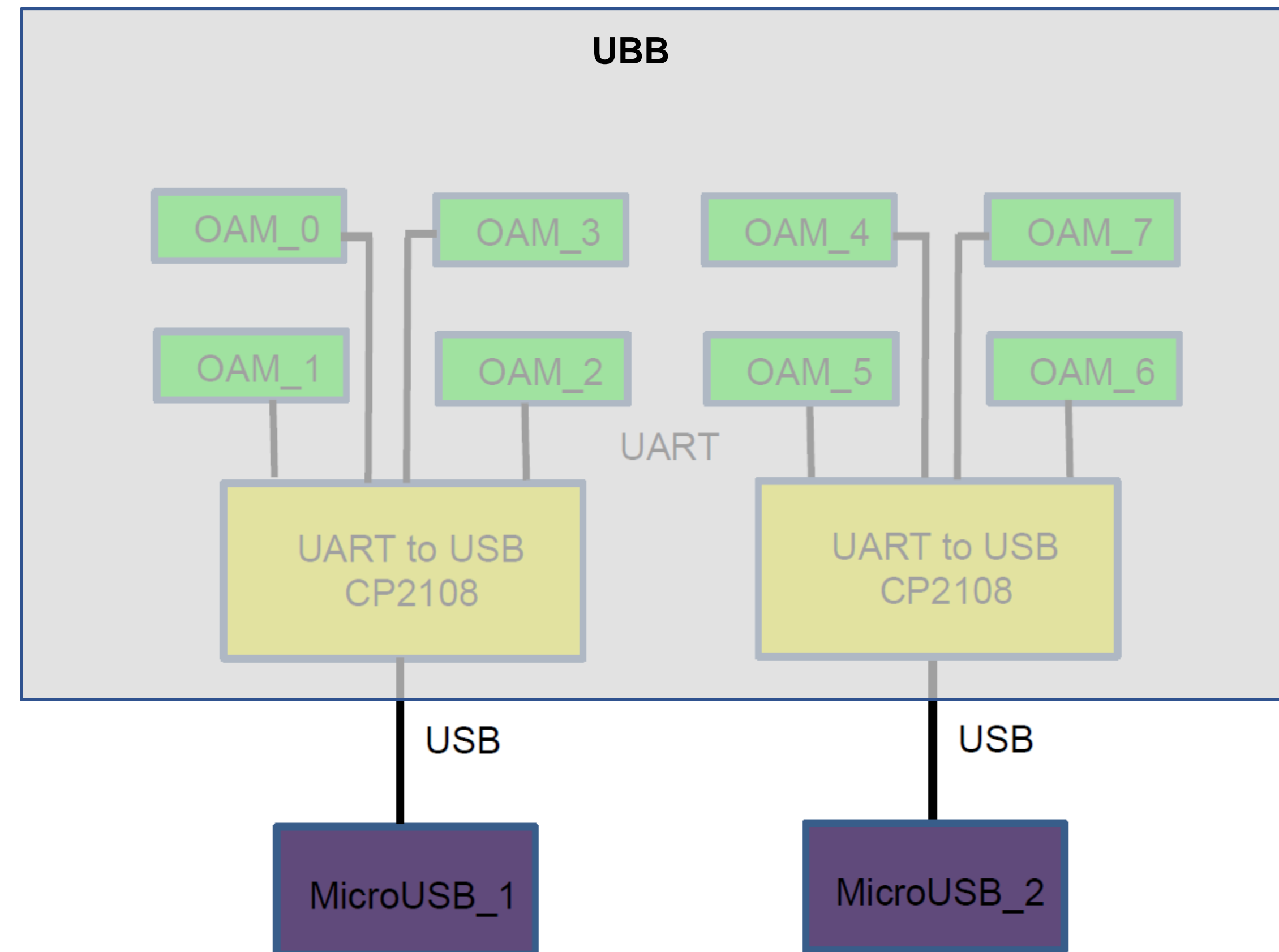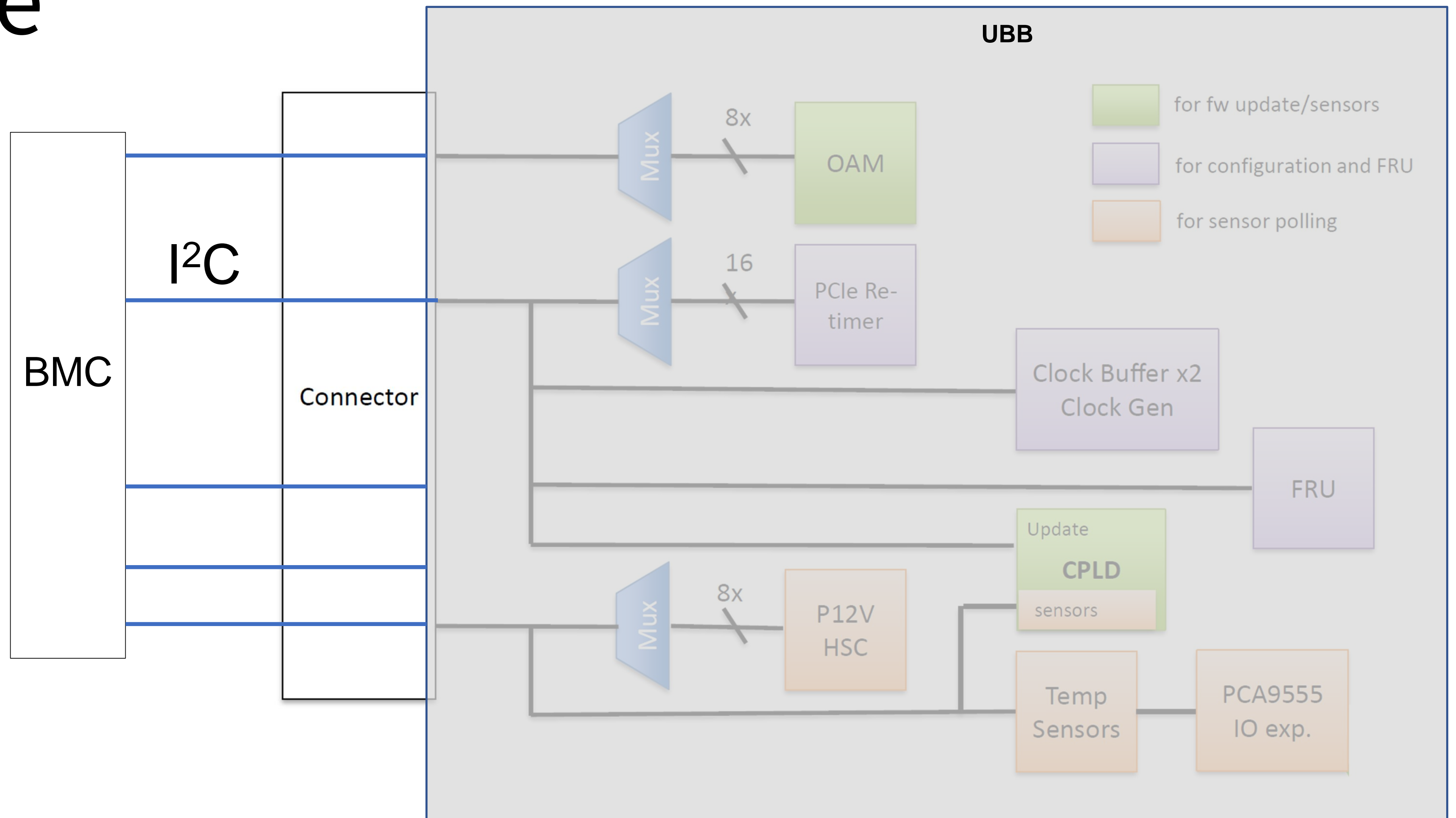
Pin Reduction via sGPIO
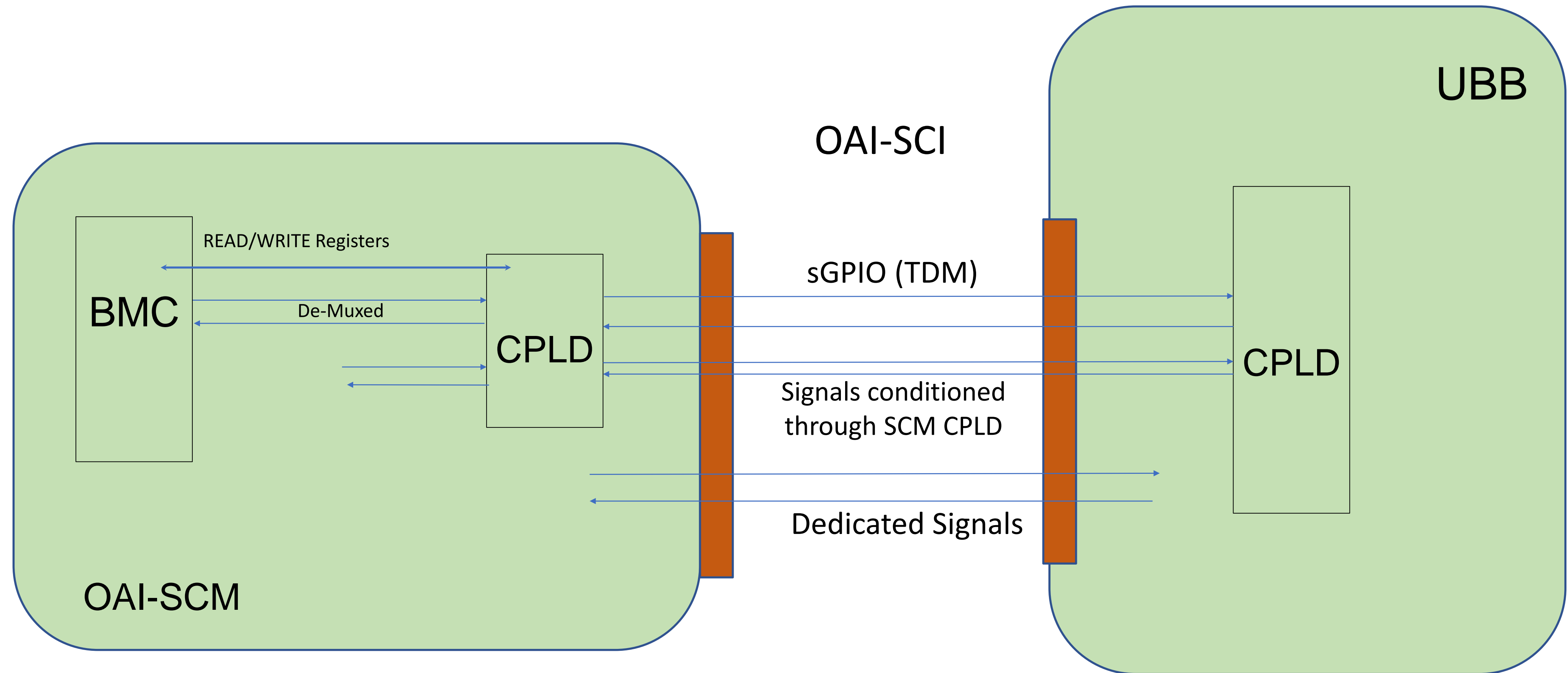
JTAG Tree
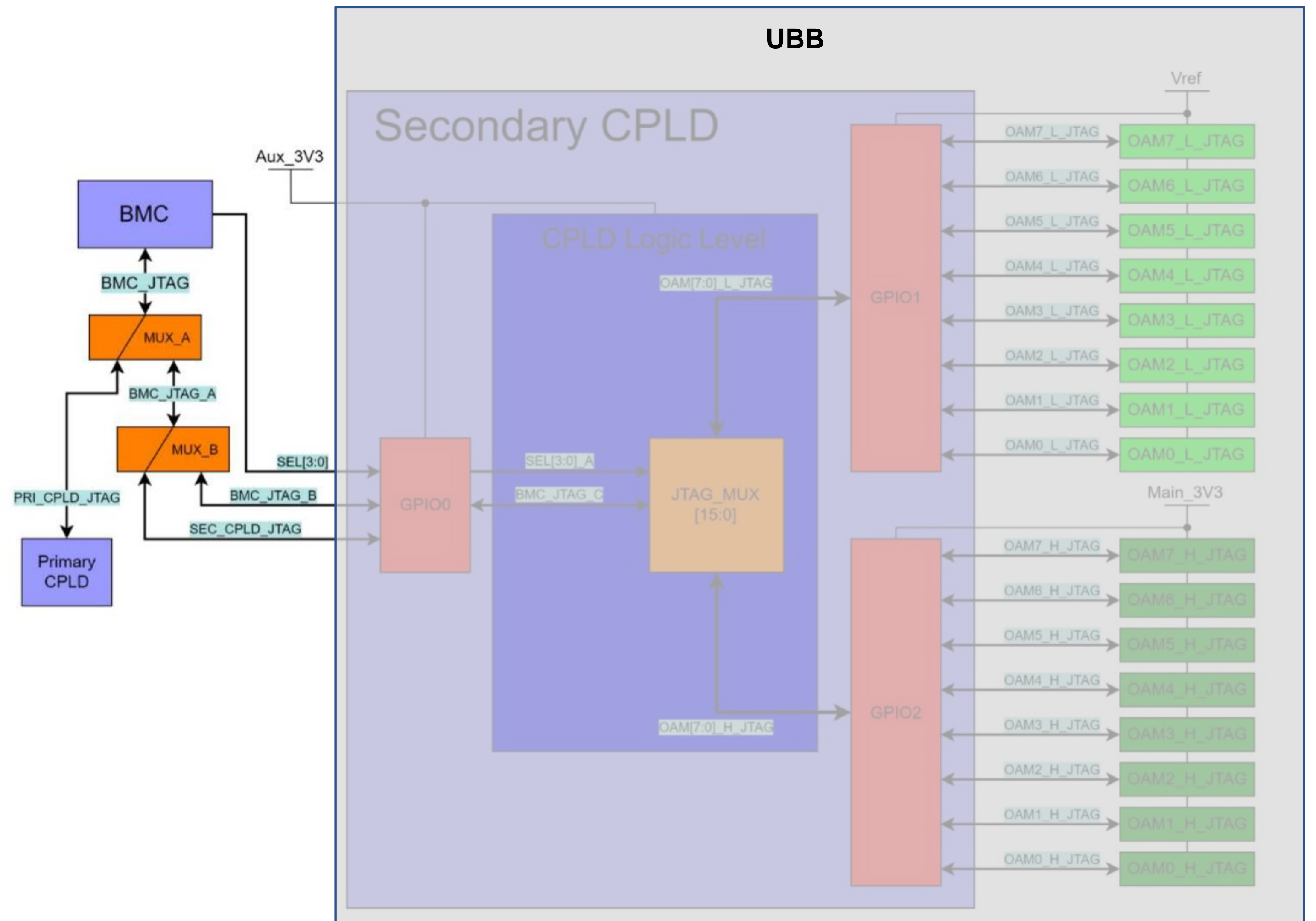
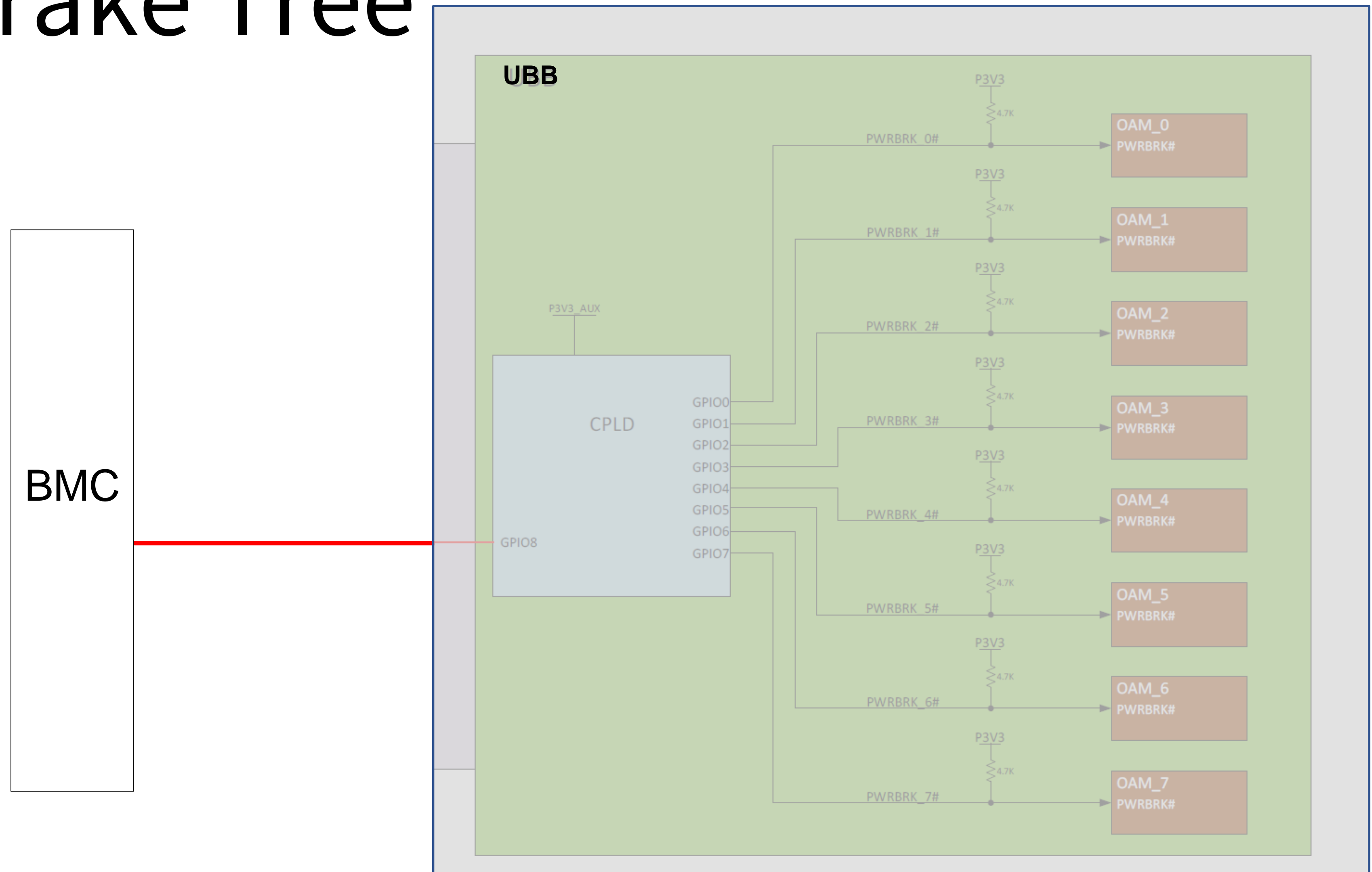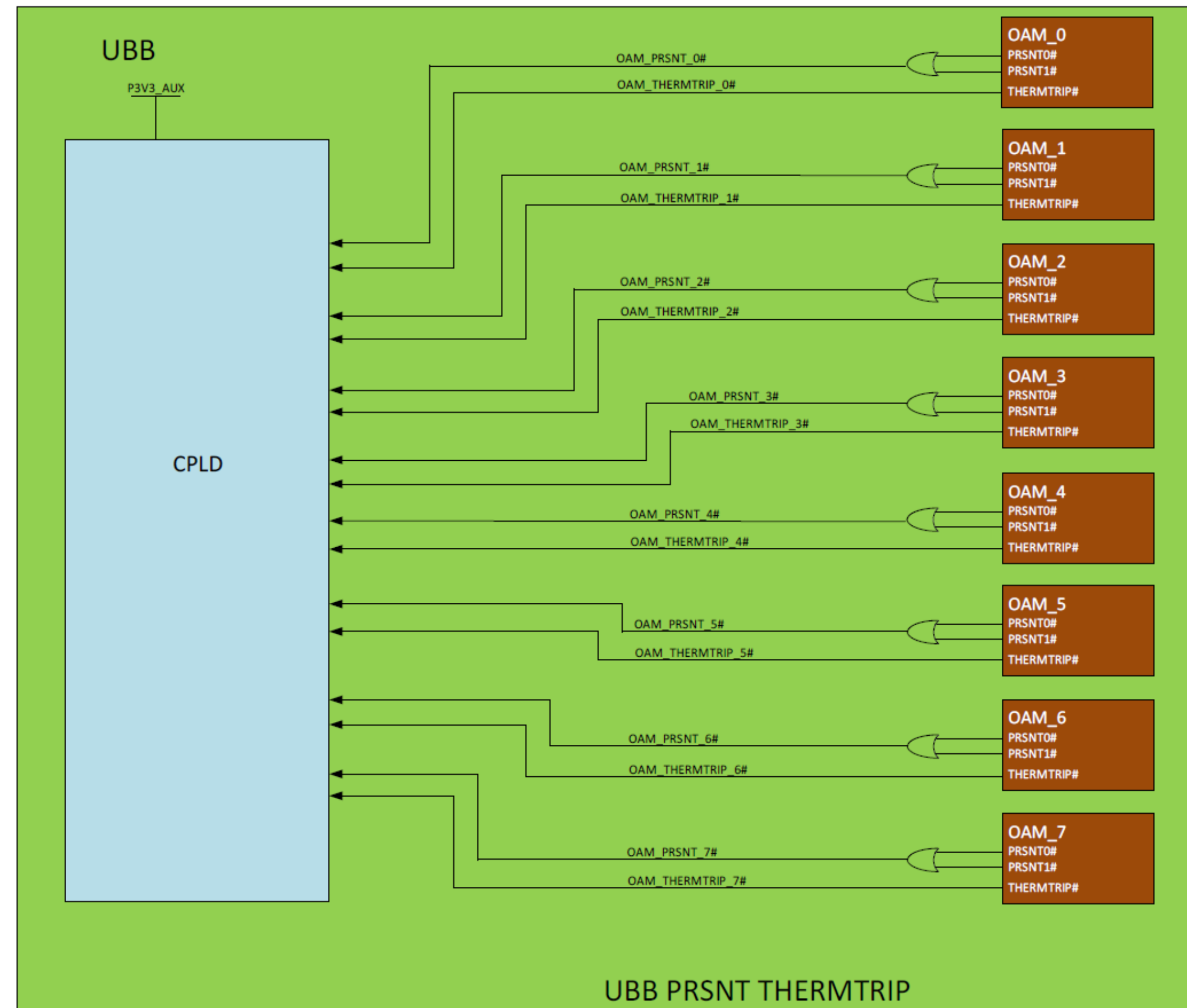# USB Ports (for OAM Debug via UART– not for production)

I^{2}C Tree

Power Brake Tree

OAM Presence# and ThermTrip#

Summary:

MBA is a *Catalyst* for interoperable *Innovation*!

- Clearly defining physical dimensions, power, cooling, management, and input/output ports enables Module interoperability in various OAI Systems

OAI-SCM facilitates Modular Building Block Architecture

- As a datacenter-ready secure control module for OAI, ***OAI-SCM*** streamlines the design and deployment of OAI Modules for Hyperscale Datacenters by driving a common and Secure Monitoring, Control, and Remote Debug for various OAI Modules and Systems (firmware, diagnostic tools, manufacturing tools, at-scale remote debug)

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Call to Action

Design your OAI System with OAI-SCM in mind

Make your solution Datacenter-Ready!

Join the effort to enhance OAI

https://www.opencompute.org/wiki/Server/OAI

Presenter

Siamak Tavallaei is a Principal Architect at Microsoft Azure, co-chair of OCP Server Project, and co-chair of CXL Technical Task Force. Collaborating with industry partners, he drives several initiatives in research, design, and deployment of hardware for Microsoft's cloud-scale services at Azure. He is interested in Big Compute, Big Data, and Artificial Intelligence solutions based on distributed, heterogeneous, accelerated, and energy-efficient computing. His current focus is the optimization of large-scale, mega-datacenters for general-purpose computing and accelerated, tightly-connected, problem-solving machines built on collaborative designs of secure, hardware, software, and management.