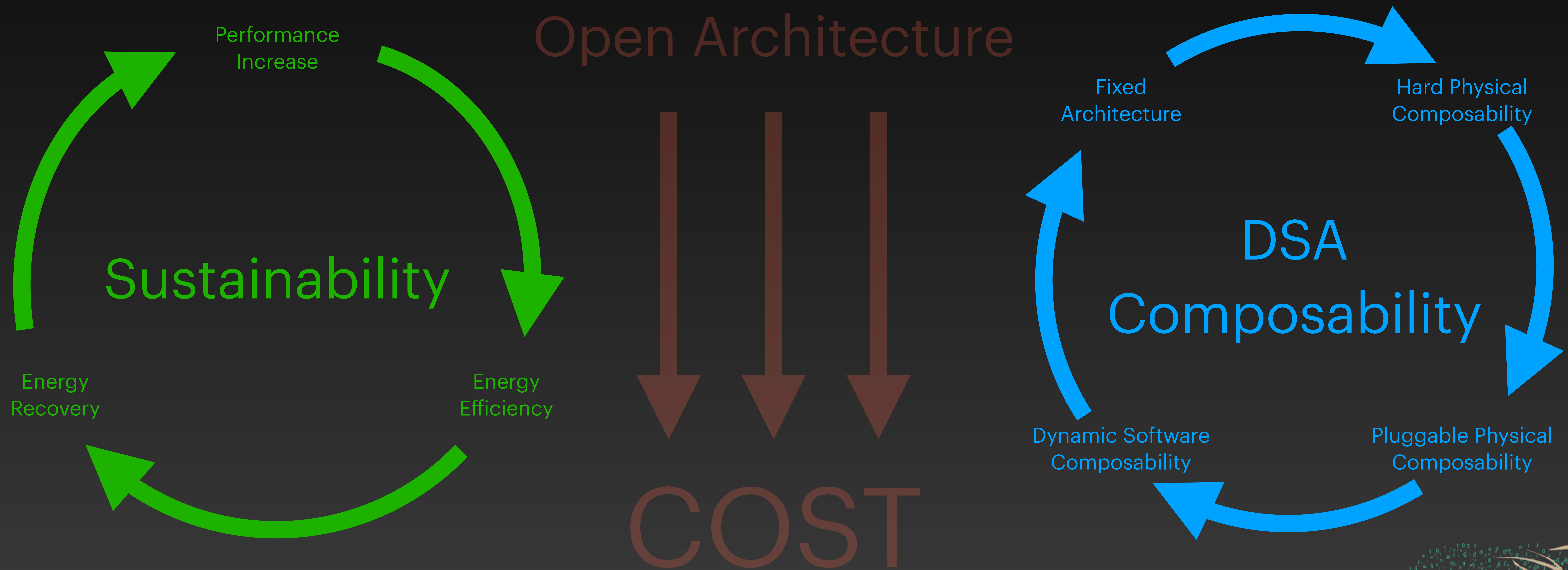
Redefining Computing Architecture Boundaries with Off Package Chiplets

An Energy Centric Computing Perspective

Allan Cantle - 6/16/2022

What's driving Computing Architecture

Power & Cost Efficient Domain Specific Architectures, DSA

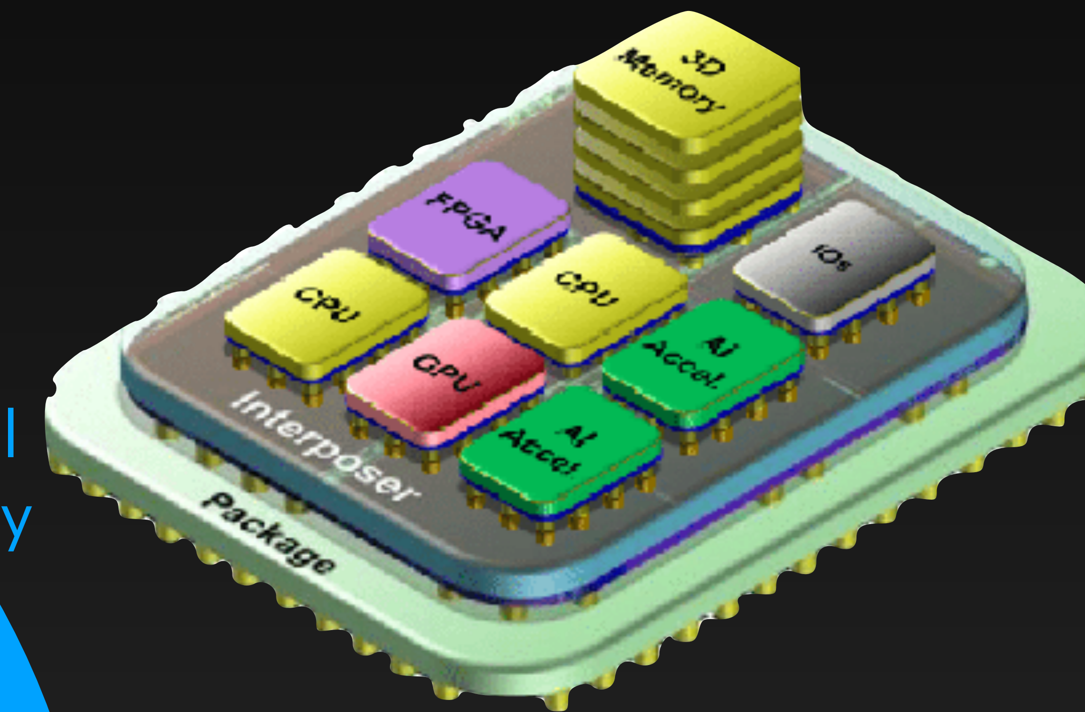


What's driving Computing Architecture

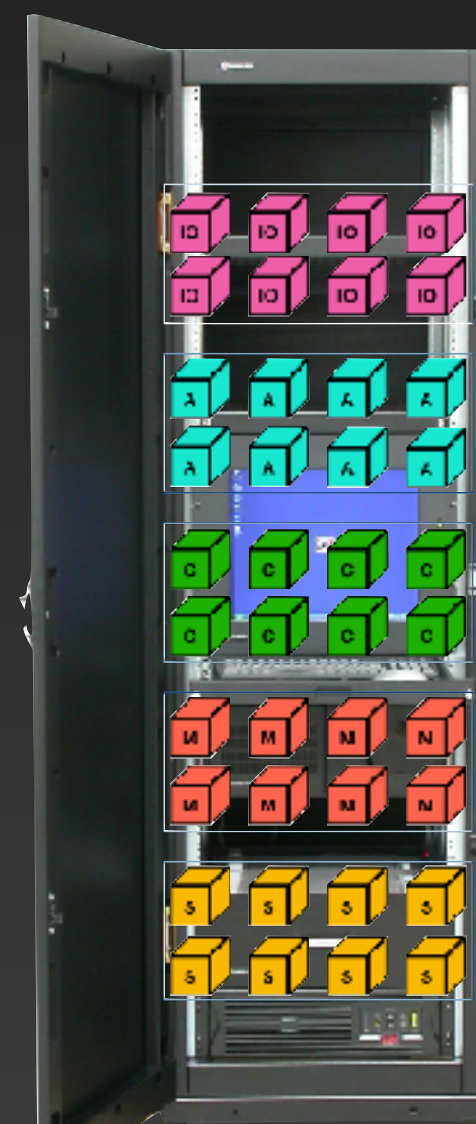
Power & Cost Efficient Domain Specific Architectures, DSA

Fixed Architecture

Hard Physical Composability

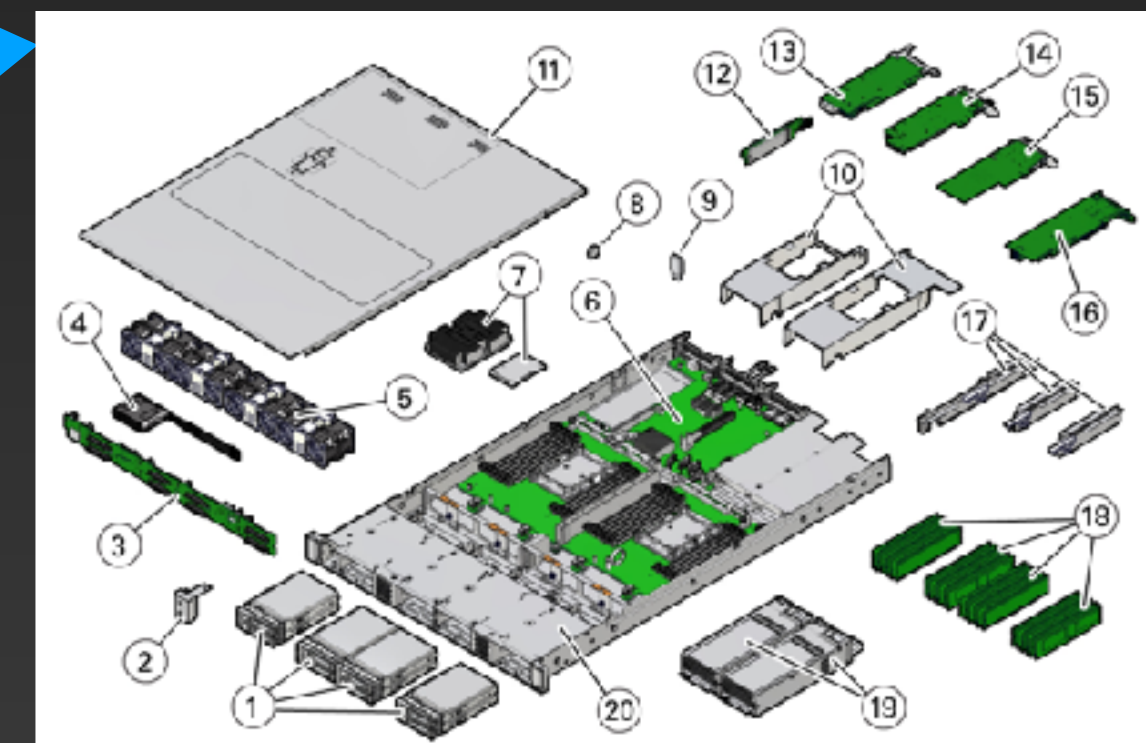


DSA Composability



Dynamic Software Composability

Pluggable Physical Composability



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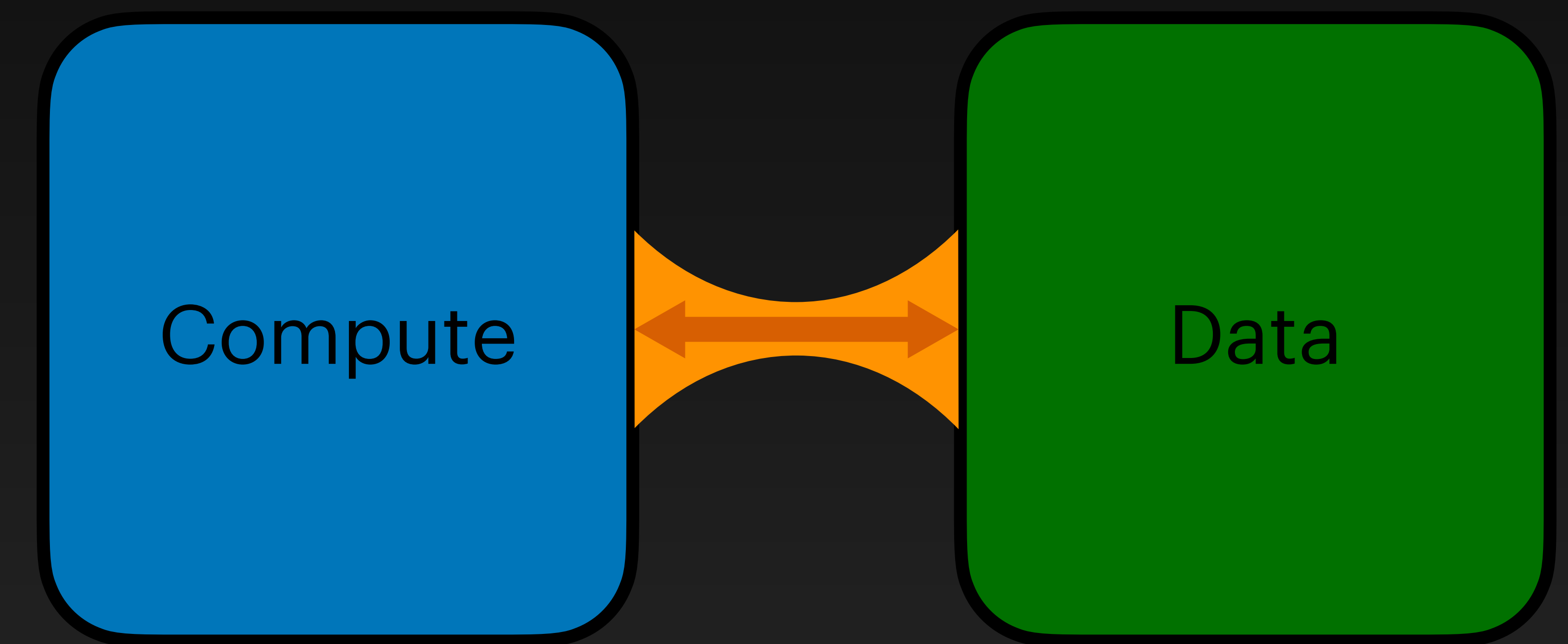
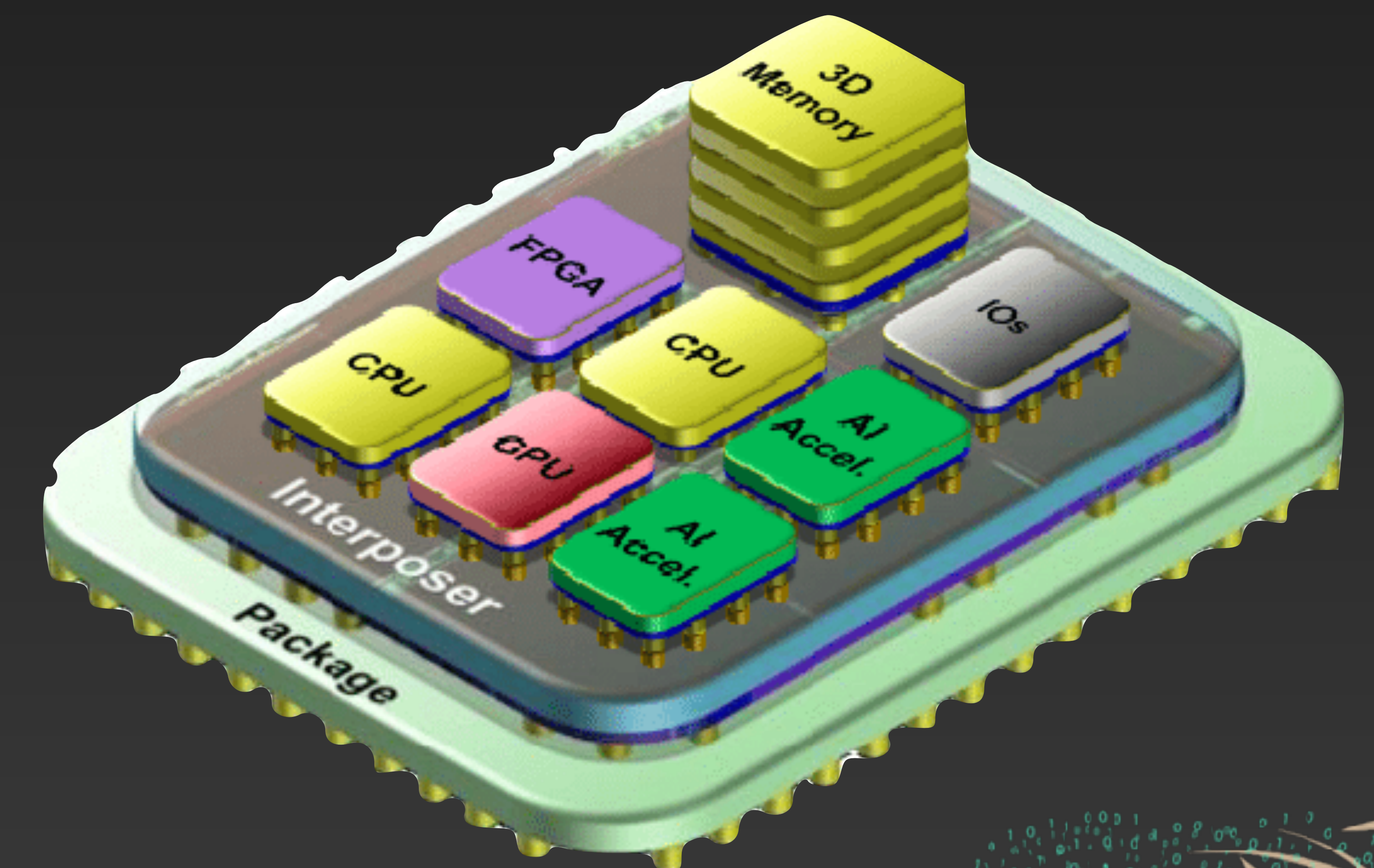
What is the Motivation for Chiplets?

Efficiently Combining Compute & Data in Pursuit of Performance

- Computer Architecture is JUST Compute & Data!
  - & Circumventing the Von-Neumann Bottleneck
- Improving Data to Compute Movement Efficiency
  - Moores Law.....shrinking everything
  - Bringing Memory on chip - Caching
  - Heterogeneous Processors
  - Moving everything closer together
    - Chiplets in a package.......2D, 2.5D & 3D





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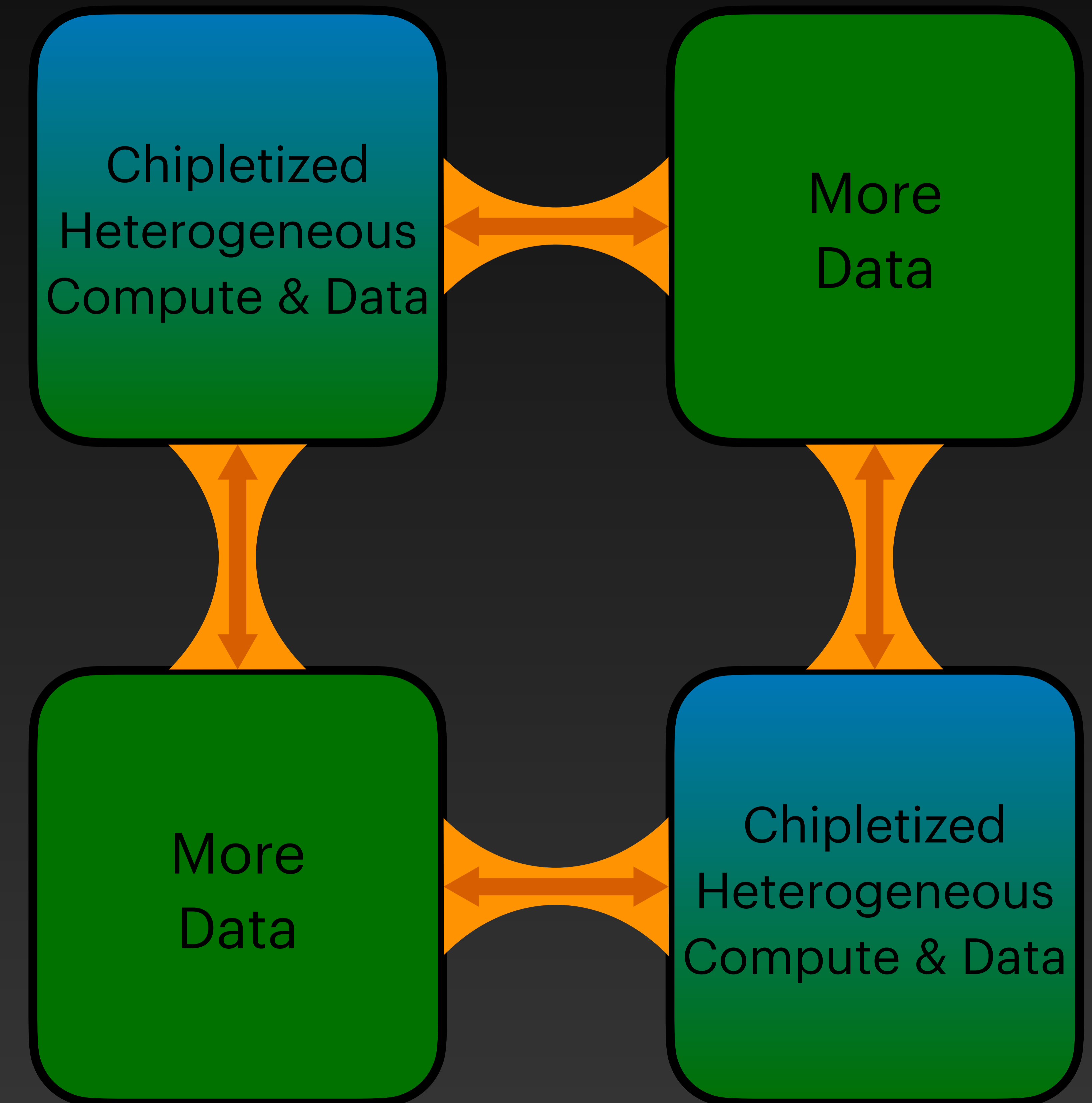
But what about Off Package IO?

System size rarely shrinks with higher density packaging!

- From ~0.5pJ/bit chiplet IO Energy
  - To ~10pJ/bit System IO Energy
    - A 20x off package increase!
- But there is the Promise of Co-Packaged Optics
- Ultimately we want Highest System Performance at the Lowest Energy & Cost
- Lets take a closer look at the data



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Popular PHY IO Standards

PHY Name	Substrate Type	Ch. Speed Gb/s	Tbits/s/mm Beachfront Tbits/s	Reach mm	Energy pJ/bit	Possible Chiplet IO	Possible Off Package IO
✤ **Traditional QSFPxx Optical IO**	Organic	112	Same as PHY	100,000's	15	✗	✓
* **PCIe-G5 Reference**	Organic	32	0.22	973	7	✗	✓
▲ **DDR Memory Ch. Reference**	Organic	6.4	0.06	300	5	✗	✓
Silicon Photonics	Any	Tb/s	Same as PHY	100,000's	1	✗	✓
* **OIF - VSR**	Organic	40	1.1	160	1.5	✓	✓
* **BoW Fast**	Organic	16	1.0	25	<0.5	✓	✗
† **UCIe - Standard**	Organic	32	1.8	<25	0.5	✓	✗
* **OpenHBI**	Silicon Interposer	8	3.4	8	0.5	✓	✗
† **UCIe - Advanced**	Silicon Interposer	32	10.5	<2	0.25	✓	✗

Potential Off Package Chiplet PHY

✤ Slide ▲ MCHPC'19 - Prospects for Memory - J. Thomas Pawlowski - Slide 29 * ODSA PHY Spreadsheet † UCIe Whitepaper

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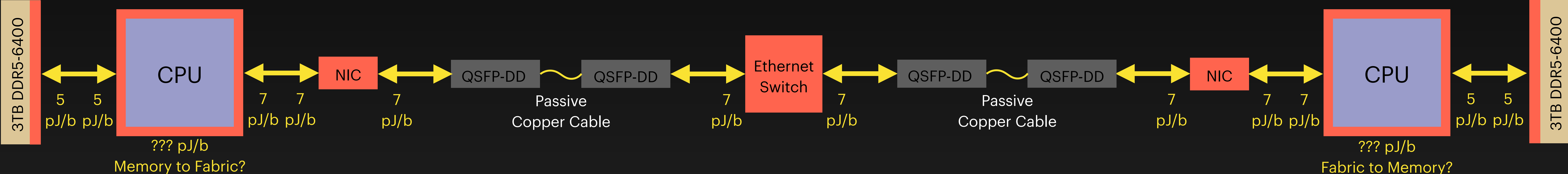
On and Off Package Memory Configurations

Traditional Local Memory + RDMA Example

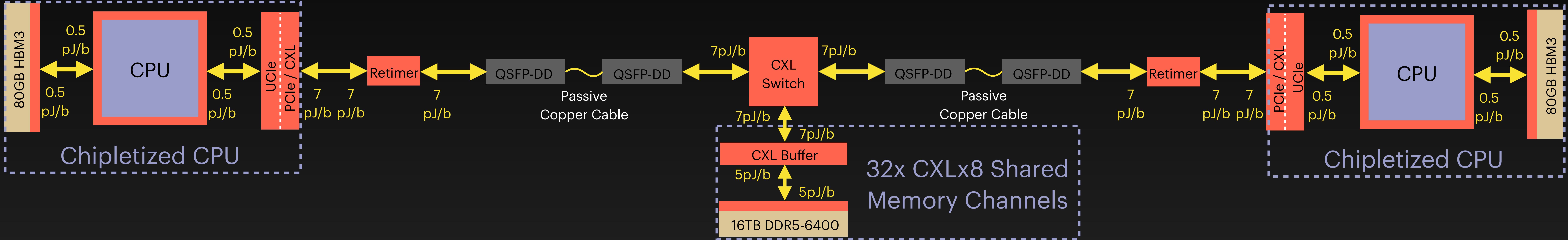


Example	80GB		3TB		8TB		16TB+	
	Bandwidth TBytes/s	Power Watts	Bandwidth TBytes/s	Power Watts	Bandwidth TBytes/s	Power Watts	Bandwidth TBytes/s	Power Watts
Traditional Local Memory + RDMA Example	0.6	49	0.6	49	0.6	373+	0.6	373+

Data Movement Energy shown in Red - Assume NIC & Ethernet Switch Power insignificant compared to their IO power

On and Off Package Memory Configurations

CXL Shared Memory Example



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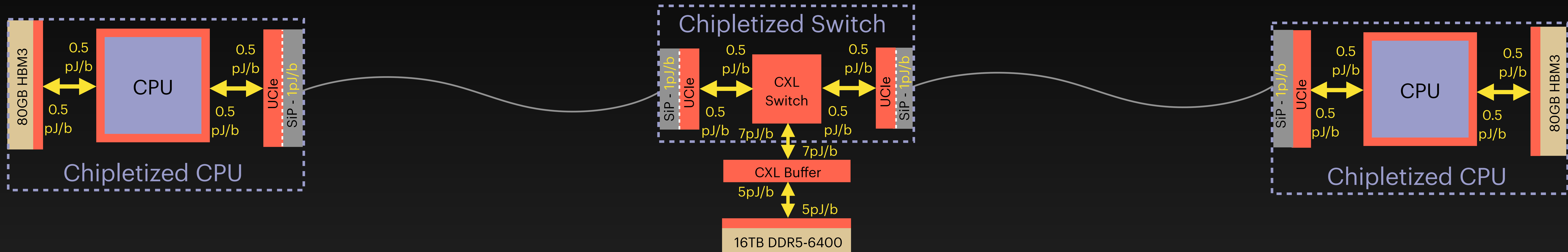
CXL Shared Memory Example	3	24	2	848	2	848	2	848

Data Movement Energy shown in Red - Assume Retimer & CXL Switch Power insignificant compared to their IO power

On and Off Package Memory Configurations

CXL Shared Memory Example with Co-Packaged Optics



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CXL Shared Memory Example	3	24	2	848	2	848	2	848
SiP CXL Shared Memory Example	3	24	2	448	2	448	2	448

Data Movement Energy shown in Red - Assume CXL Switch Power insignificant compared to its IO power

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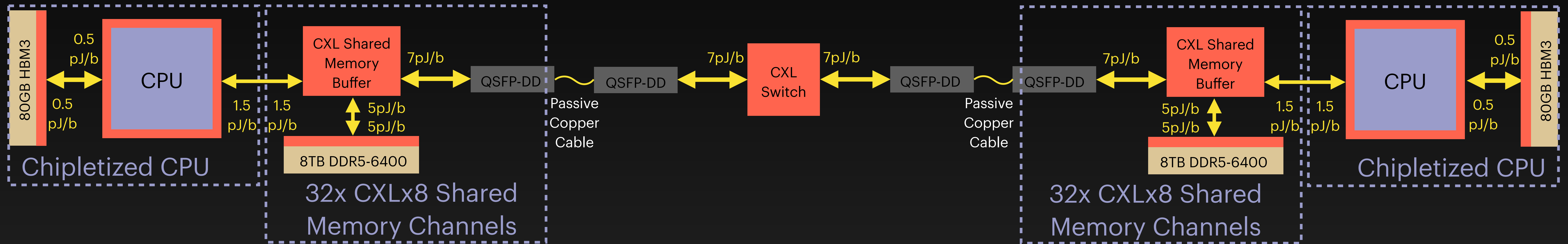
On and Off Package Memory Configurations

CXL Shareable, Local Memory using OIF-VSR Example



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SiP CXL Shared Memory Example	3	24	2	448	2	448	2	448
CXL Shareable, Local Memory Example	3	24	2	208	2	208	2	656

Data Movement Energy shown in Red - Assume CXL Shared Memory Buffer & CXL Switch Power insignificant compared to their IO power

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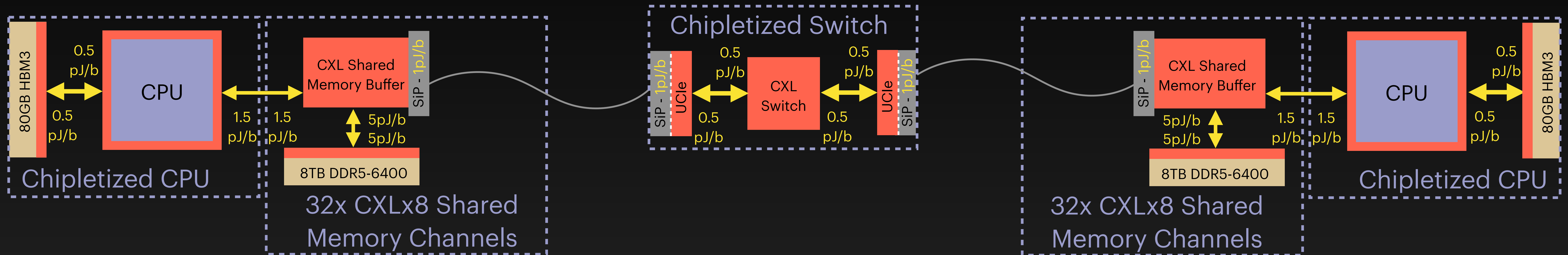
On and Off Package Memory Configurations

Optical, CXL Shareable, Local Memory using OIF-VSR Example



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CXL Shareable, Local Memory Example	3	24	2	208	2	208	2	656
SiP CXL Shareable, Local Memory Example	3	24	2	208	2	208	2	304

Data Movement Energy shown in Red - Assume CXL Shared Memory Buffer & CXL Switch Power insignificant compared to their IO power

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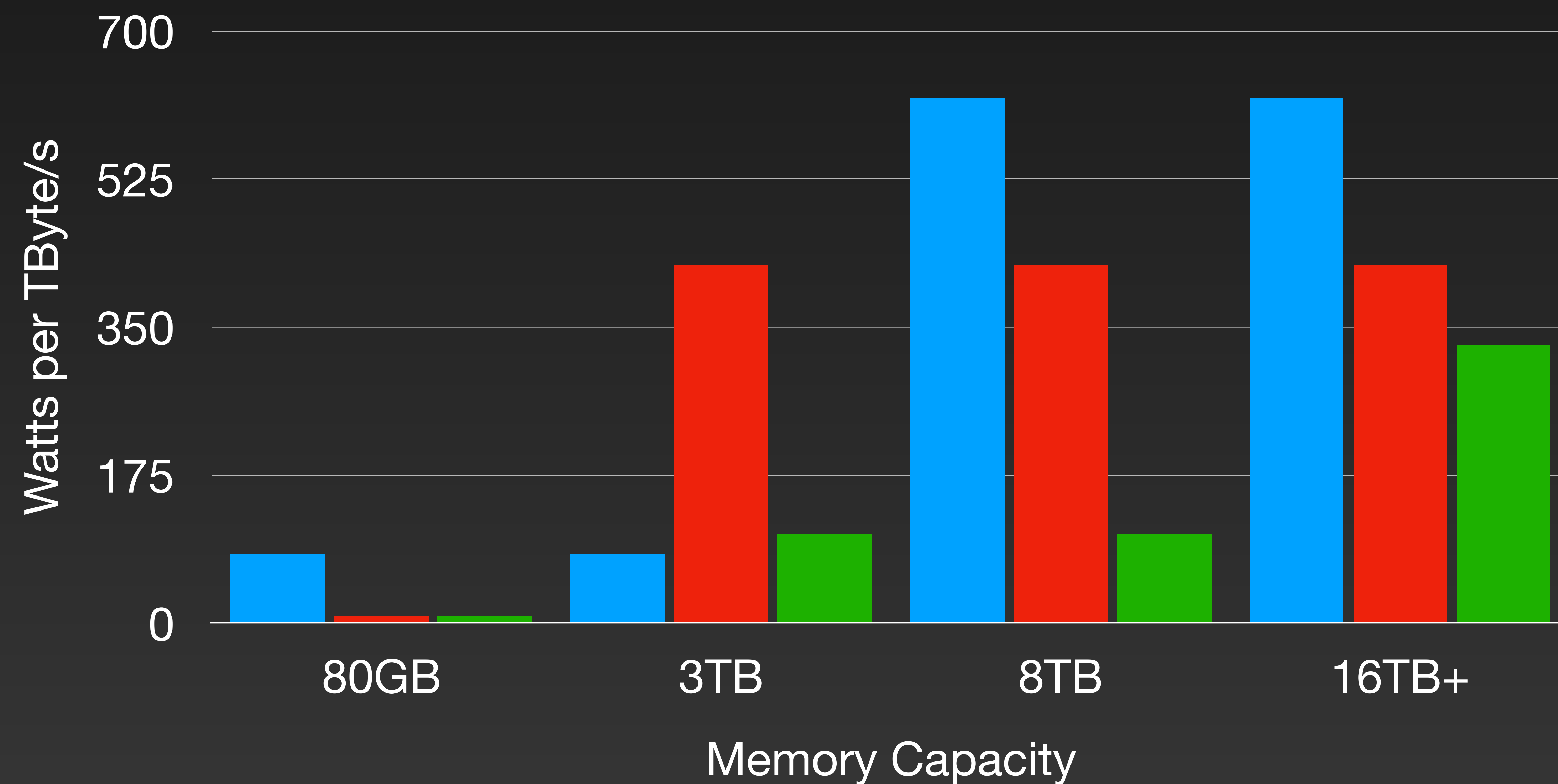
Watts/TByte/s Memory Sharing Comparison

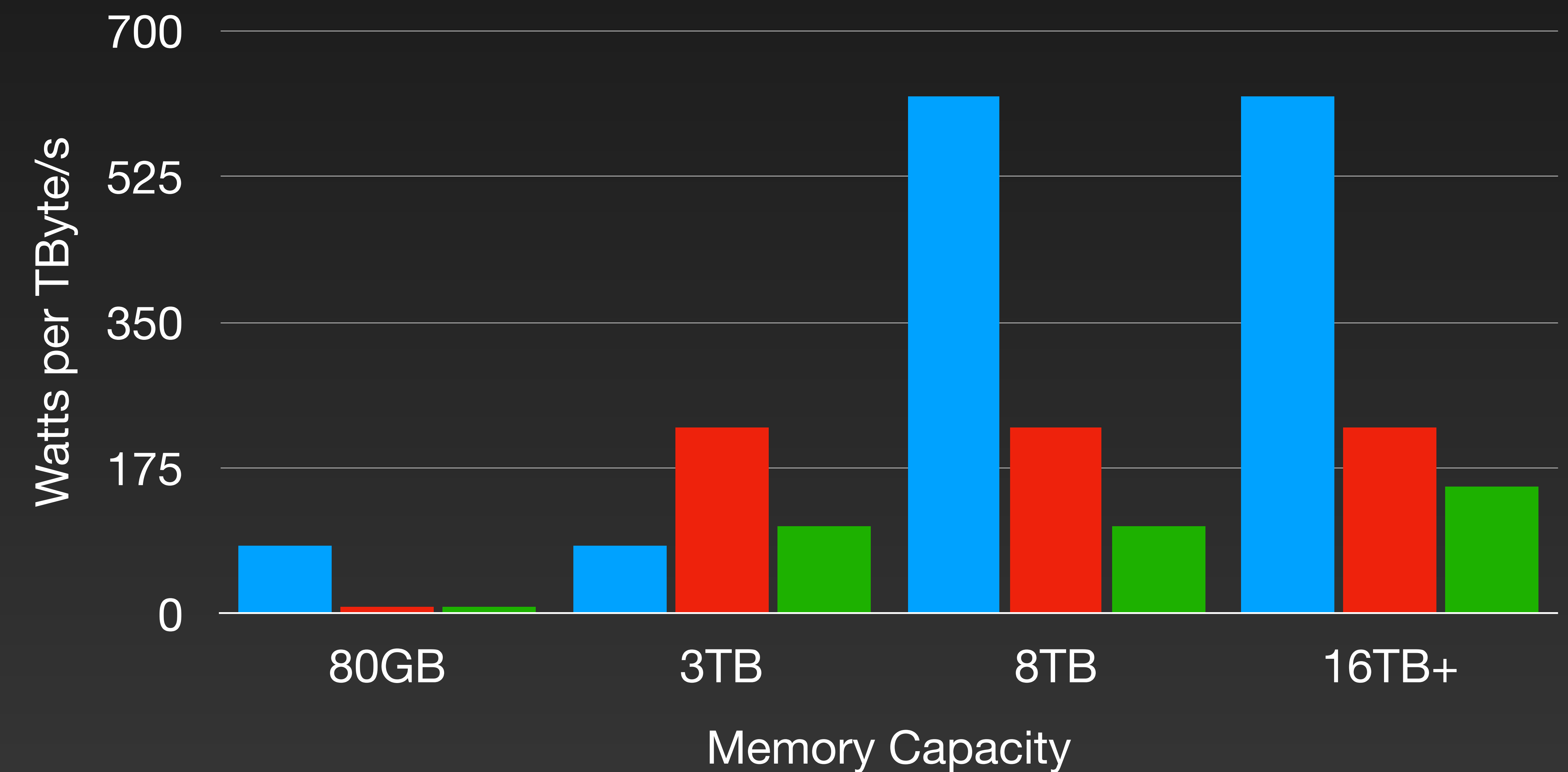
Energy Advantage of Off-Package Chiplet Shared Memory Buffers

Passive Copper Interconnect

Lower is Better



Silicon Photonic Interconnect



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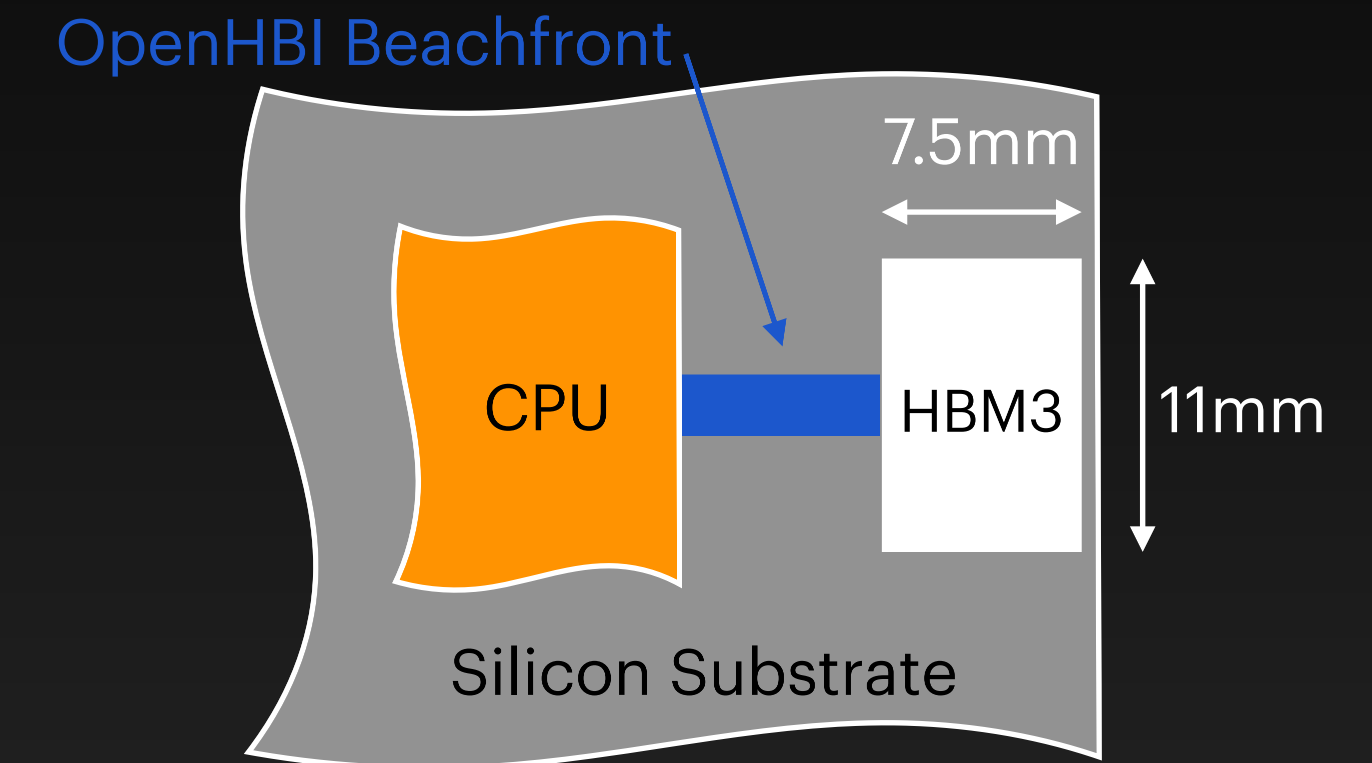
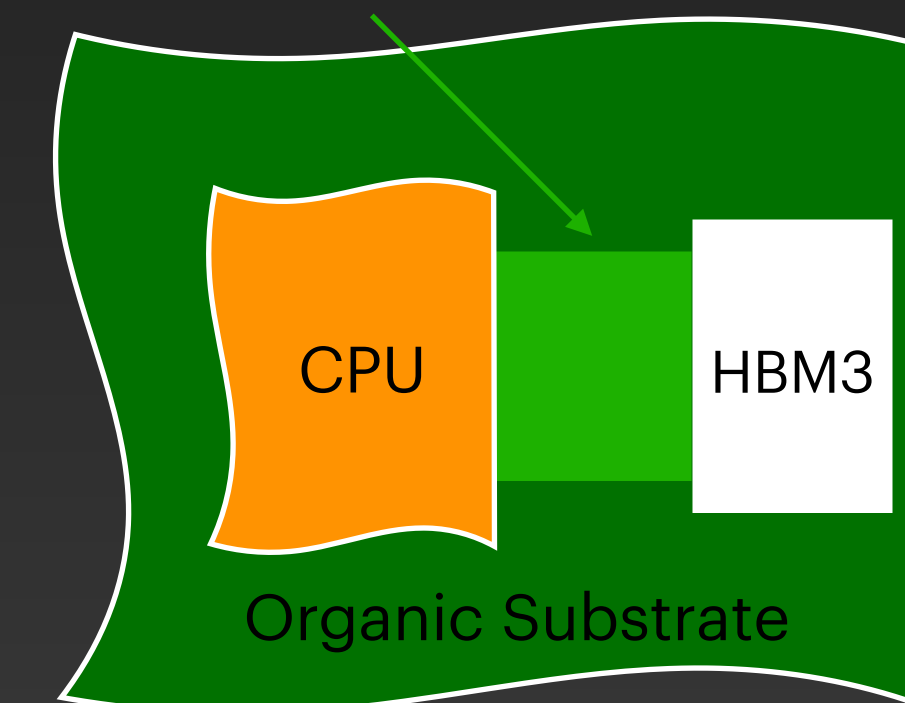
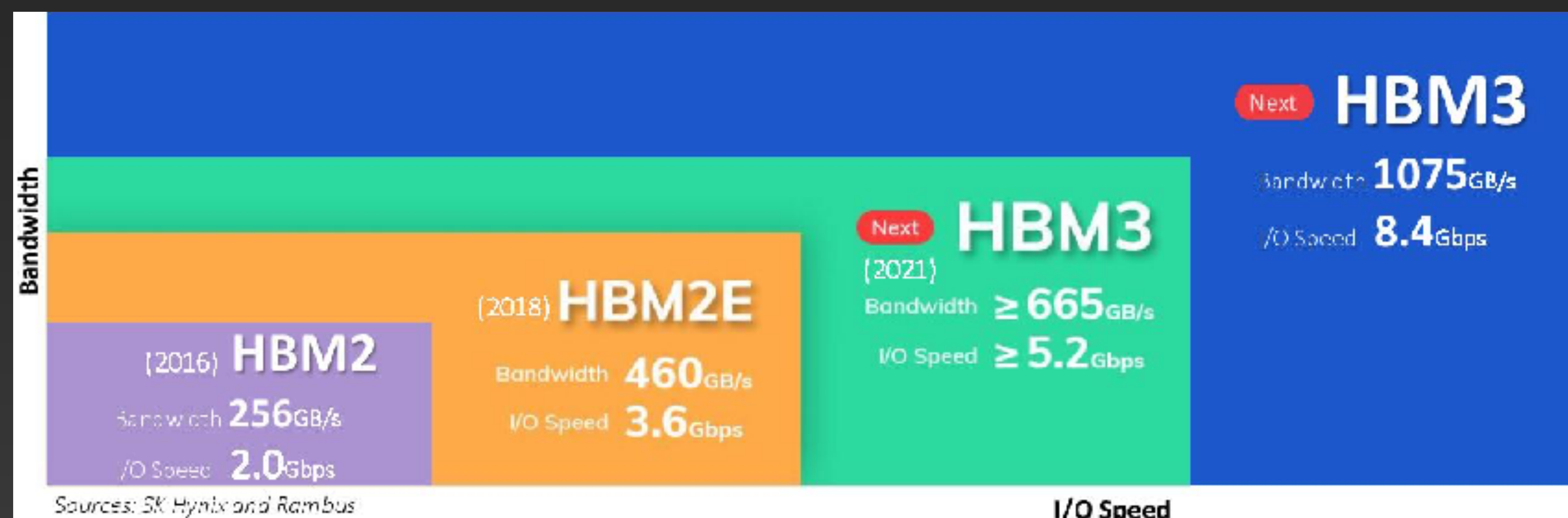
Can UCIe Standard or BoW support HBM?

BoW & UCIe-Standard for HBM with Organic packages

- HBM = 11mm beachfront + roadmap to 1.1TB/s
  - Requires 1.1TB/s * 8 / 11mm = 0.8Tb/s/mm
    - UCIe-Standard & BoW can support HBM using organic substrates







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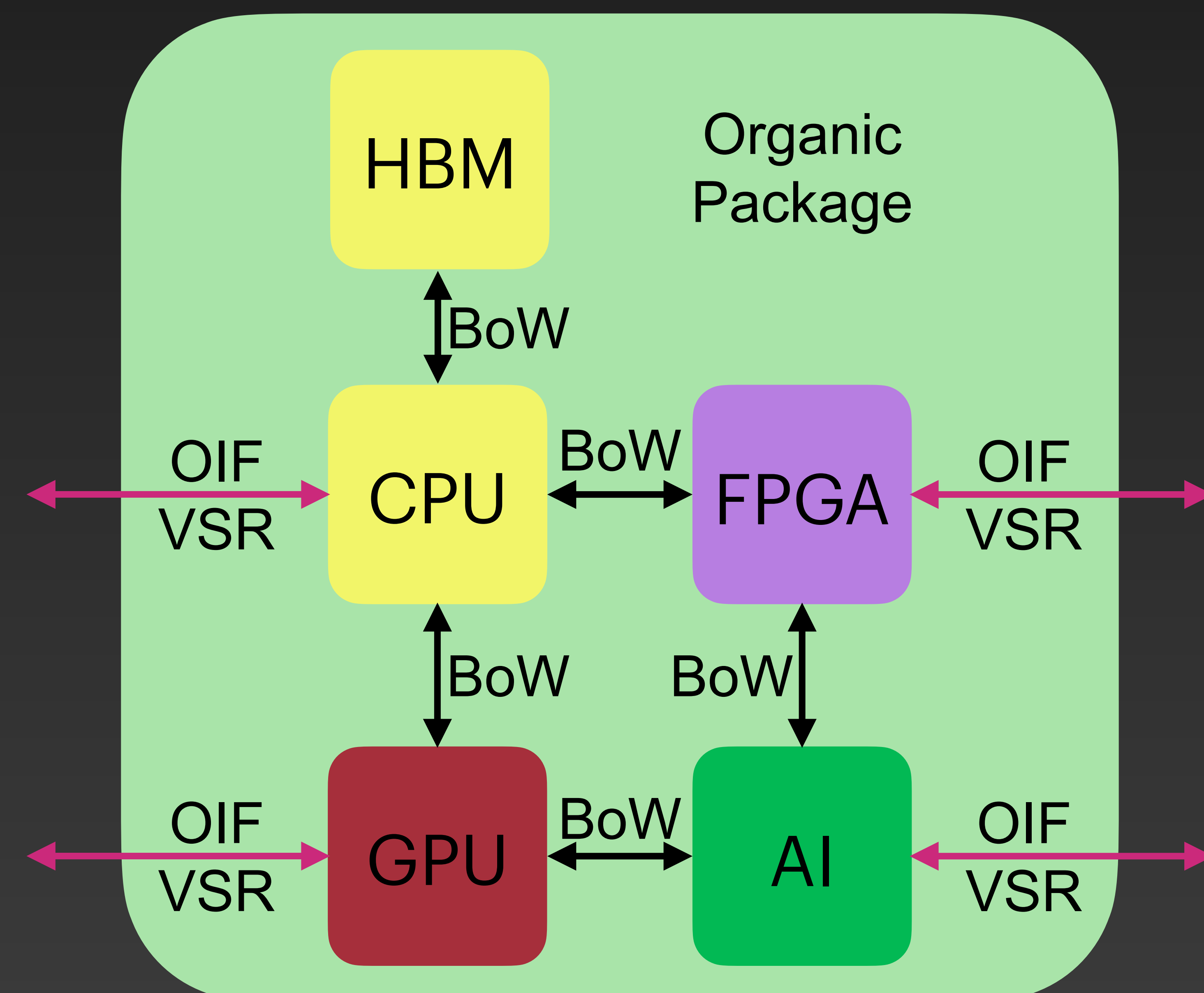
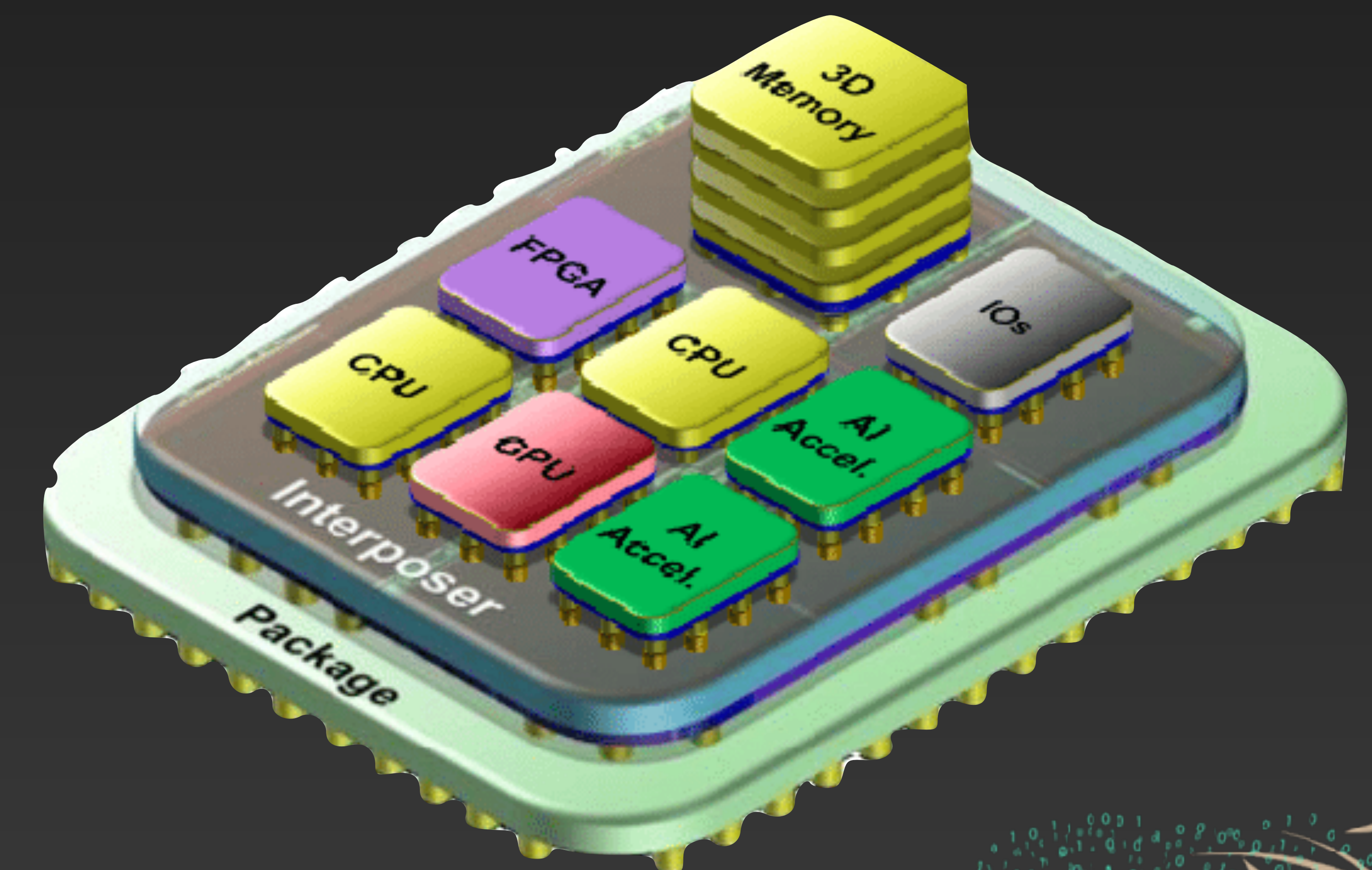
Proposed Chiplet Industry Standardization

Accessible to Tier 2 and 3 Industry Players

- Utilize BoW & OIF-VSR PHYs for On & Off Package Chiplet IO's respectively
- Leverage Cost effective Organic Packaging
- Unifying Off Package IO for ALL Processors WILL Democratize Compute





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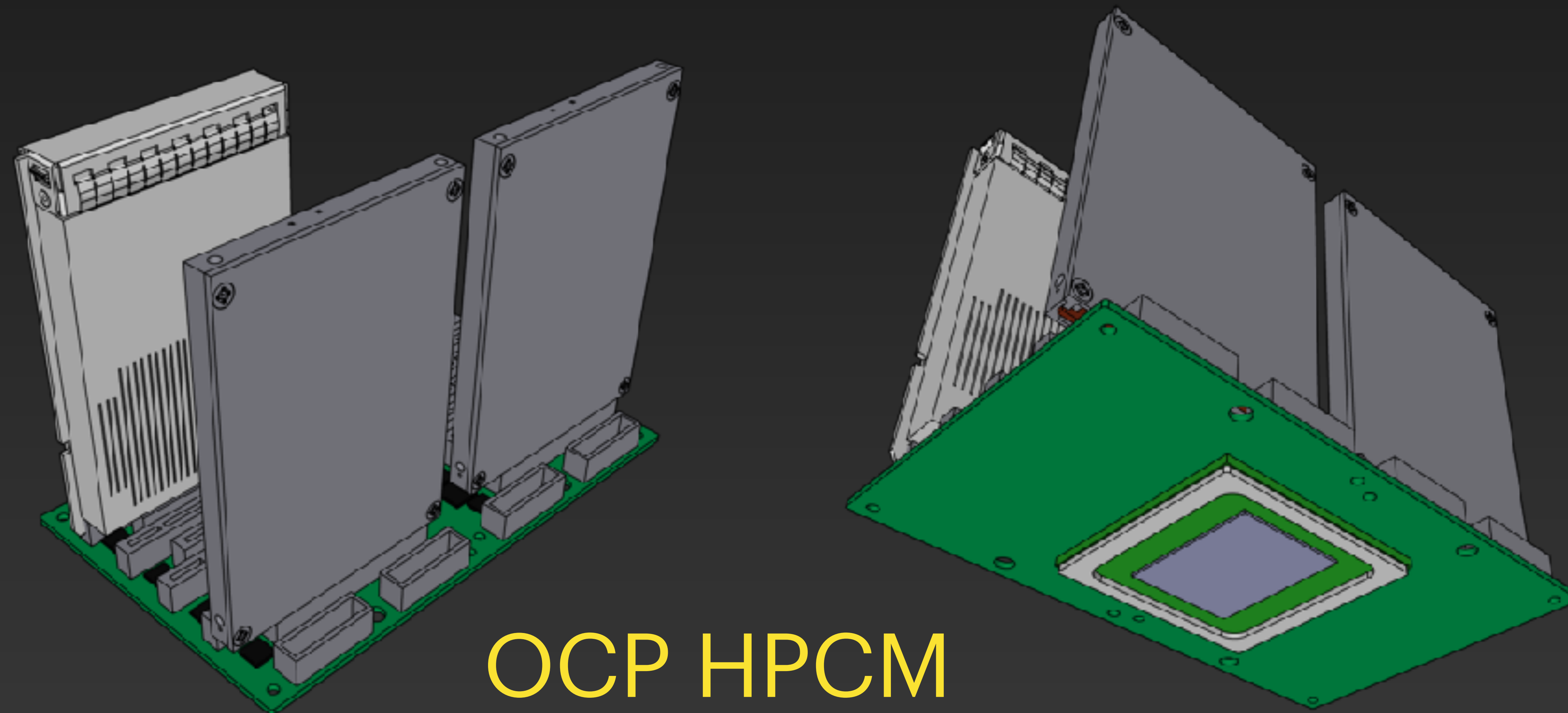
Proposed Chiplet Industry Standardization

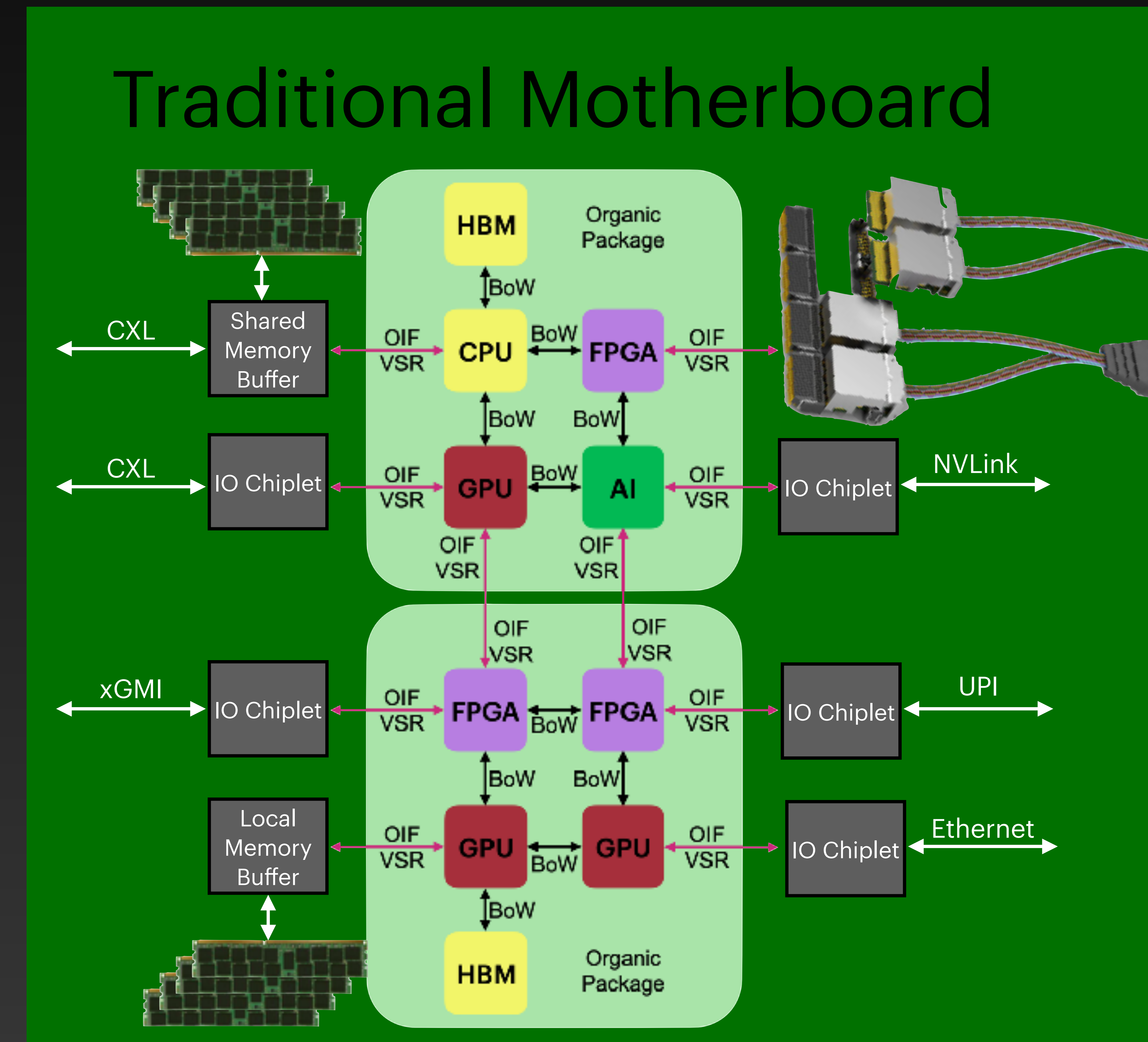
Accessible to Tier 2 and 3 Industry Players

- Off-Package Chiplets are simply IO Translators!
  - For differing IO Use Cases
- OCP HPCM - 3D System Level Packaging



OCP HPCM

Novel Pluggable Chiplet 3D System Level Packaging



Near Package Optical IO

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Summary

- Today's Disaggregation Models are taking Energy Efficiency in the wrong direction
  - Insight through Energy Centric Compute Analysis
- Support of an off-package Chiplet IO Standard will allow :-
  - Graceful Power and latency increase
- This Presentation ONLY assessed Off-Package Chiplets from an Energy Saving Perspective. Several other significant benefits accrue :-
  - Low Latency to Large Capacities at High Bandwidths
  - Flexible, Modular and Composable
  - Lower cost and improved manufacturability
  - Simpler, Sustainable and Competitive Ecosystem Business Model