

# OPEN POSSIBILITIES.

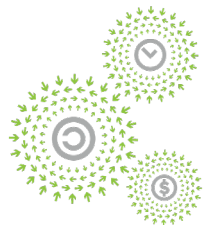
## Reimagining Memory Expansion for Single Socket Servers with CXL



NOVEMBER 9-10, 2021

# Reimagining Memory Expansion for Single Socket Servers with CXL

Chris Petersen, HW System Technologist, Meta  
Bharath Muthiah, Technical Sourcing Manager, Meta



**OPEN**  
PLATINUM™

OPEN POSSIBILITIES.

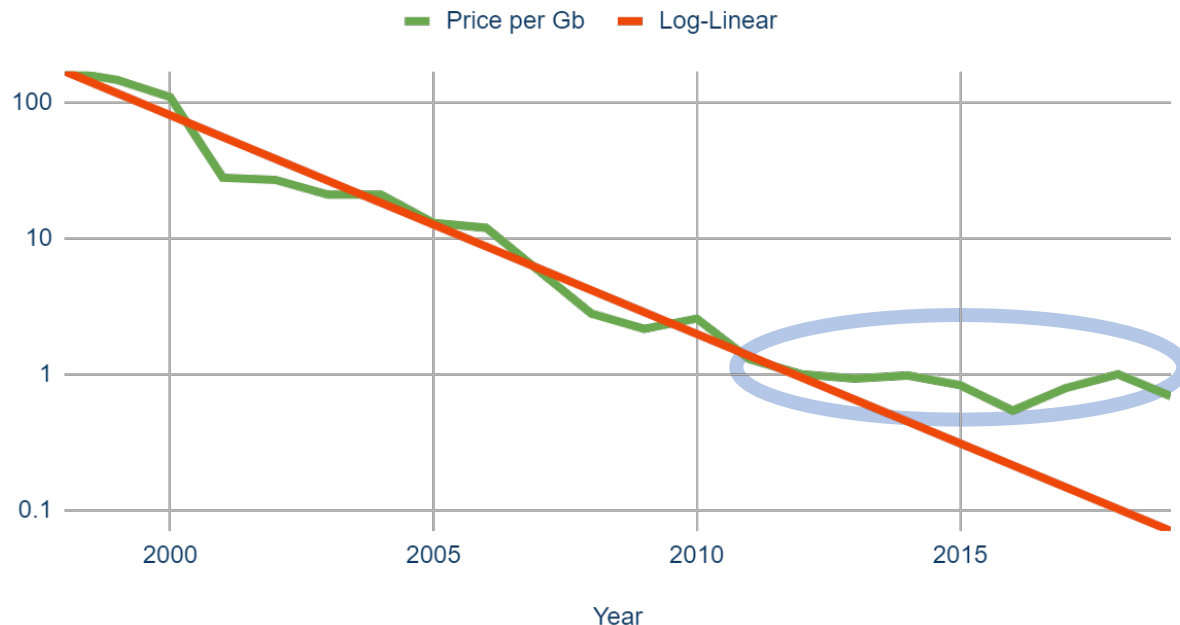


# Increasing Memory Cost and Power



SERVER

Price per Gb (Log Scale)



**Memory an increasing % of system power and cost**

- Memory price (cost/bit) flat due to scaling challenges

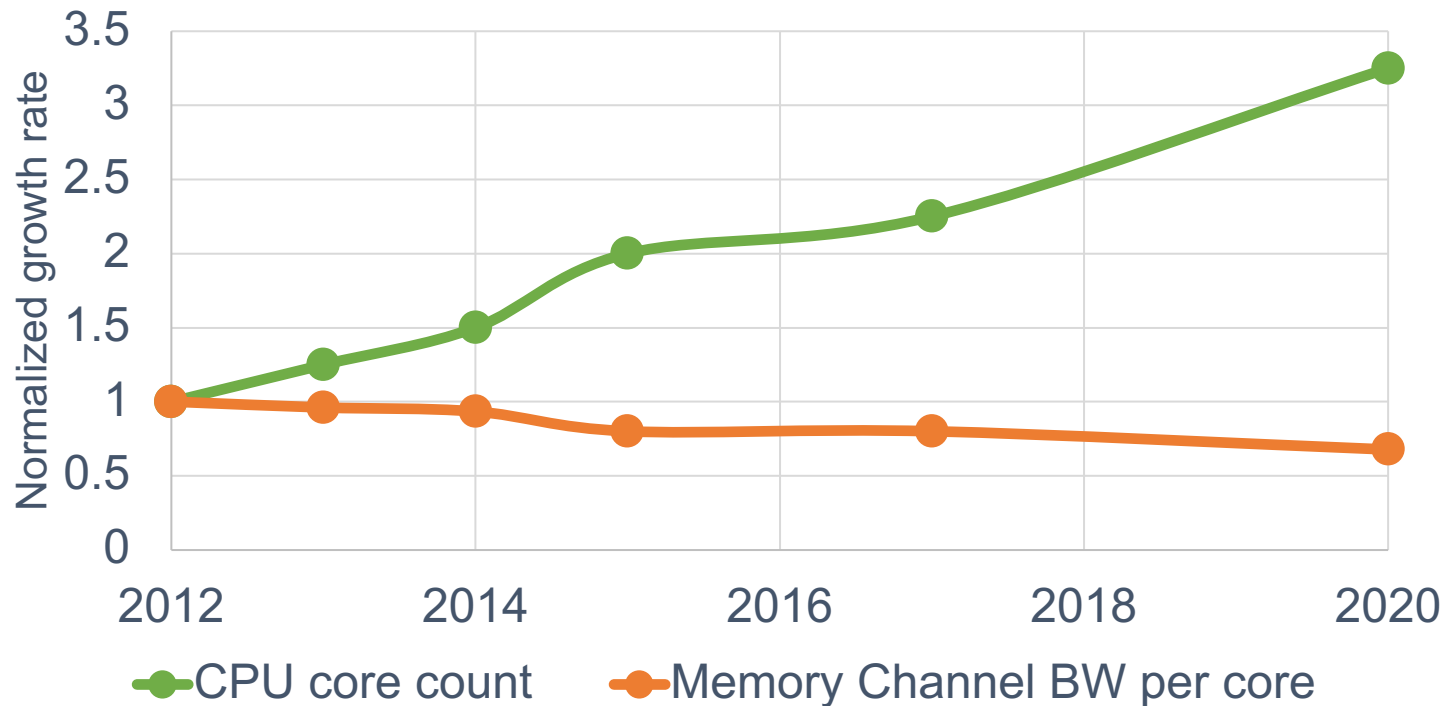
OPEN POSSIBILITIES.



# Increasing Core Counts Drives Growth



SERVER



**Increasing core counts driving memory demand**

- Increased Bandwidth
- Increased Capacity

OPEN POSSIBILITIES.





# Server Design Implications



SERVER

- Adding CPU-attached memory channels is expensive
- Increasing DDR\* speed is challenging
- Emerging memory needs a better method of attachment
- Memory configurations today are homogeneous, but more flexibility is needed

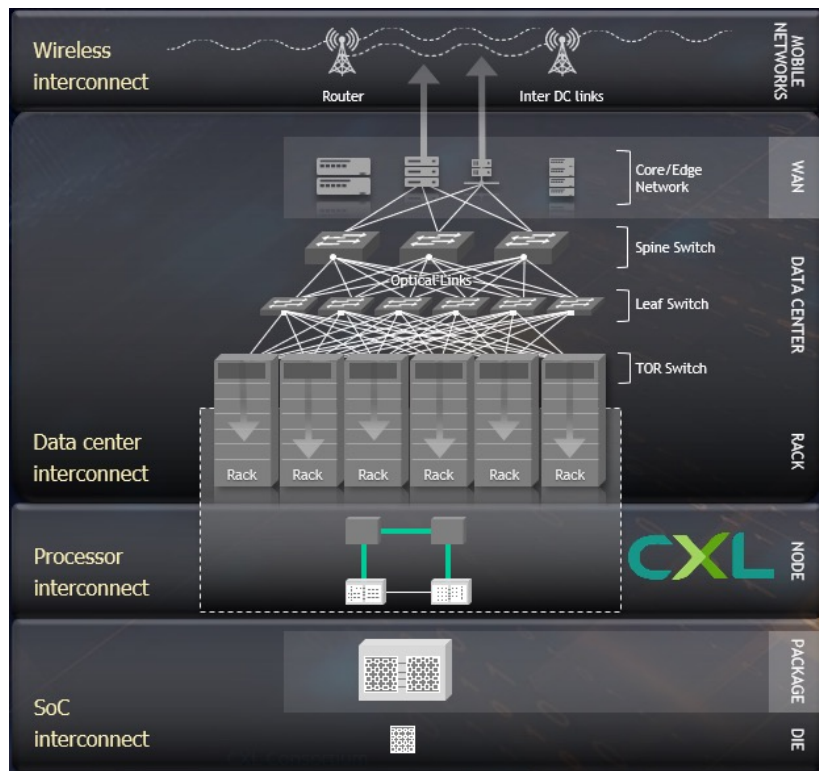
OPEN POSSIBILITIES.



# Introducing CXL

## Processor Interconnect:

- Open industry standard
- High-bandwidth, low-latency
- Coherent interface
- Leverages PCI Express®
- Targets high-performance computational workloads

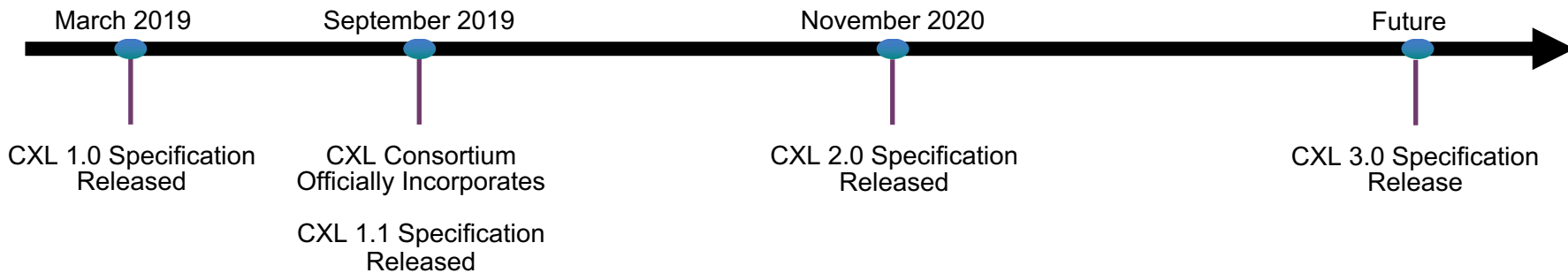


SERVER

A new class of interconnect for device connectivity

OPEN POSSIBILITIES.

# CXL - Looking Ahead



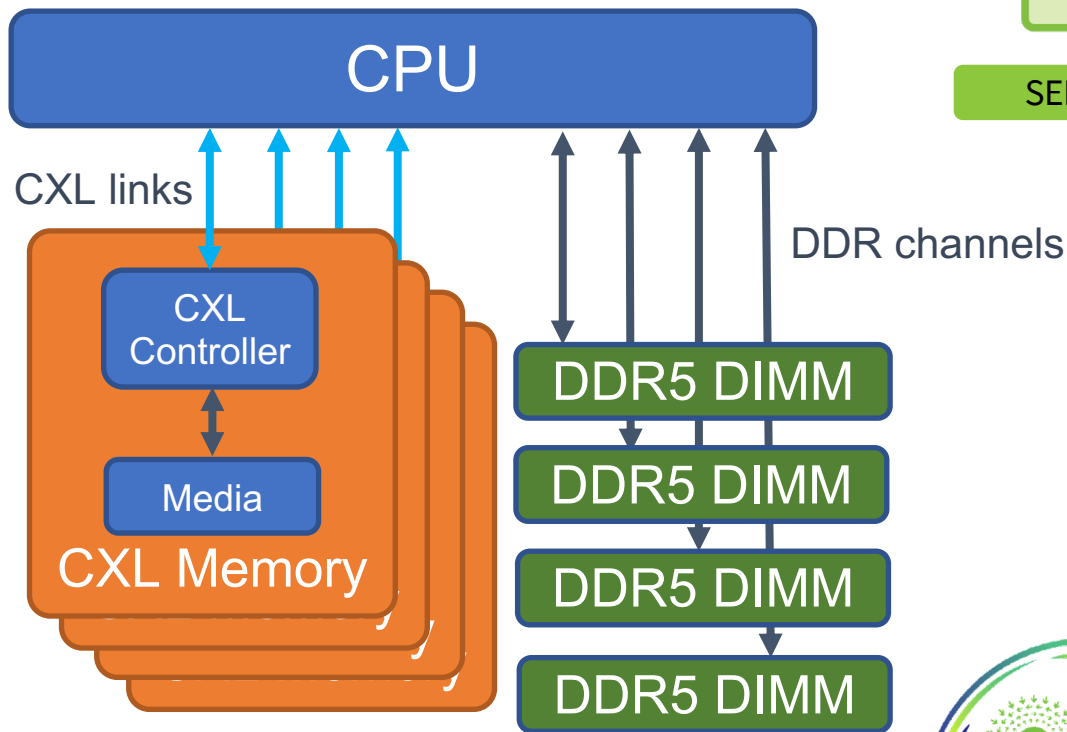
- CXL Specification development progressing at predictable cadence
- CXL 2.0 introduces new features & usage models including switching, pooling, persistent memory support, and security
- CXL 3.0 in development

OPEN POSSIBILITIES.



# CXL Memory Expansion

- Scale BW
- Scale Capacity
- Enable heterogeneity



OPEN POSSIBILITIES.

# CXL Memory Expansion POC



SERVER

- Intel Sapphire Rapids CPU (pre-prod)
- Intel CXL FPGA card w/  
2x DDR4 DIMMs

Packet 95	Rx	x16	Mem	M2S Request	MemOpcode	SnpType	Tag	Address	TC	Time Delta	Time Stamp
					MemRdData	SnpData	34014	0x000115EE60000	0	41 500 ns	0000 501 603 112 810 s
Packet 140	Rx	x16	Protocol ID	Data	Time Delta	Time Stamp					
			0x5555	66 bytes	40 250 ns	0000 501 603 154 310 s					
Packet 165	Rx	x16	LLCTRL	Type	SubType	Full_Ack	Time Delta	Time Stamp			
				LLCRD	Ack	0x01	120 000 ns	0000 501 603 194 560 s			
Packet 166	Rx	x16	Mem	S2M No Data Response	MemOpcode	MetaField	MetaValue	Tag	Time Delta	Time Stamp	
					CompE	MetaState	Invalid	34014	39 250 ns	0000 501 603 314 560 s	
Packet 167	Rx	x16	LLCTRL	Type	SubType	Full_Ack	Time Delta	Time Stamp			
				LLCRD	Ack	0x01	42 250 ns	0000 501 603 353 810 s			
Packet 168	Rx	x16	LLCTRL	Type	SubType	Full_Ack	Time Delta	Time Stamp			
				LLCRD	Ack	0x02	38 500 ns	0000 501 603 396 060 s			
Packet 169	Rx	x16	LLCTRL	Type	SubType	Full_Ack	Time Delta	Time Stamp			
				LLCRD	Ack	0x01	39 250 ns	0000 501 603 434 560 s			
Packet 170	Rx	x16	Mem	S2M Data Response Header	MemOpcode	MetaField	MetaValue	Tag	Poison	Idle	Time Stamp
					MemData	MetaState	Invalid	34014	0	0 000 ns	0000 501 603 473 810 s
Packet 171	Rx	x16	Cache/Mem	Data Chunk	Data	Idle	Time Stamp				
					4 dwords	0 000 ns	0000 501 603 473 810 s				
Packet 172	Rx	x16	Cache/Mem	Data Chunk	Data	Idle	Time Stamp				
					4 dwords	3 680 ns	0000 501 603 473 810 s				
Packet 173	Rx	x16	Mem	S2M Data Response Header	MemOpcode	MetaField	MetaValue	Tag	Poison	Idle	Time Stamp
					MemData	MetaState	Invalid	34014	0	0 000 ns	0000 501 603 477 810 s
Packet 174	Rx	x16	Cache/Mem	Data Chunk	Data	Idle	Time Stamp				
					4 dwords	0 000 ns	0000 501 603 477 810 s				
Packet 175	Rx	x16	Cache/Mem	Data Chunk	Data	Time Delta	Time Stamp				
					4 dwords	35 250 ns	0000 501 603 477 810 s				

Please visit the Meta booth for a demo video!

OPEN POSSIBILITIES.



# Server Design Concept w/ CXL Memory



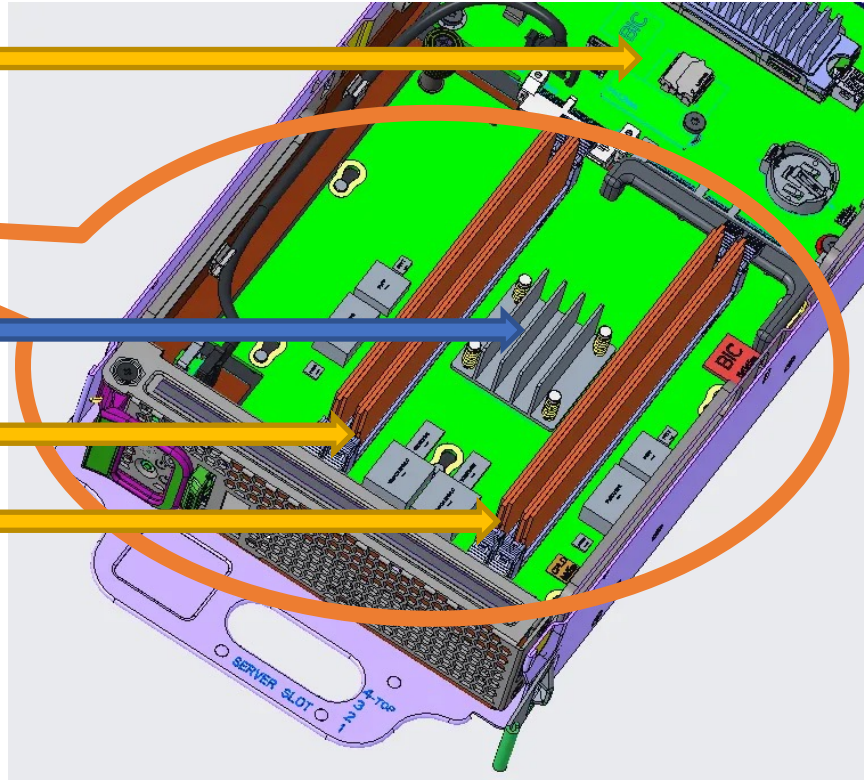
SERVER

Motherboard

Expansion board

CXL Controller

DDR4/DDR5  
DIMM Slots



OPEN POSSIBILITIES.

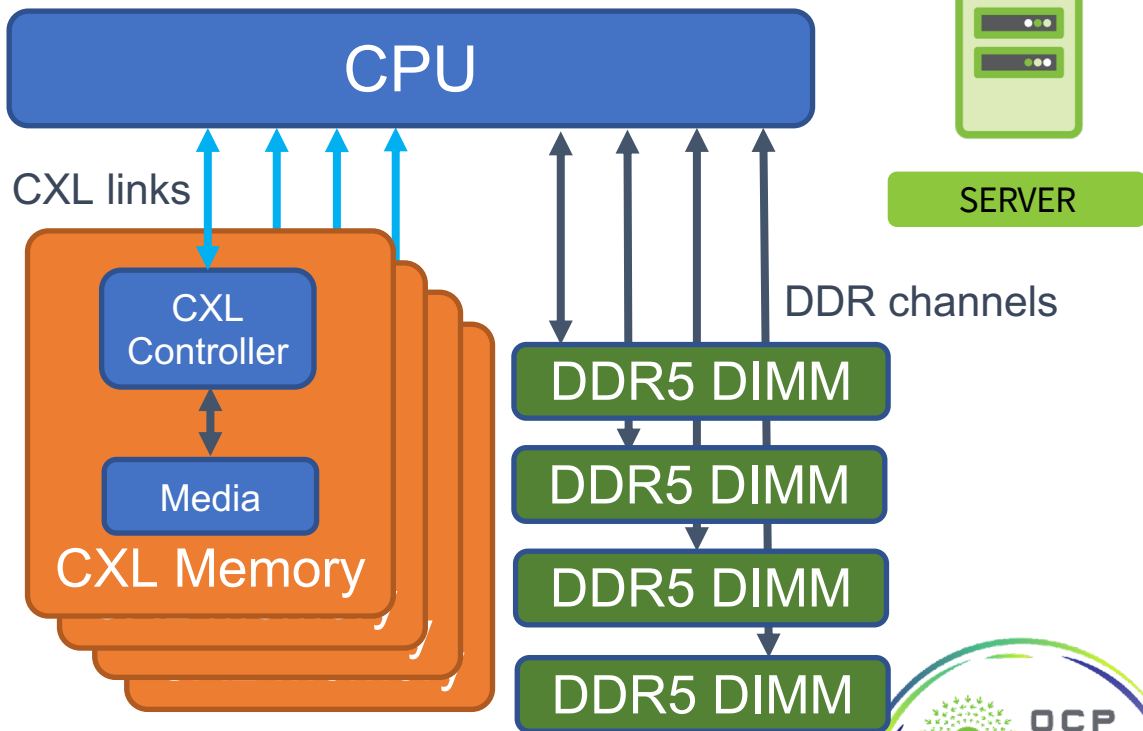
# Building Open & Interoperable Ecosystem

Building an Open and Interoperable Ecosystem across Technology and System Providers is key to successful adoption!

Technology Providers

- CPU
- CXL Controller ASIC
- Memory

System Providers



OPEN POSSIBILITIES.



# Building Open & Interoperable Ecosystem

“CXL is a game-changer in the compute landscape. Intel was a key author of the specification and like so many previous successful standards, drove to make it an industry-owned technology. Our Next Gen Intel Xeon Scalable processor (codenamed Sapphire Rapids) will be Intel’s first data center processor with CXL, and here at OCP you can see the first customer implementations built on Next Gen Intel Xeon processors and Intel FPGA technology. ” **Dr Debendra Das Sharma, Intel Fellow, Director Intel IO Technology & Standards, Co-chair CXL Consortium Technical Task Force, and PCI-SIG Board Member.**



SERVER

CPU

“We are excited about the data center innovation that CXL can enable. AMD is committed to delivering breakthrough memory expansion with CXL in our next generation server processors. We are actively working with CXL consortium members and partners such as Meta to bring these capabilities to market. ” **Jay Kirkland, CVP, Server Platform Solutions Eng, AMD**

OPEN POSSIBILITIES.





# Building Open & Interoperable Ecosystem

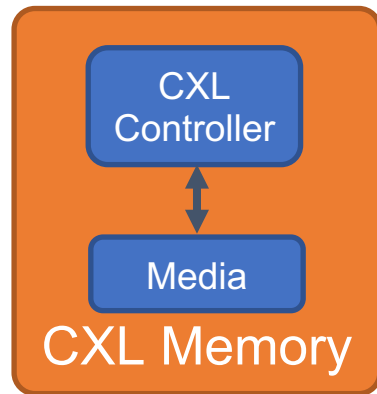
“Improving memory utilization and reducing total cost of ownership continue to be a key focus for the industry and CXL is an important innovation vector to address these challenges. Microchip has contributed significantly to the CXL specification and we are excited to work with Meta to deliver solutions and contribute our joint efforts to OCP in the future.” **Andrew Dieckmann, VP Marketing, Microchip Technology**

More technology providers and startups innovating in this space! Support from all major memory partners!

OPEN POSSIBILITIES.



SERVER



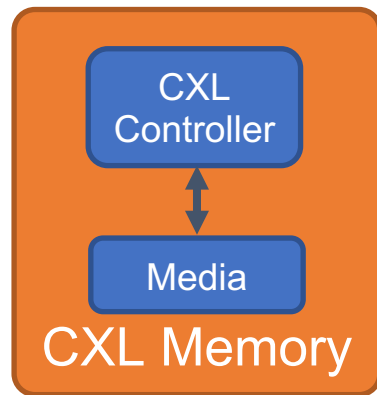
# Building Open & Interoperable Ecosystem

“We are excited to be partnering and innovating with Meta on the 1st generation CXL Memory modules! We look forward and are committed to enabling this transformative technology on Meta’s next generation perf/w optimized Yosemite Servers.” **Mike Yang, SVP of Quanta Computer and President of QCT**

“We are thrilled to see CXL progress from technology specifications into 1st generation products. Wiwynn is excited to partner with Meta to enable CXL Memory Modules for Meta’s perf/w optimized Yosemite 1S Servers,” **Steven Lu, Senior Vice President of Product Development, Wiwynn**



SERVER



OPEN POSSIBILITIES.



# Call to Action

- Join us in developing CXL Memory solutions!
- We expect to provide a server design contribution in 2022.
- Where to find additional information:

Mailing list: <http://lists.opencompute.org/mailman/listinfo/opencompute-server>

CXL: <https://www.computeexpresslink.org/>

OPEN POSSIBILITIES.



Thank you!



NOVEMBER 9-10, 2021