

Advanced Packaging Enabling the Post Moore Era

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ASE at a Glance

Established 1984, production commenced at flagship factory in Kaohsiung, Taiwan

Achieved global leadership in IC Assembly, Test & Materials (ATM) in 2003 & maintained #1 OSAT position since

Completed acquisition of Universal Scientific Industrial Co. (USI) to expand DMS/EMS/ODM module & system manufacturing capability

Completed acquisition of SPIL, Ltd. to expand IC assembly & test manufacturing capability

Operating at 19 facilities worldwide, serving multiple markets, applications & geographies

> 90K employees: Global team comprises operations, engineering, R&D, sales & marketing

ASE Technology Holding overall revenue (pro forma) of \$13.2B in 2018



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ASE Organization



ASE in the Electronics Value Chain

Bridging OSAT and EMS





Semiconductor Revenue vs. Process Generation





Chip & System Integration





Role and Value of Semiconductor Packaging Increasing





Drivers for Heterogeneous Integration

- Moore's law slowing
- Exponential rise in chip development costs
- Decreasing number of leading edge fabs
- SoC scaling cost barriers
 - Increasing cost per transistor on advanced node
 - Increasing SoC die size wafer yield/die cost impact
- SoC scaling technology barriers
 - Integration challenges for logic, analog and memory
 - Reduced availability of IP for advanced nodes
- Opportunity to leverage mature process nodes for analog and other IP blocks
 - Performance and cost optimized
 - Design re-use / increased flexibility
 - Faster time to market
- Virtual SoC





Source: Intel



Advanced Integration Solutions - Foundry



- WLSI Wafer Level System Integration
 - InFO (Integrated FanOut)
 - InFO_PoP (FO Pkg on Pkg)
 - InFO_AiP (FO with Antenna in Pkg)
 - MUST (Multi-Stack)
 - InFo_oS (FO on Substrate)
 - InFO_MS (FO with Memory on Substrate)
 - InFO_UHD (FO Ultra High Density)
 - CoWoS (Chip on Wafer on Substrate- 2.5D)

Applications

Mobile AP, RF FEM, Baseband, etc.



High Performance Mobile, Network, AI/HPC, etc.

Source: WikiChip (Semicon, July 2019)



Advanced Integration Solutions - IDM

HPC Packaging Toolbox

- EMIB: Embedded interconnect bridge in organic substrate
- Foveros: Integration on TSV interposer
- Co-EMIB: Integration of multiple Foveros structures and memory/IP chiplets using EMIB
- ODI (Omni Directional Interconnect): Integration on reduced size interposer enabling direct vertical interconnect to top die for power delivery



Source: Intel/EE Times (07.09.19)



Advanced Integration Solutions - OSAT



MCM

- Die partition or multi device integration on organic substrate
- High performance SoC and IP die (i.e. SERDES) integration
- Multi fab/process node device combinations
- Low to medium interconnect density: 100's-1000's
- Separation of digital/analog blocks
- Benefits
 - Enables IP reuse with advanced wafer node devices
 - Reduced SoC design and validation time
 - Enable multiple sources for 'standard' IP blocks / devices
 - Smaller SoC die size increased yield
 - Lower bump/die stress increased reliability



SoC + 16 chiplets 60um die to die spacing min



FanOut / FOCoS

- Homogeneous partition
 - Yield & cost optimization
 - Scalable integration
- Heterogenous die partition
 - Process and performance optimization
- Medium to high interconnect density
 - 1000's to 10,000's
- Separation of digital/analog/memory
- Benefits
 - Die size, yield and cost optimization
 - Process node / functionality optimization
 - Short, high density interconnect
 - Increased reliability





2.5D TSV

Homogeneous partition

- Yield & cost optimization
- Scalable integration
- Heterogenous die integration
 - SoC, HBM2 & SerDes
- High interconnect density
 - 10,000's to 100,000
 - 40um microbump pitch
- Benefits
 - Silicon interconnect performance
 - High bandwidth interface enablement
 - Reduced power
 - Si on Si first level interconnect
 - System board size reduction





Challenges & Opportunities

- Supply chain
 - Chiplet ecosystem enablement
 - IP chiplet type/functionality development roadmap and priorities
 - Pin out/interface standards (by chiplet type/function) where possible (eg. JEDEC HMB 'chiplet' spec)
 - KGD performance and reliability criteria definition
 - Business model definition and development
 - Who is selling what to whom? What are associated liability limitations?
- Design & Simulation
 - Co-design flow definition and optimization
 - Development of packaging PDK for various package integration solutions
 - Import and integration capability of multi-device GDS into package design tool
 - Chiplet representation for EDA ODSA CDX (Chiplet Design Exchange)
 - Multi-physics simulation tools for multi-device integration design validation
 - SiP and virtual SoC system simulation
- DFT/Test
 - Chiplet KGD testing standards & criteria
 - Debug and final test of multi device SiP or virtual SoC
 - Failure isolation and identification
 - ATE vs. SLT



Summary





Thank You

www.aseglobal.com

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