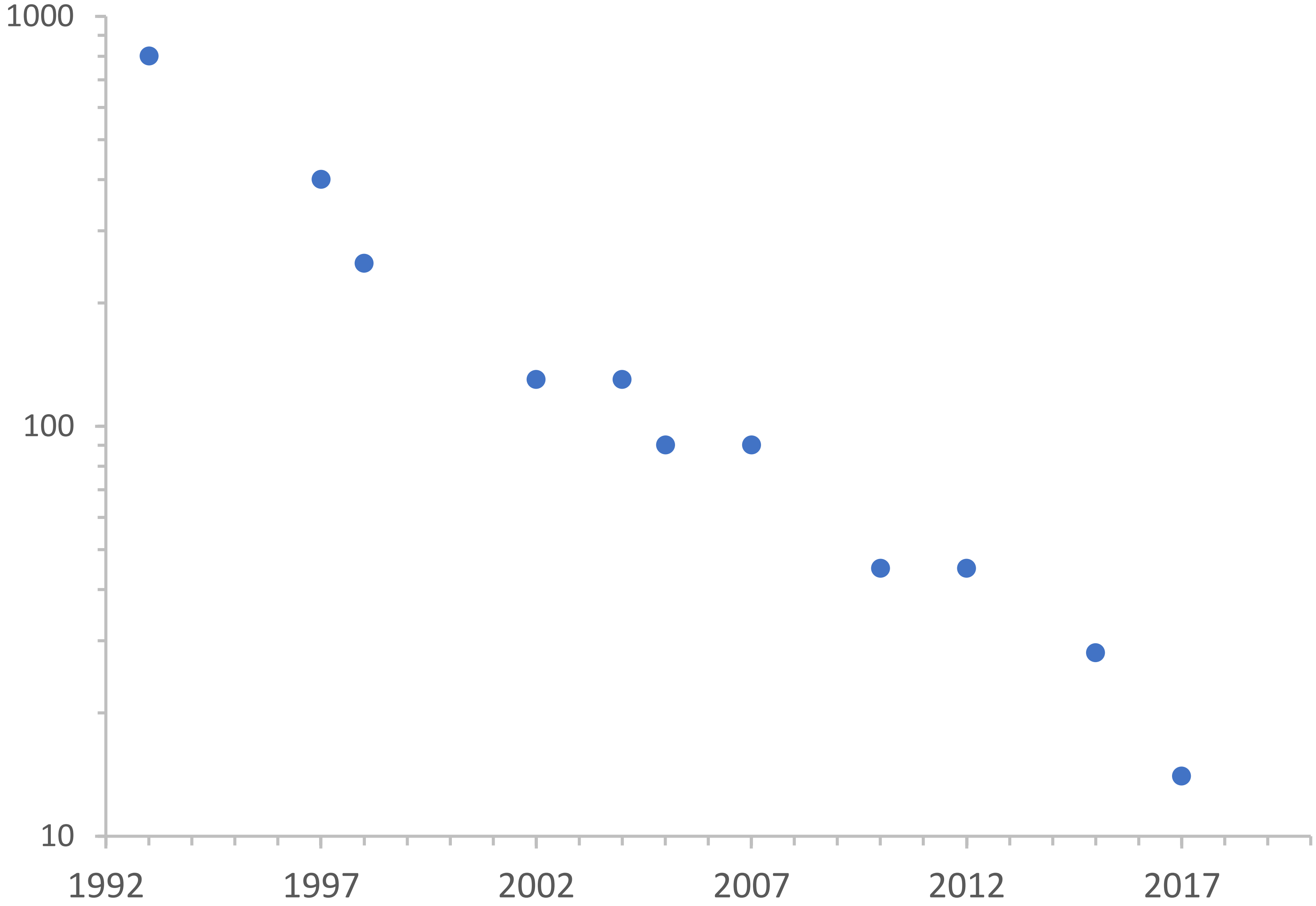
Die-to-die interconnect in a post-Moore world

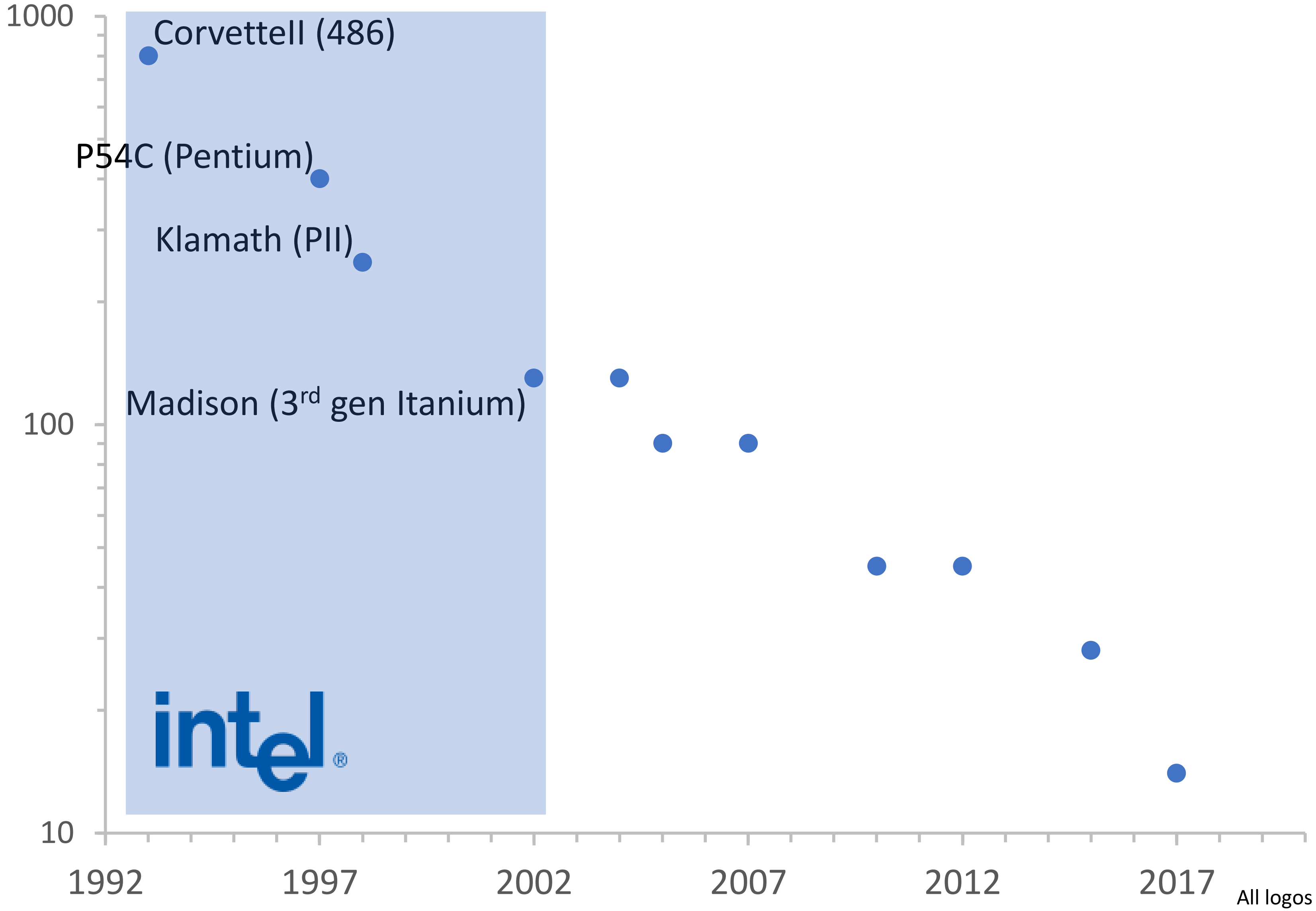
Ron Ho, Ph.D.

Director, Silicon Engineering, Facebook

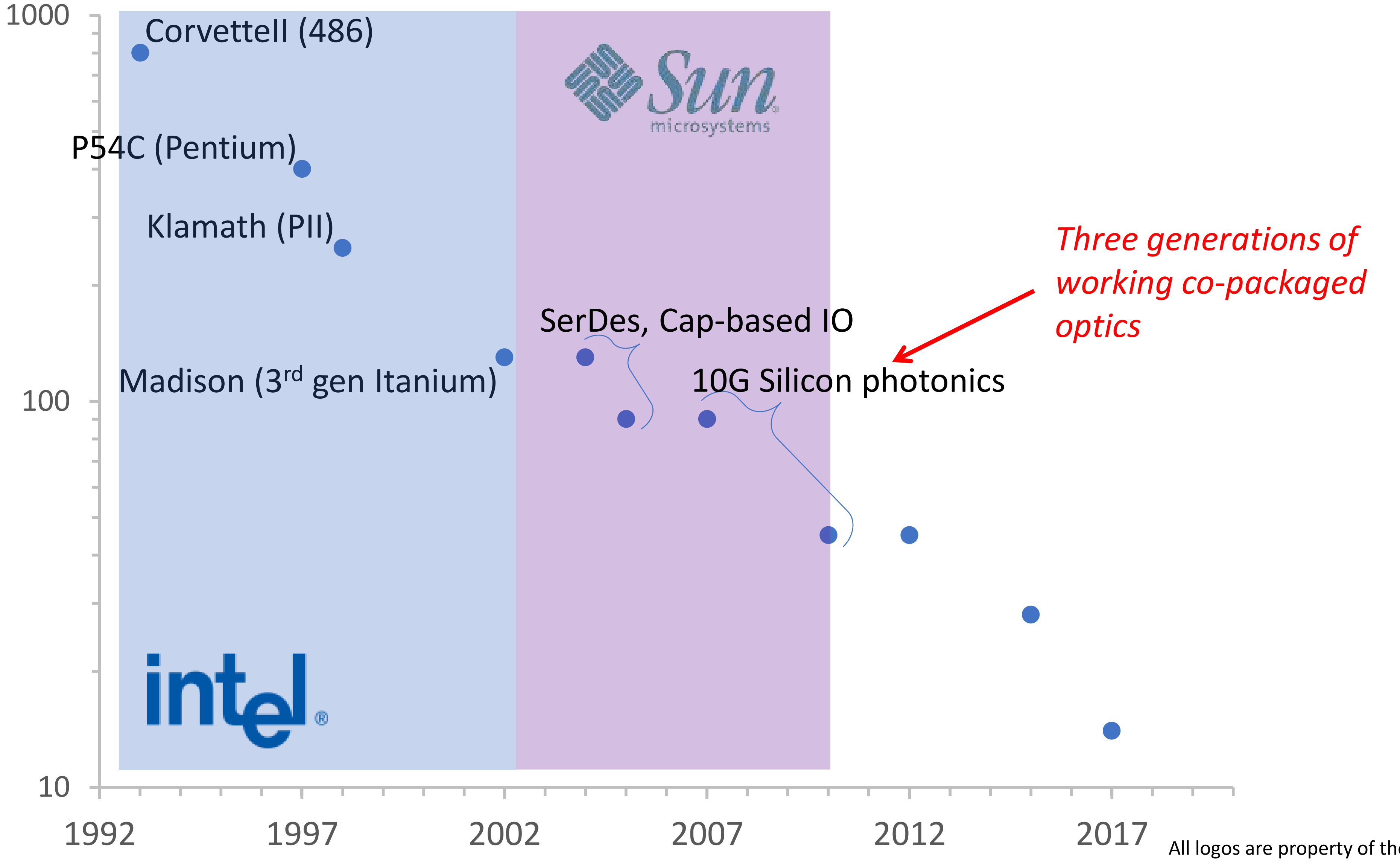
A personal corporate history of Moore's Law



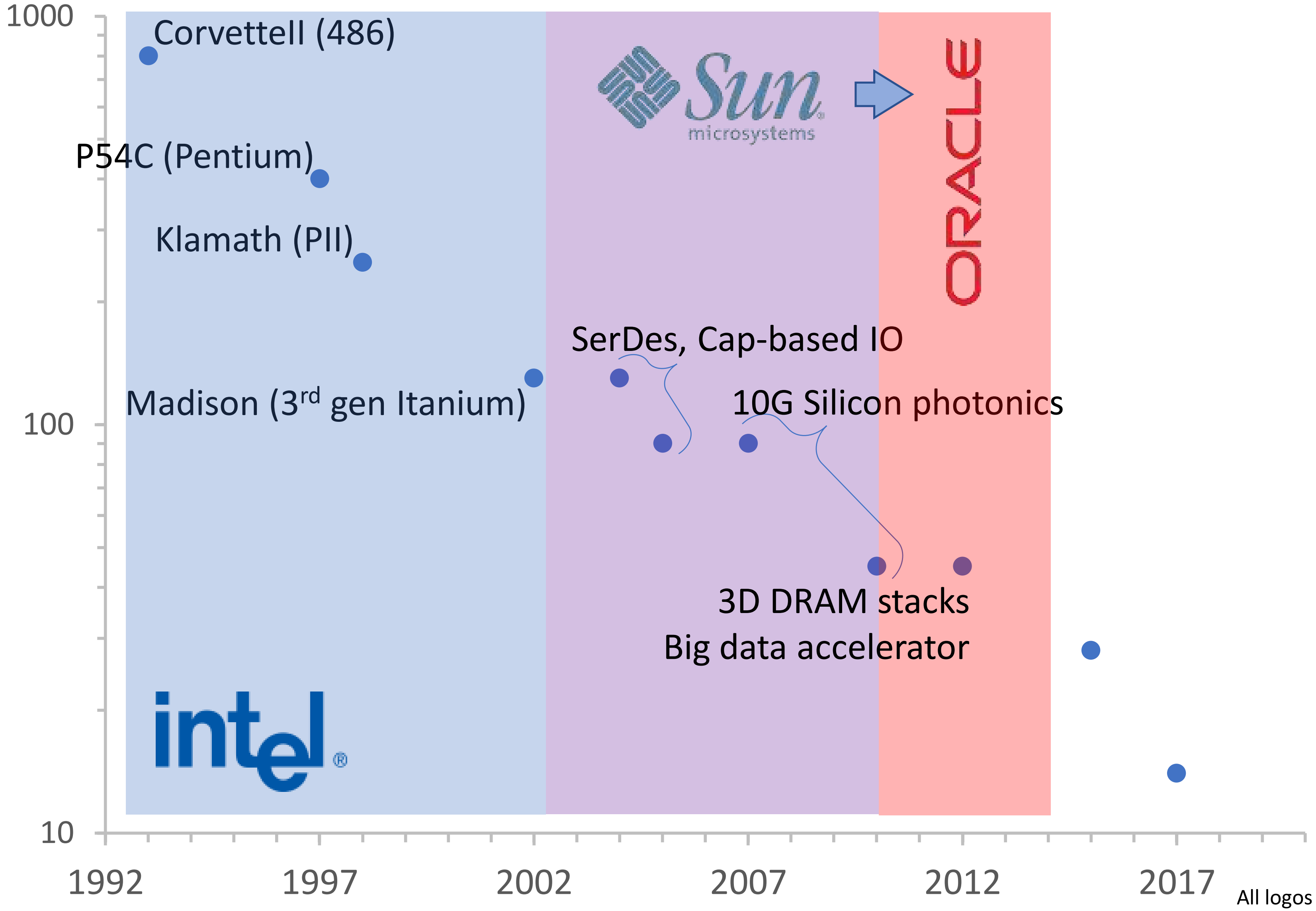
Only the paranoid survive!



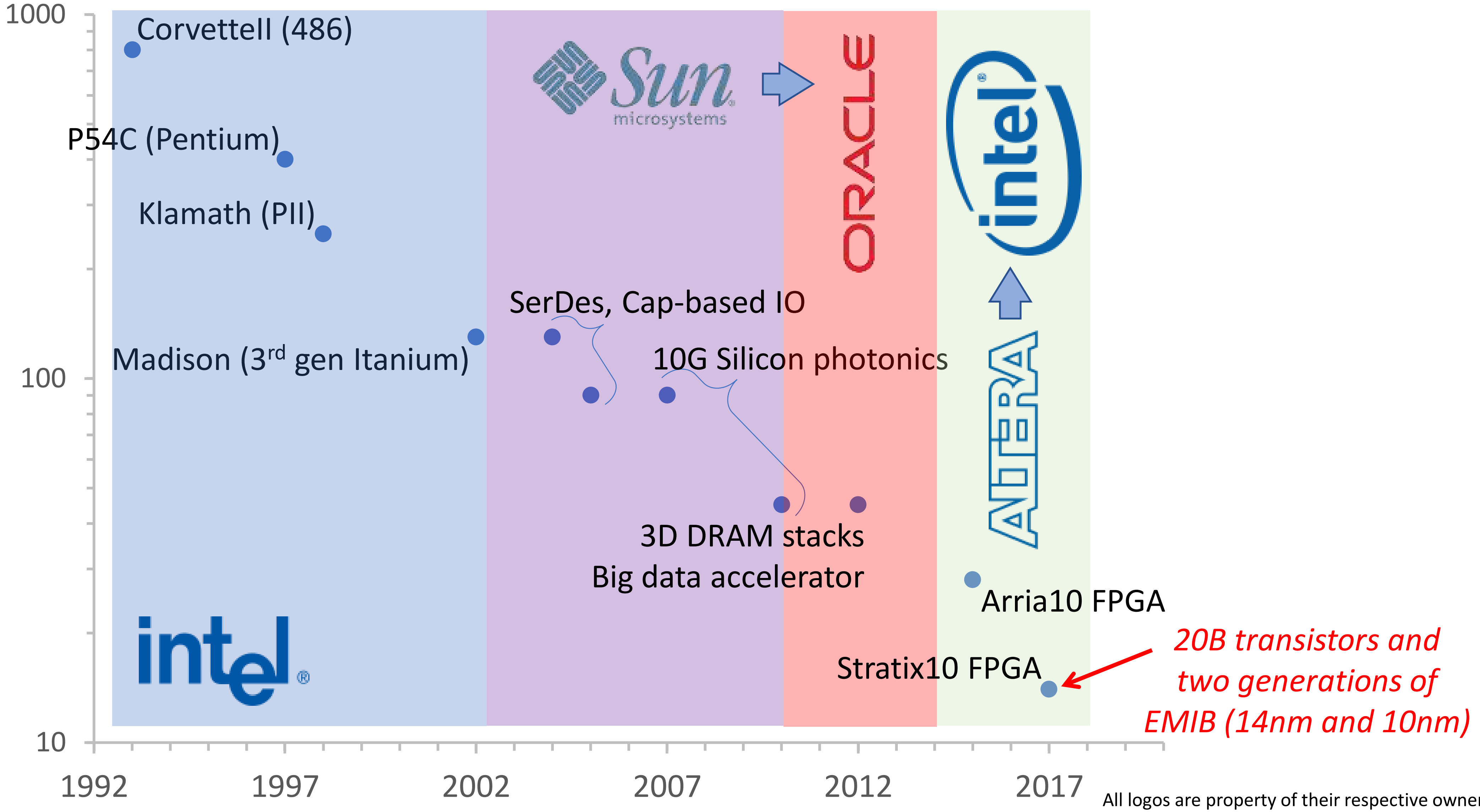
Can “Super IO”™ obviate Moore’s Law?



Big data: SW peeps decide to build HW!

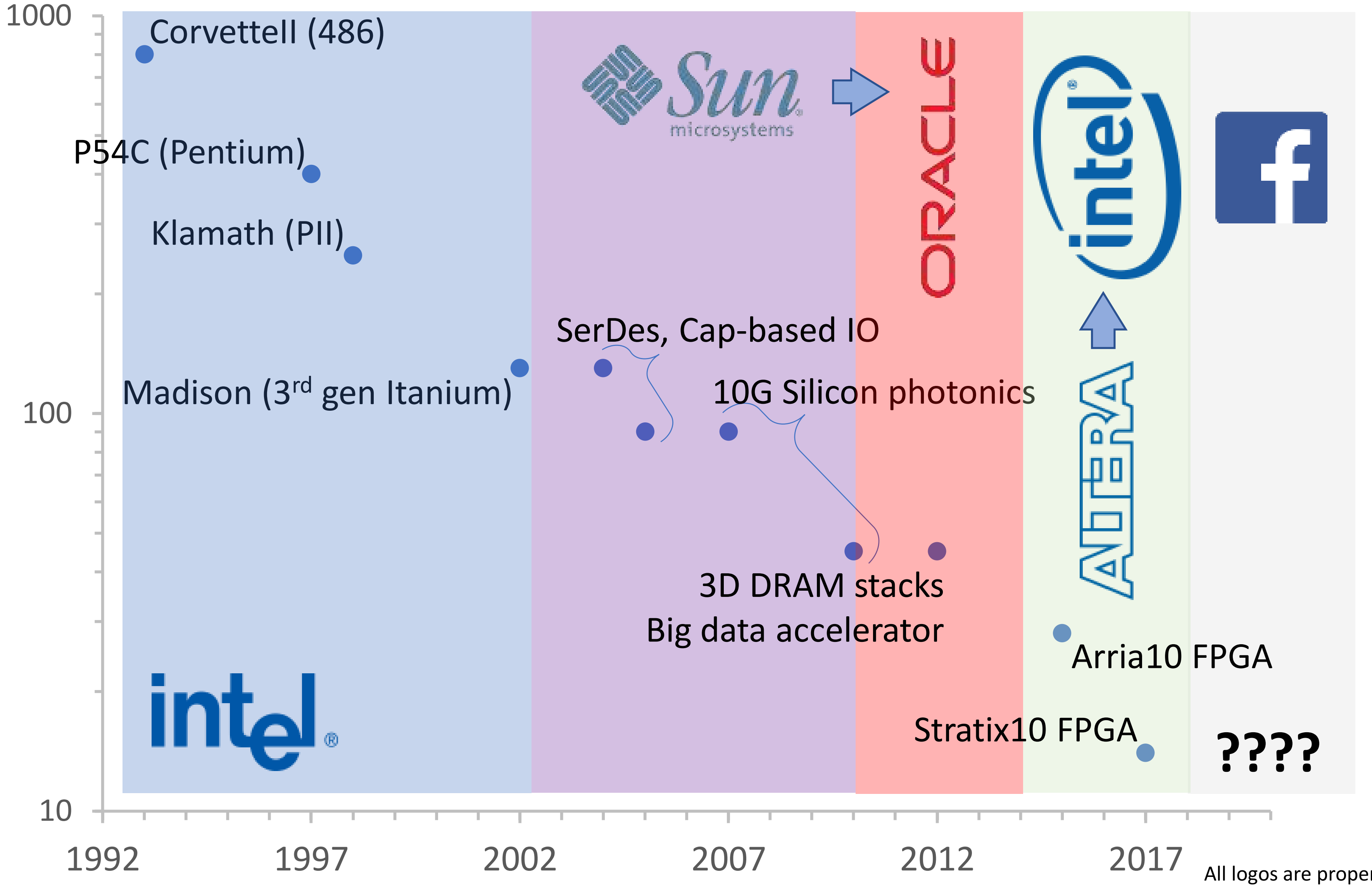


But custom Si is too costly for most people!

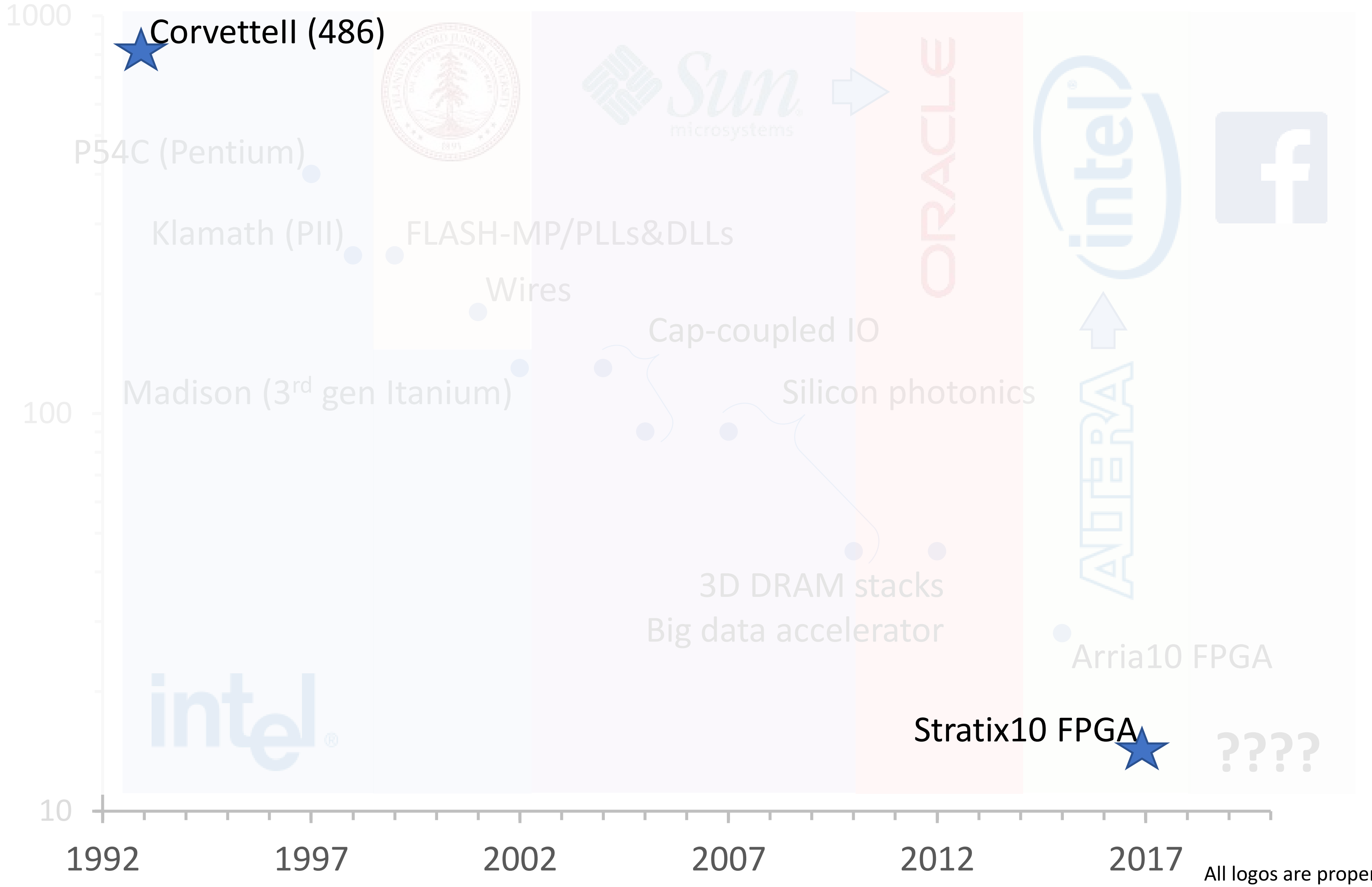


All logos are property of their respective owners.

AR/VR: SW peeps decide to build HW!

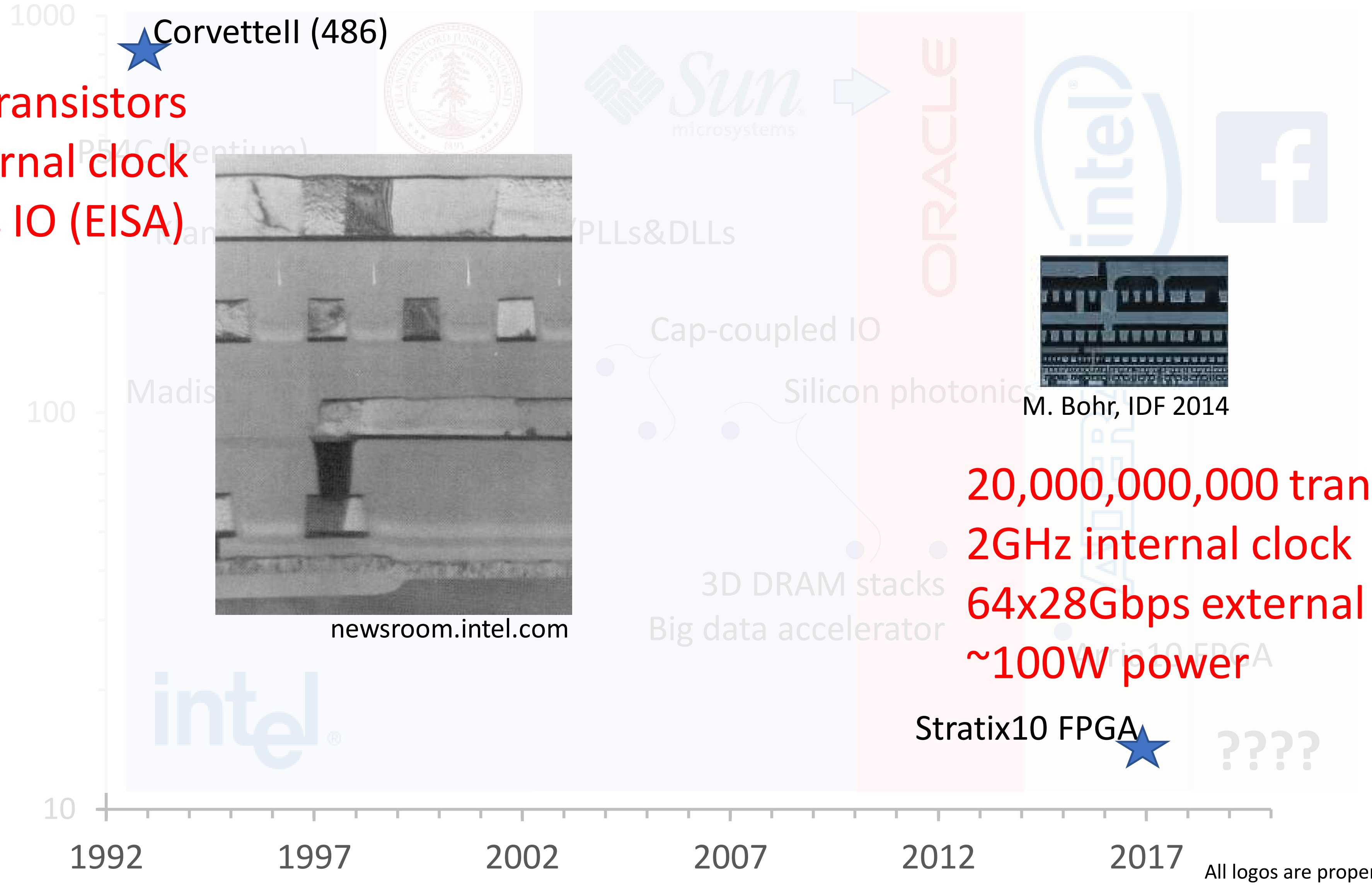


Moore’s Law in a nutshell



Moore’s Law in a nutshell

1,000,000 transistors
25MHz internal clock
32x10Mbps IO (EISA)
~5W power



newsroom.intel.com

M. Bohr, IDF 2014

20,000,000,000 transistors
2GHz internal clock
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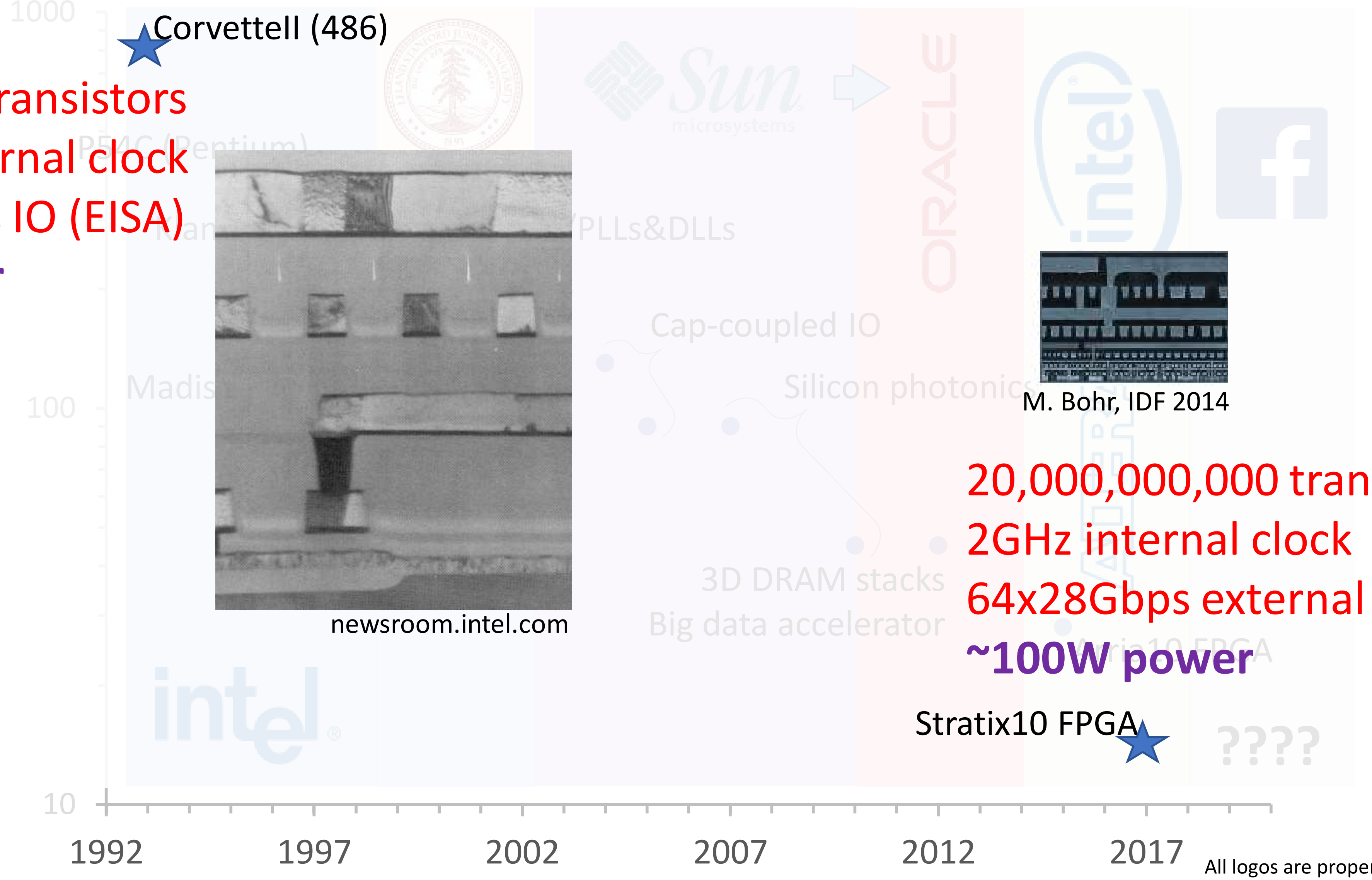

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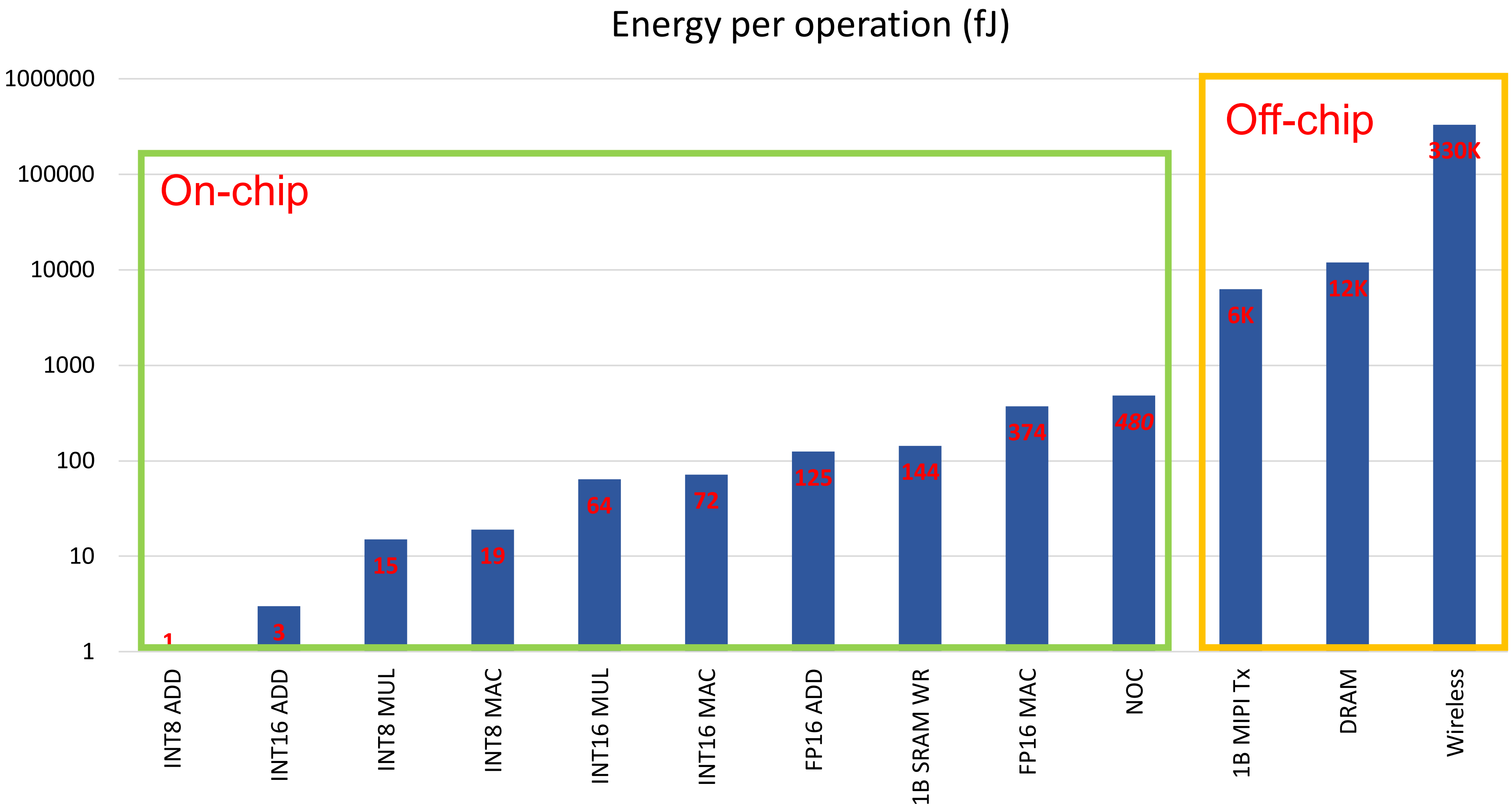
Why Moore’s Law has been so great

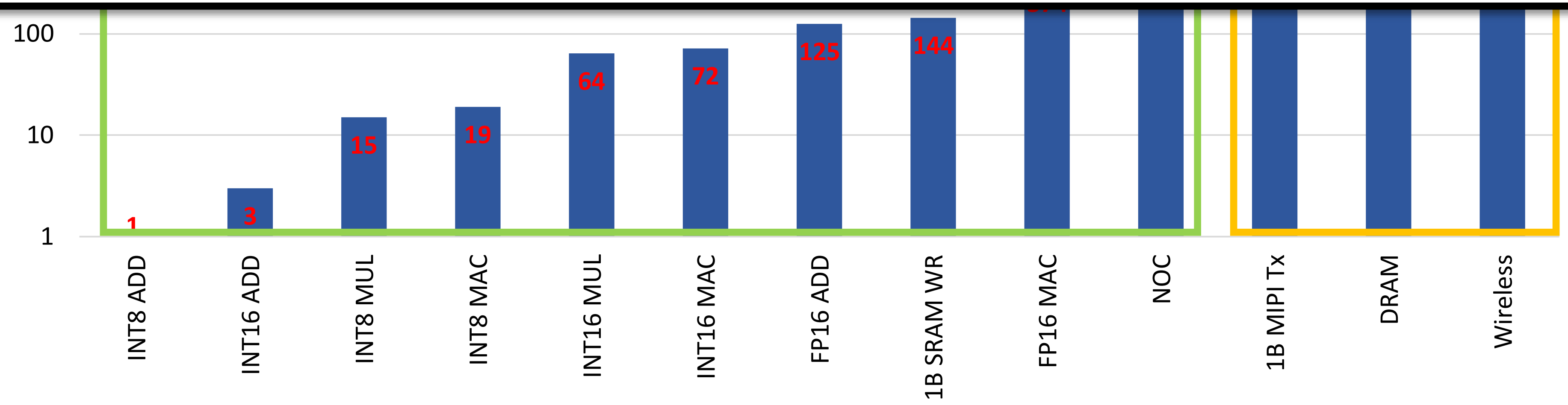


S. Rabii, VLSI Symp. 2019

Why Moore's Law has been so great

Energy efficiency is EVERYTHING

Power	=	Energy / operation	*	operation / second
	=	Energy efficiency^{-1}	*	performance
[const]	=	[drive down]	*	[drive up]



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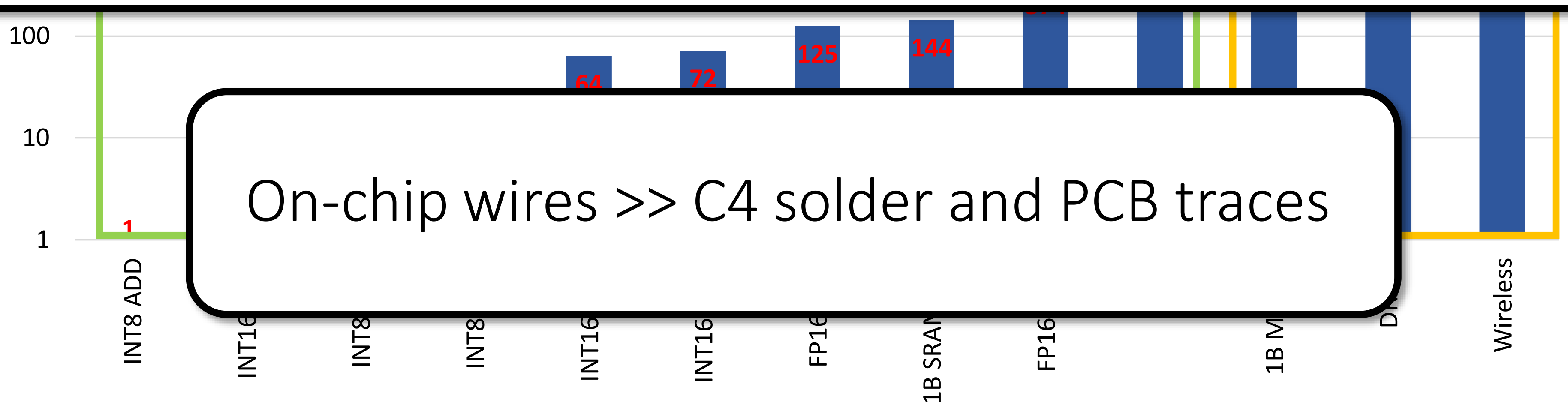
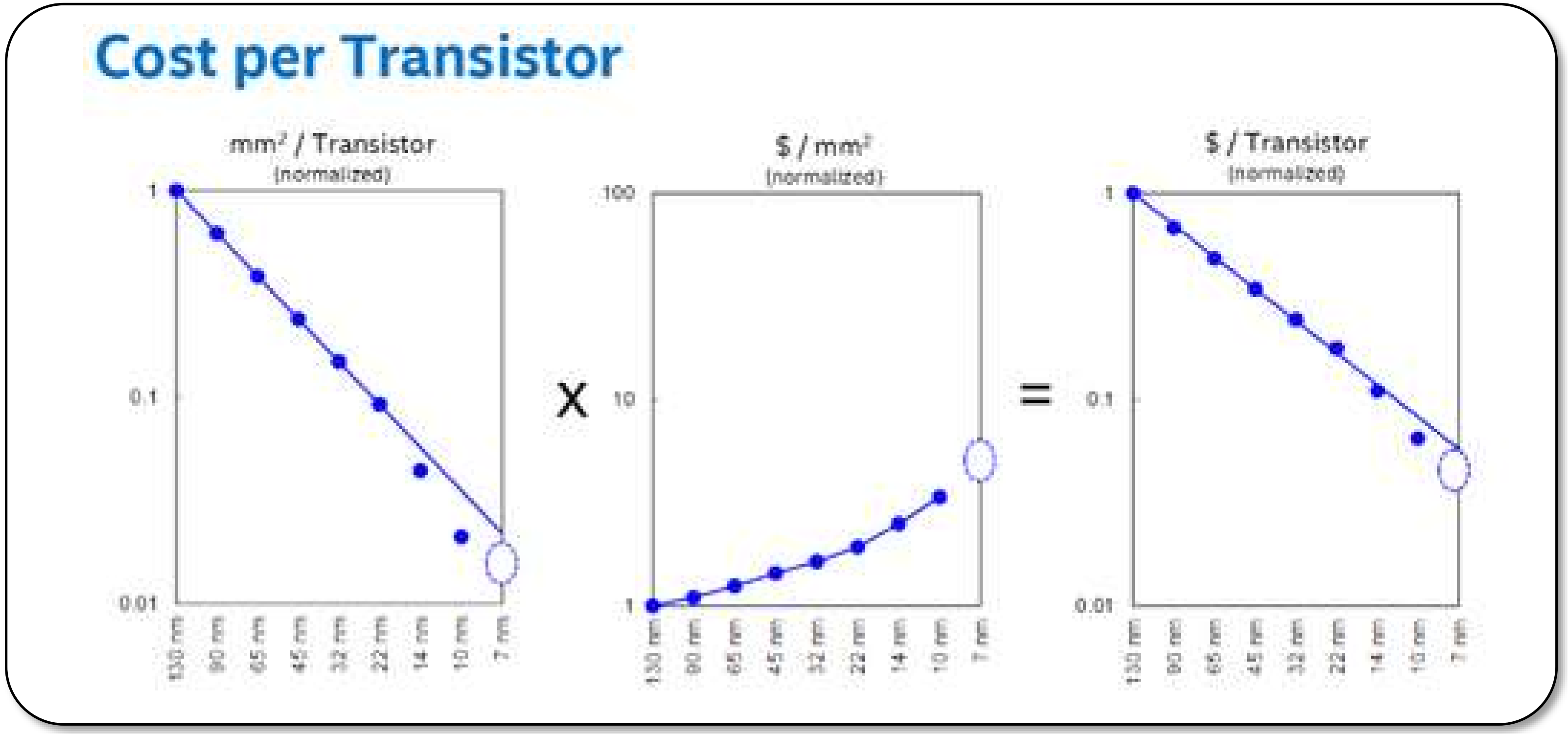


On-chip wires >> C4 solder and PCB traces

S. Rabii, VLSI Symp. 2019

Wait… isn't Moore's Law dead?

- This is the theory…

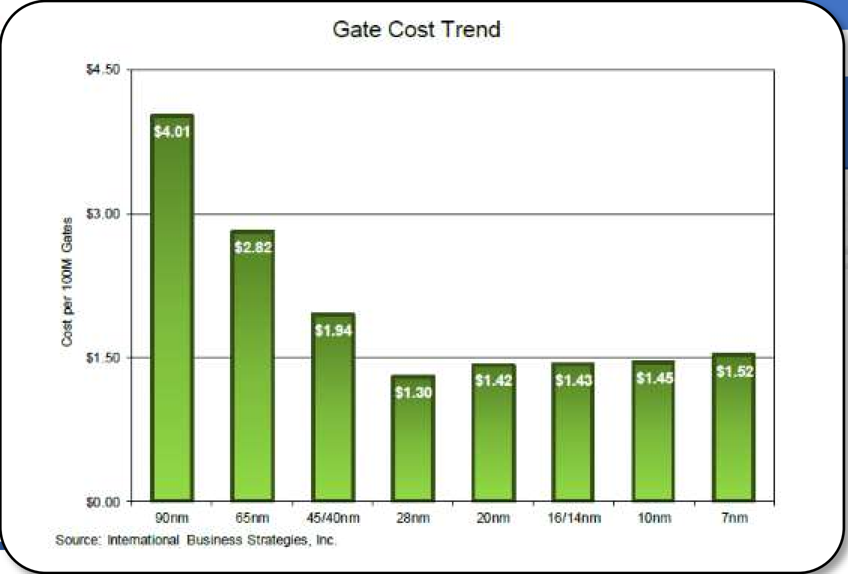


M. Bohr, IEDM 2015

Hm. It's certainly dying…

Why EUV Is So Difficult

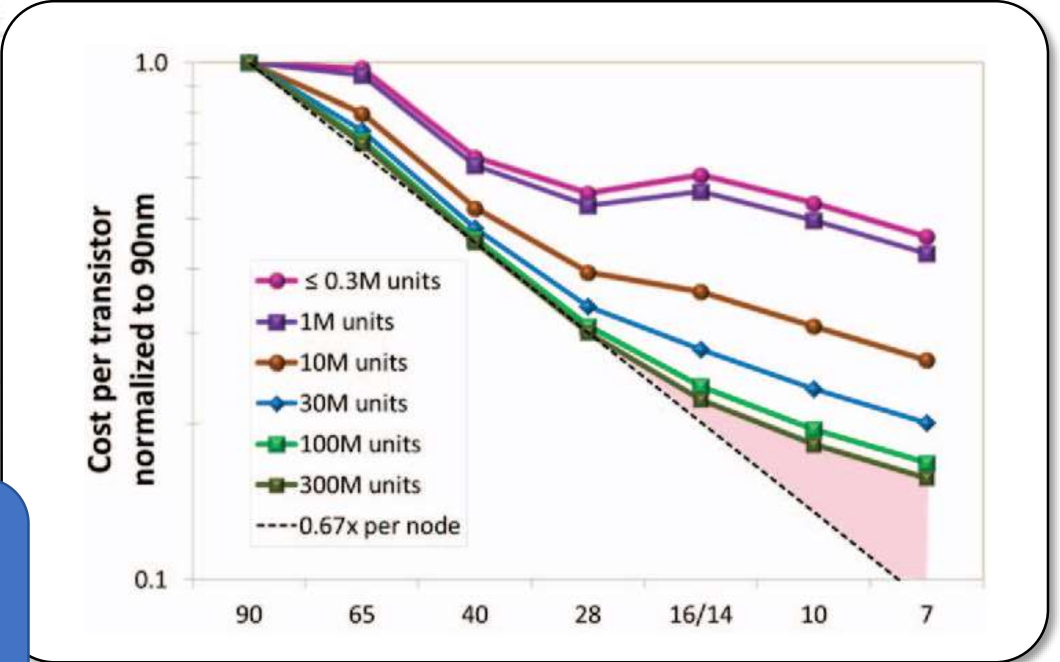
669



IBS, 2016

"…GF is putting its 7nm FinFET program on hold indefinitely…"

globenewswire.com, 8/27/18



G. Yeric, IEDM 2015

BUSINESS

Chip factory spending to hit all-time high of $67.5 billion in 2019

"Intel's slip on 10nm is significant."

extremetech.com, 5/17/18

Rhetorical question #1

If Moore’s Law enabled “on-chip-everything”;

And “on-chip-everything” enabled low energy;

And “low energy” is EVERYTHING…

What the heck do we do after Moore’s Law?

Rhetorical question #1

If Moore’s Law enabled “

Low-power die-to-die interfaces to the rescue

- Achieve “Moore-like” energy scalability
- Allow multi-die systems w/ energy of monolithic ICs
- Exploit high-density IO to obviate serdes
- Leverage simplicity & standardization (esp. test)

Would you ever NOT want integration?

- You’re porting a design to an advanced FinFET logic process
  - …tuned for low-power CPUs, NOT low-variability high-speed analog circuits
- Unfortunately, you also need 28Gbps standards-compliant Ethernet
  - Do you hire 100 people & spend 2 years to re-design the analog serdes?

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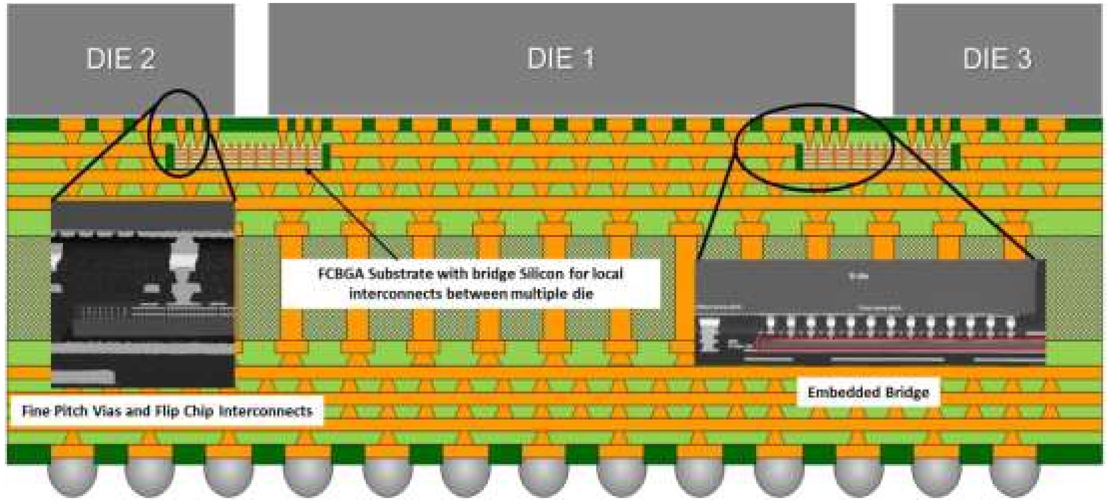
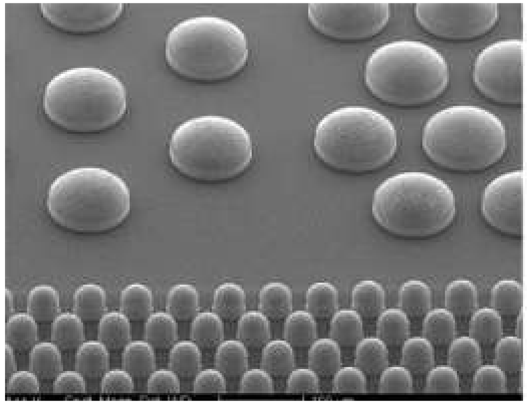
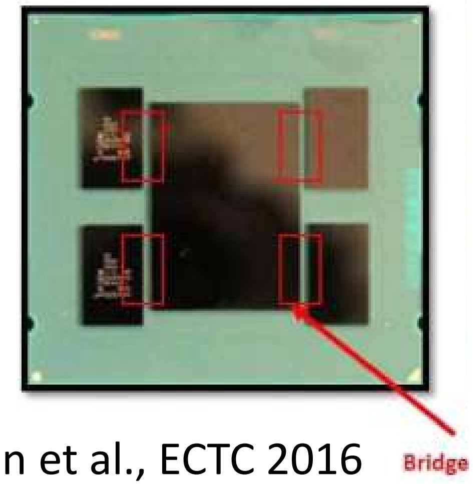






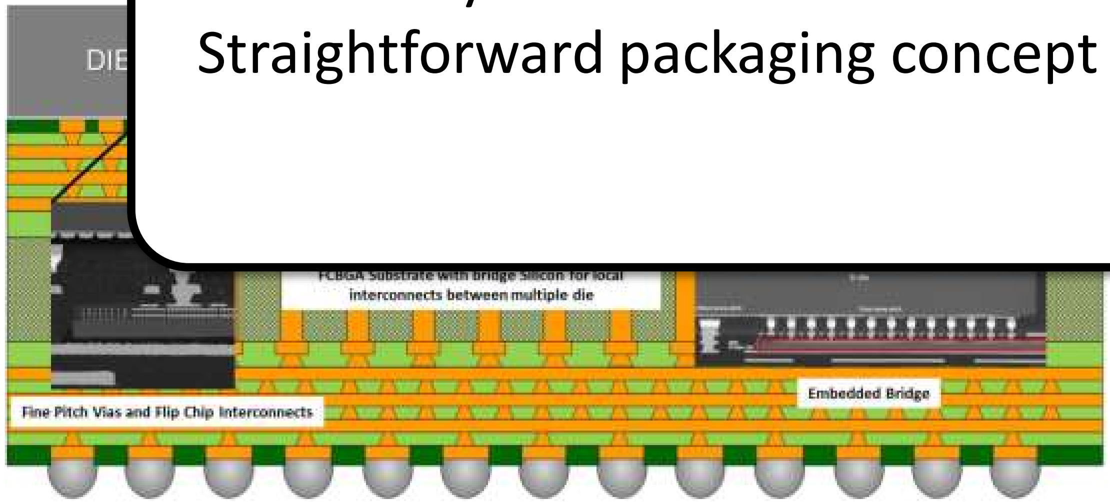
R. Mahajan et al., ECTC 2016

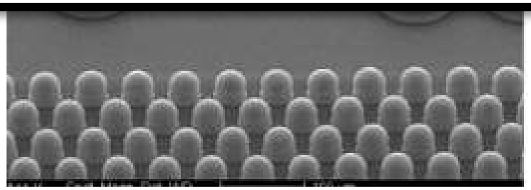
Would you ever NOT want integration?

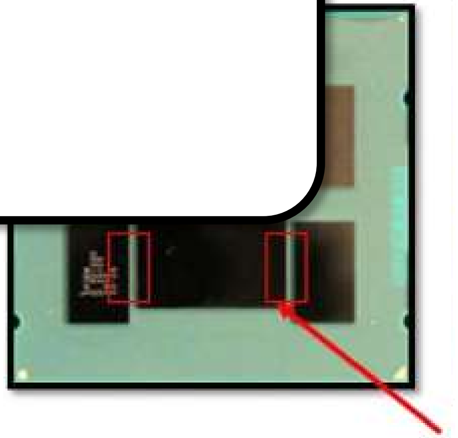
- ~~Yo~~
- U
- N

What are the keys to EMIB?

High-density microsolder to minimize serialization and de-serialization
Short channels whose performance is RC-dominated
Modularity and standardization for “circuit construction of correctness”
Straightforward packaging concept avoids incremental risks







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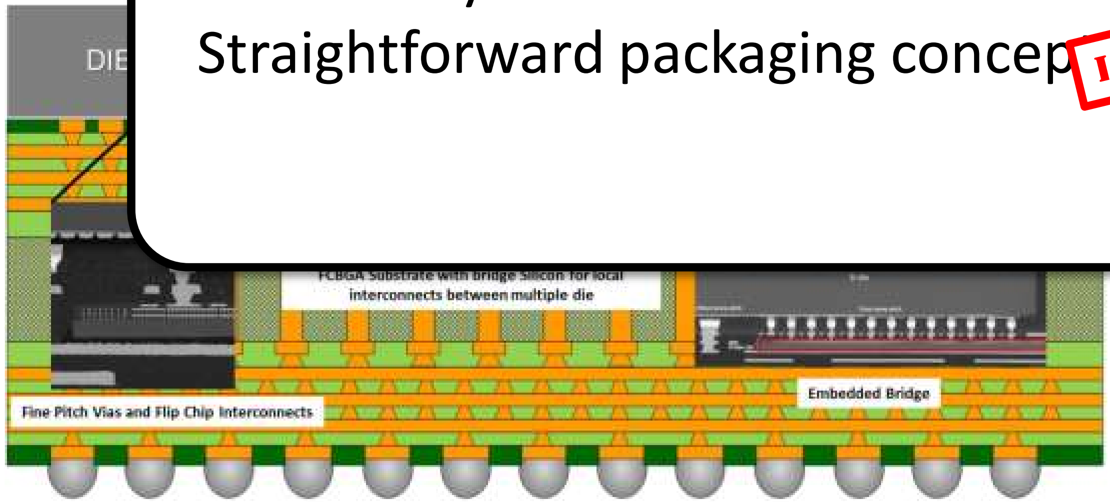
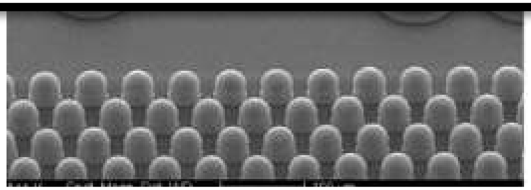
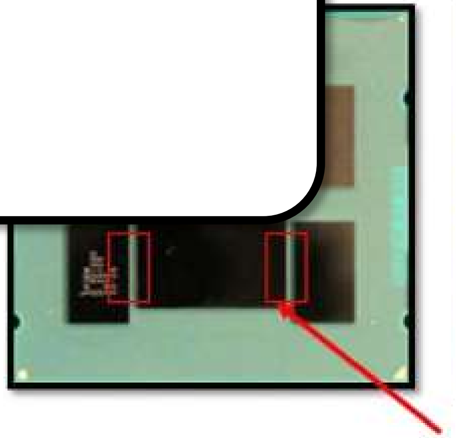


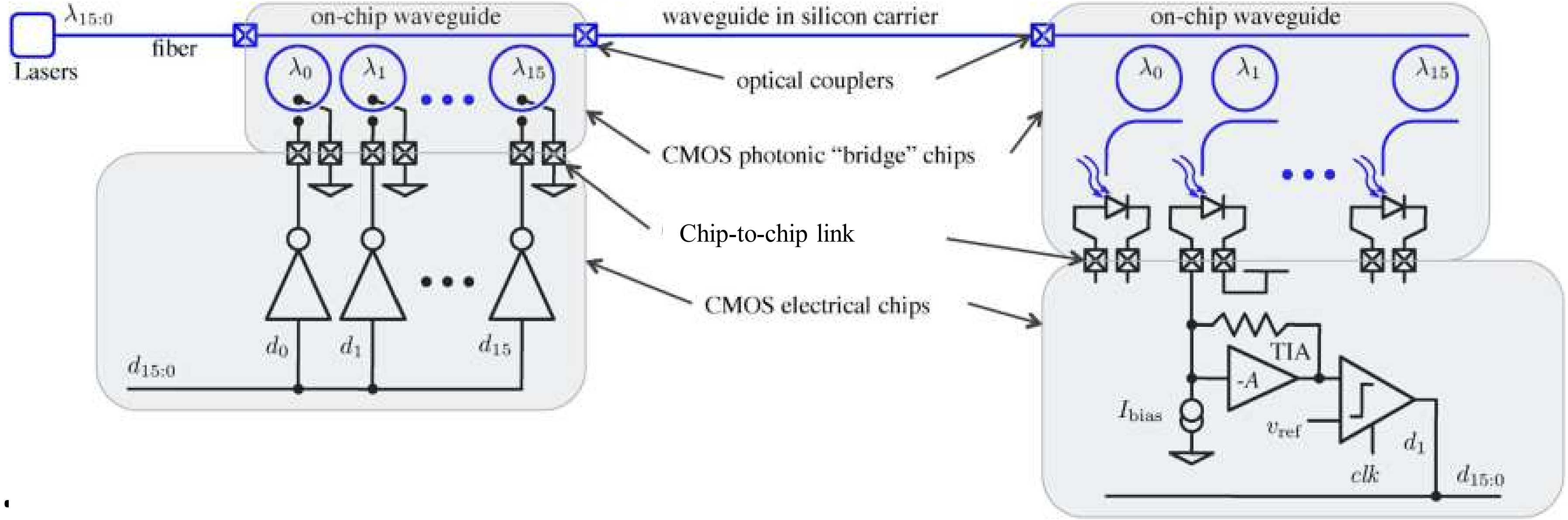




R. Mahajan et al., ECTC 2016

Would you ever NOT want integration?

- You want to build co-packaged optics (the Si photonics edition)
  - …to leverage a >10x improvement in energy/bit over long electrical links



F. Liu et al., JSSC 2012

- But…
  - A transmitter needs silicon processing to minimize thermal effects
  - A receiver needs a non-silicon photodiode and a high SNR

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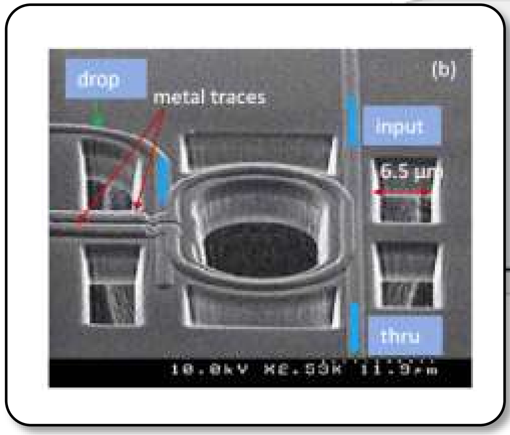
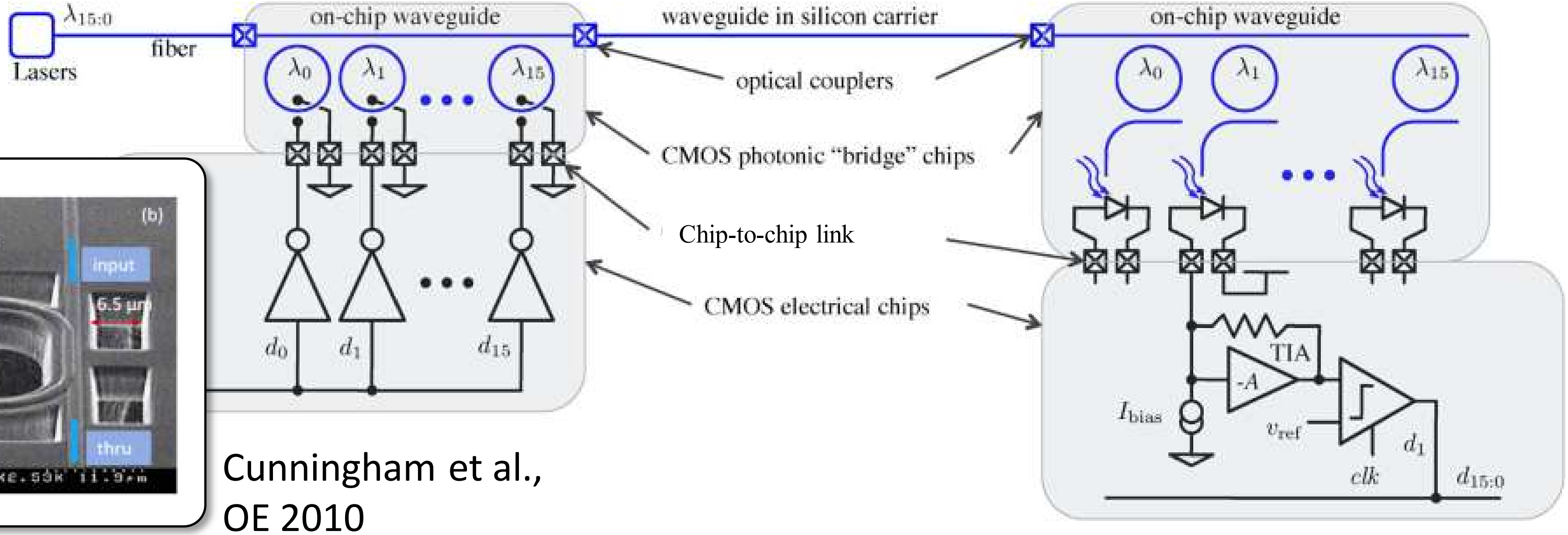


Cunningham et al., OE 2010



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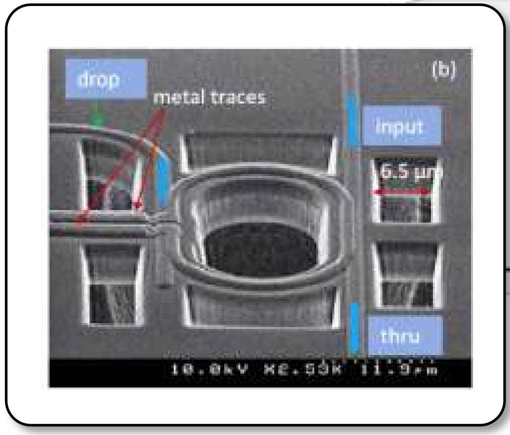
$$R_t = \frac{1}{2\pi \, BW \, C_d}$$



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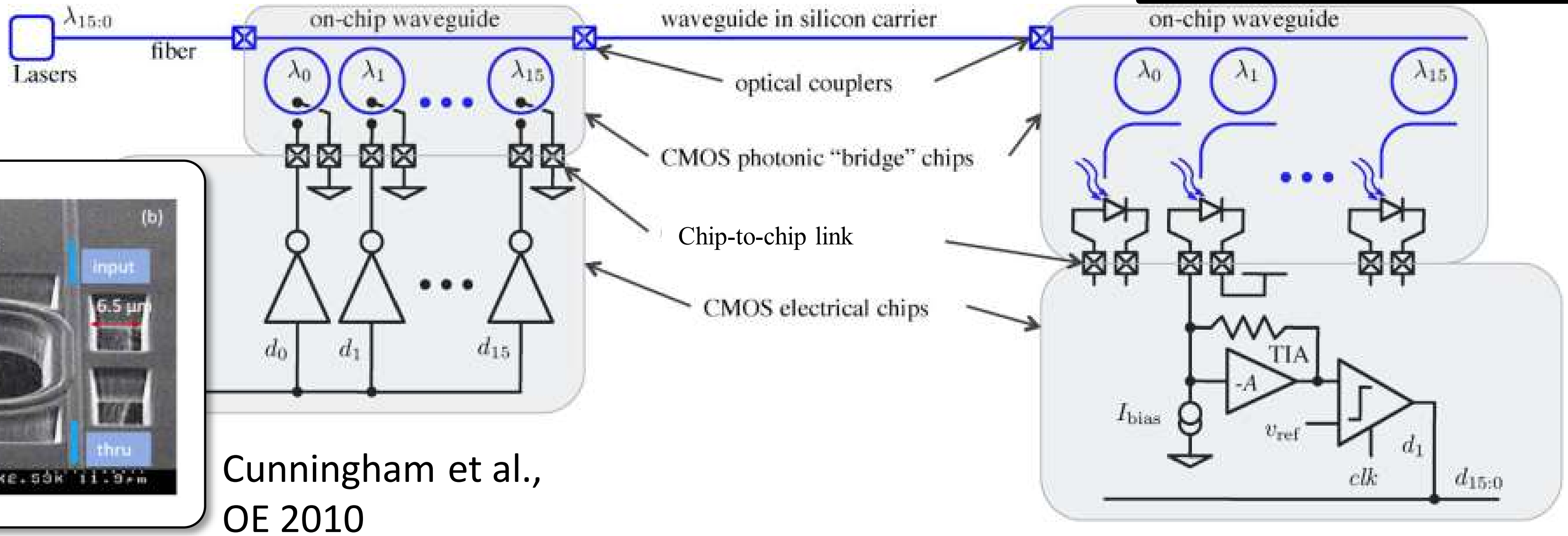

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Would you ever NOT want integration?

• Yo...

What are the keys to photonic integration?

High-density microsolder to minimize serialization and de-serialization

Short channels with minimal capacitive loading

- TX energy directly proportional to channel capacitance
- RX's SNR inversely proportional to channel capacitance

Separation of optical devices from CMOS enables cost feasibility

- TX's micromachining to reduce thermal crosstalk
- RX's heterogenous materials separated from CMOS fab

u et al.,
SC 2012

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u et al., SC 2012

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Rhetorical question #2

We don’t always ***want*** monolithic chips;

Separate chips can be simpler, less risky, or lower cost;

How do we enable such heterogenous systems?

Rhetorical question #2

We don't always

Sep cost;

?

Standardized die-to-die interfaces to the rescue

- Separate chips with "unlike" technology needs
- Enable low-cost micromachining in production
- Exploit high-density IO with small parasitics
- Again: leverage simplicity & standardization

The virtue of simplified die-to-die interfaces

Use cases are pretty clear

- Extend (cost and energy versions of) Moore’s Law
- Enable tailoring of silicon needs to diverse applications

Key characteristics are also pretty clear

- Low energy (and low-cost) is critical
- Simplicity and standardization unlocks productization

Thank you

Rhetorical question #1

If Moore’s Law enabled “ thing”;

And “on-chip- nergy;

What Law?

Low-power die-to-die interfaces to the rescue – *make multi-die systems the energy equivalent of monolithic ICs*